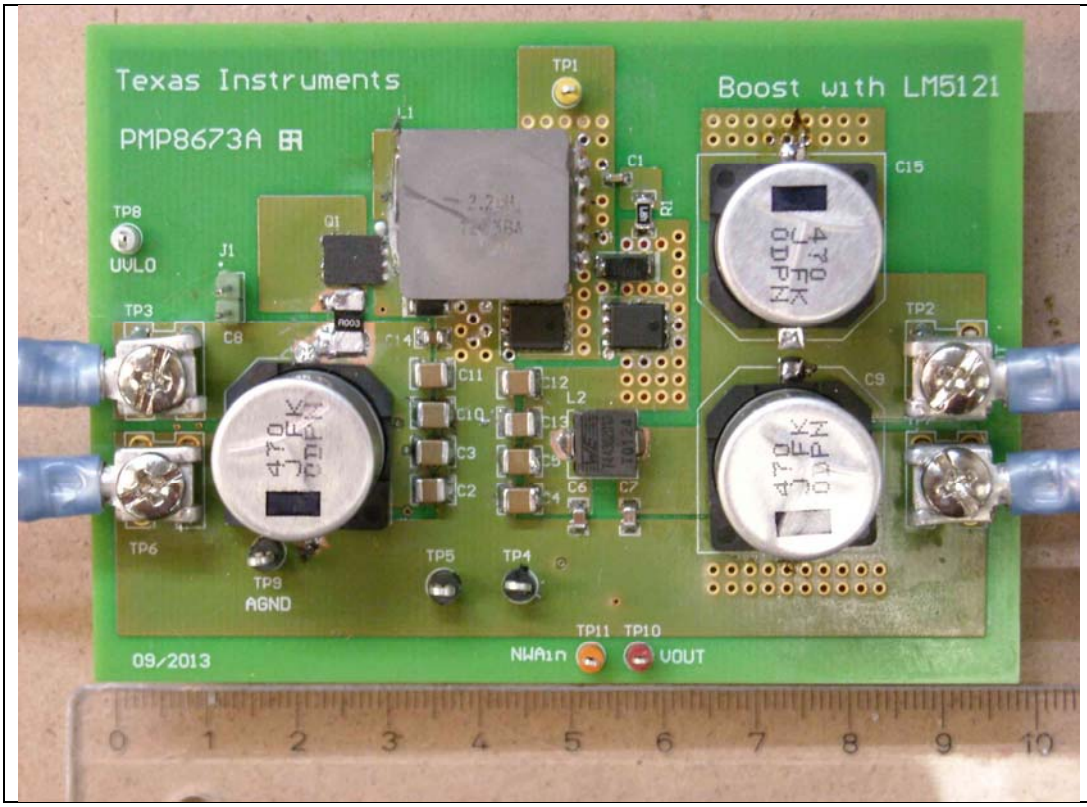
PMP10092RevA Test Results

Topology: Boost
Device: LM5121



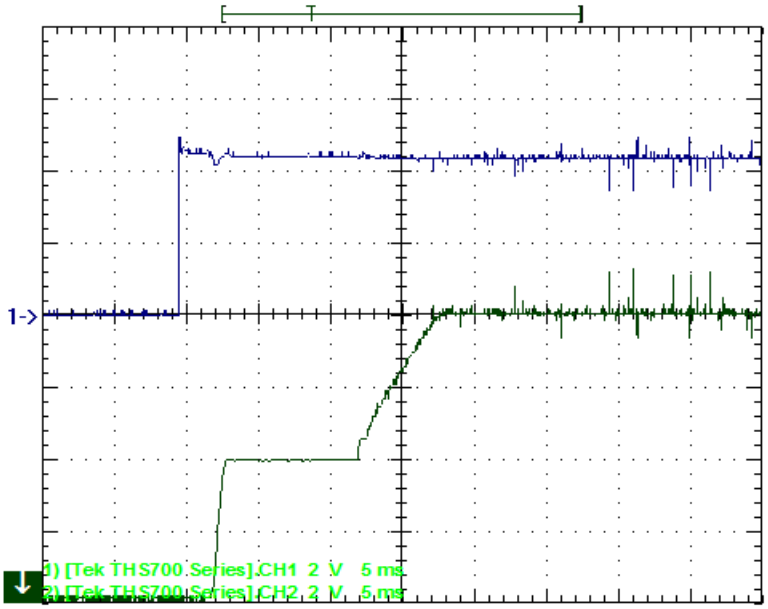
The measurements were done with additional airflow at 3Vin unless otherwise mentioned;
The board is operational down to Vin 4.5V w/out bias power;
For operation at Vin 3V..4.5V a bias supply is needed to power Vcc in a range 9V..14V;
For this test purposes the design simply has been powered out of Vout, means:

- **startup needs input voltage >4.5V**
- **maximum input voltage <14V; at higher Vin the controller will be damaged**

Furthermore:
Full load operation at Vin 3V needs a source that is able to drive >25Adc
Limit continuous full load operation <60secs or use forced cooling 1m/s (200lfm)

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 4.5V, with 7A load at the output. Power supply was connected.



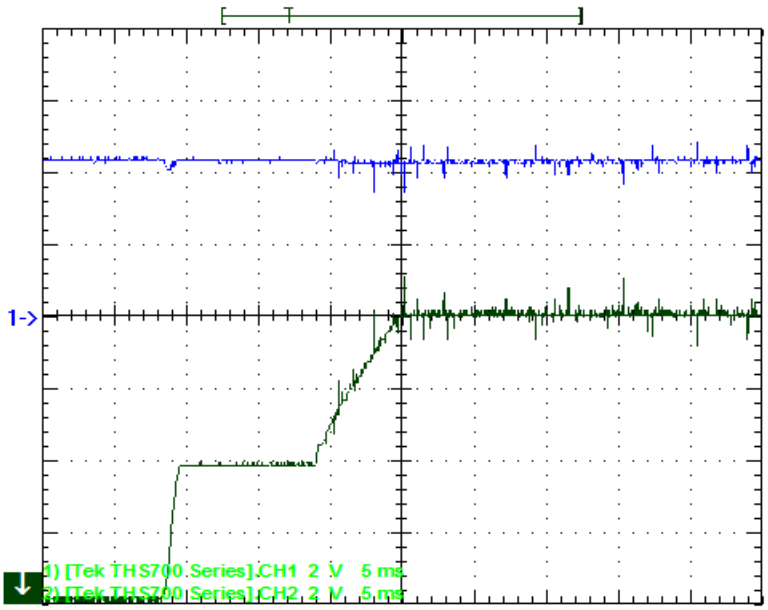
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

5ms/div

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 4.5V, with 7A load at the output. Power supply output enabled.



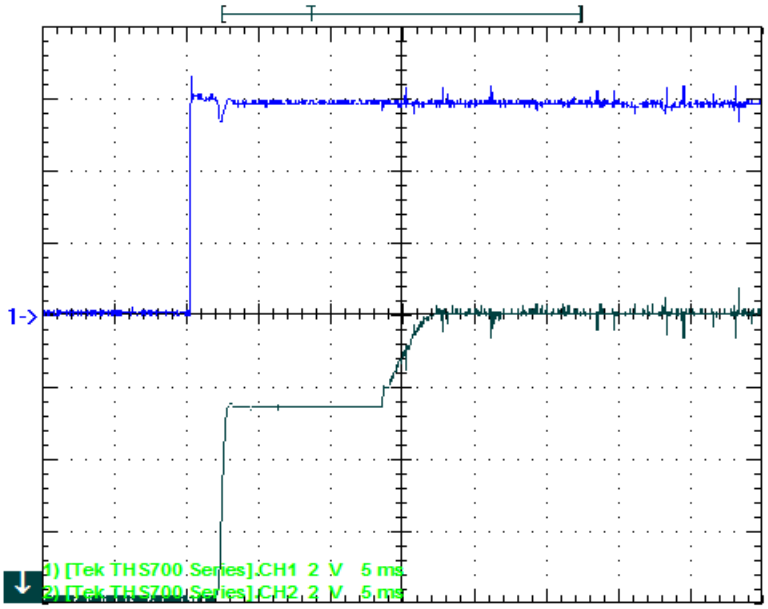
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

5ms/div

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set at 6V, with 7A load at the output. Power supply was connected.



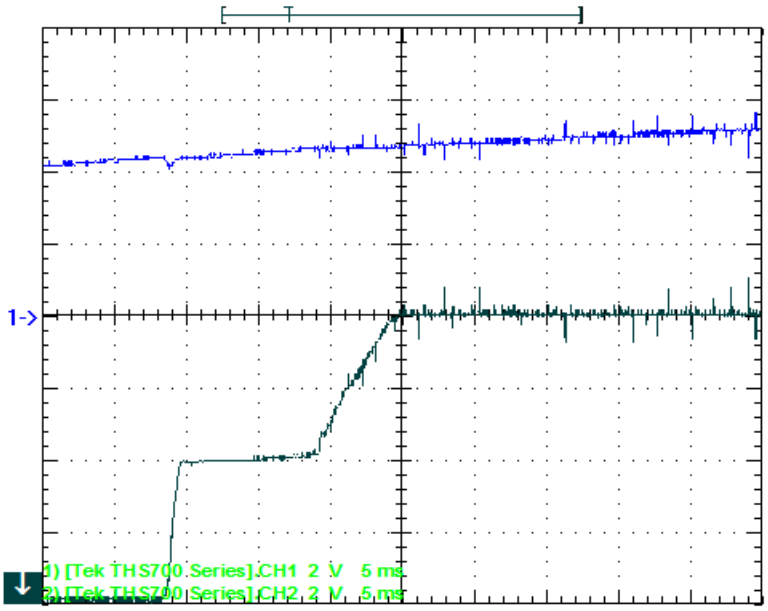
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

5ms/div

Figure 3

The startup waveform is shown in the Figure 3. The input voltage was set at 6V, with 7A load at the output. Power supply output enabled.



Ch1=> input voltage 2V/div

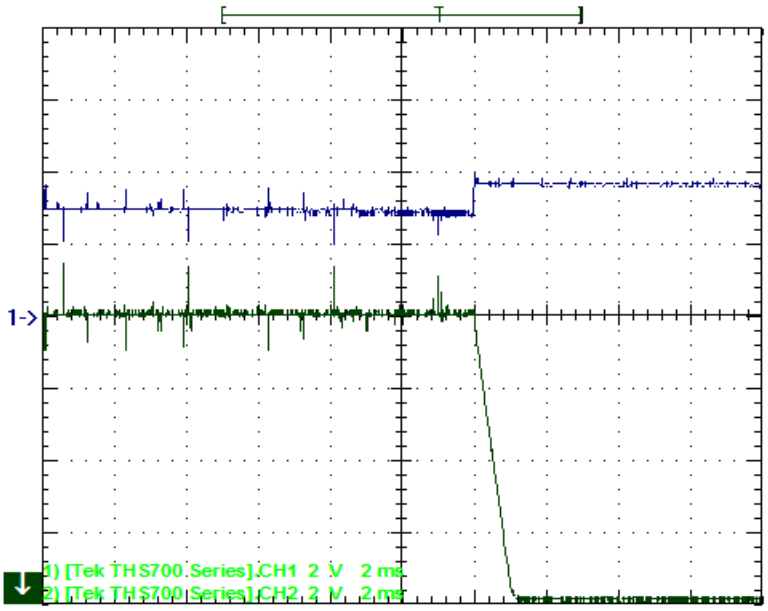
Ch2=> output voltage 2V/div

5ms/div

Figure 4

2 Shutdown

The shutdown waveform is shown in the Figure 5. The input voltage was set at 3V, with 7A load on the output. Power supply was disconnected.



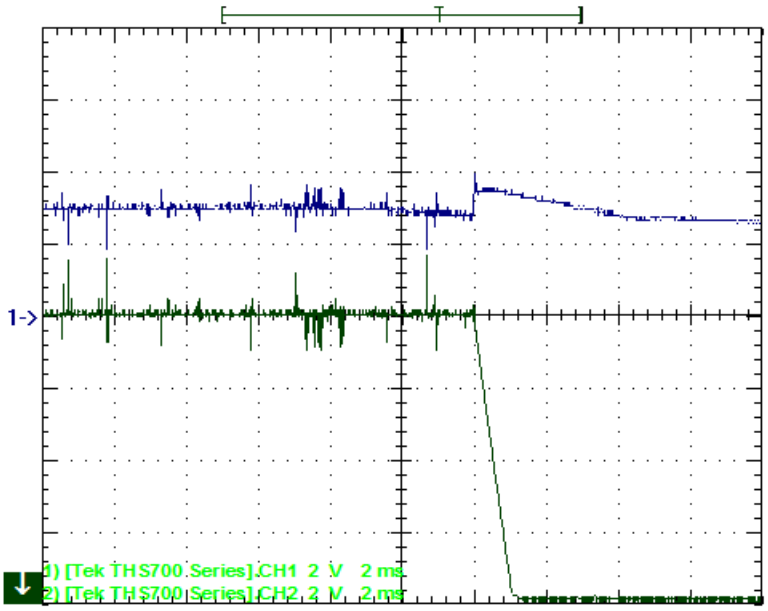
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

2ms/div

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set at 3V, with 7A load on the output. Power supply output disabled.



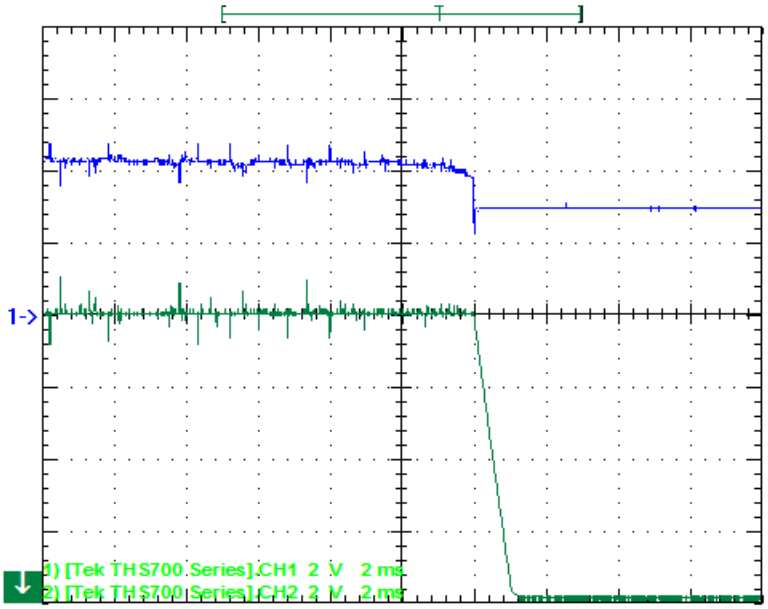
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

2ms/div

Figure 6

The shutdown waveform is shown in the Figure 7. The input voltage was set at 4.5V, with 7A load on the output. Power supply was disconnected.



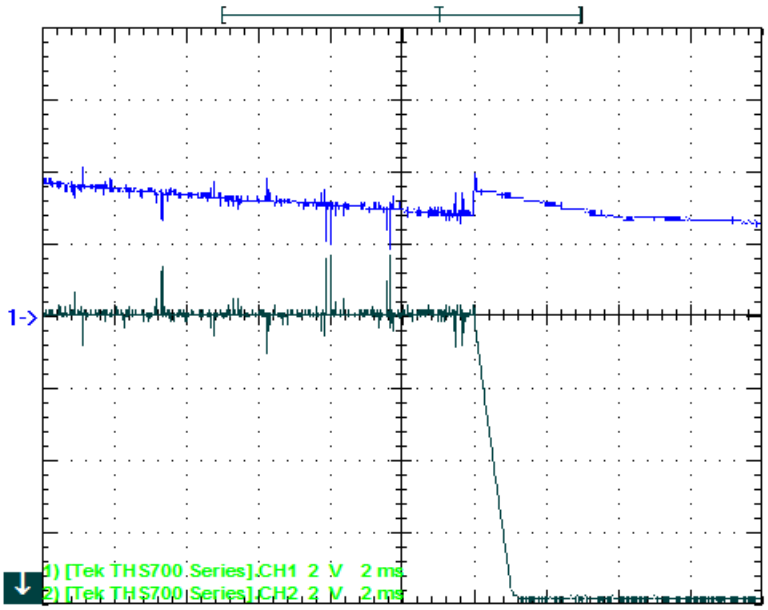
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

2ms/div

Figure 7

The shutdown waveform is shown in the Figure 8. The input voltage was set at 4.5V, with 7A load on the output. Power supply output disabled.



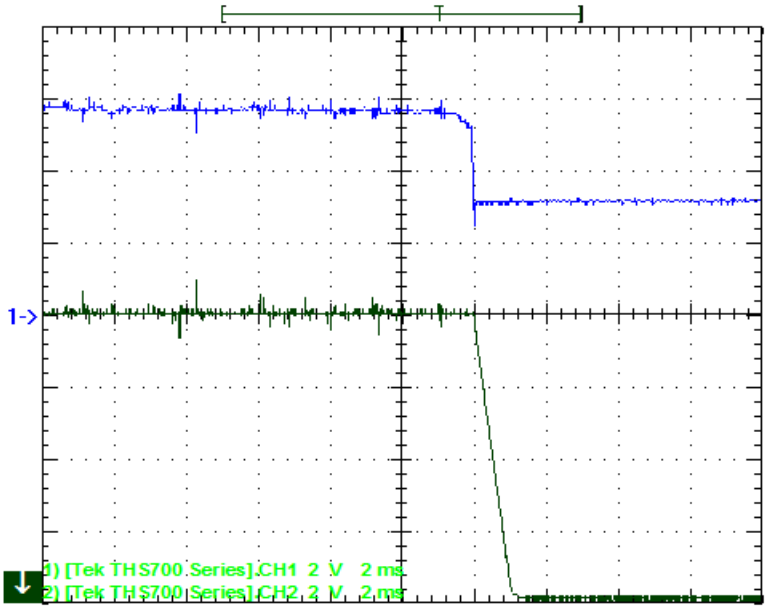
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

2ms/div

Figure 8

The shutdown waveform is shown in the Figure 9. The input voltage was set at 6V, with 7A load on the output. Power supply was disconnected.



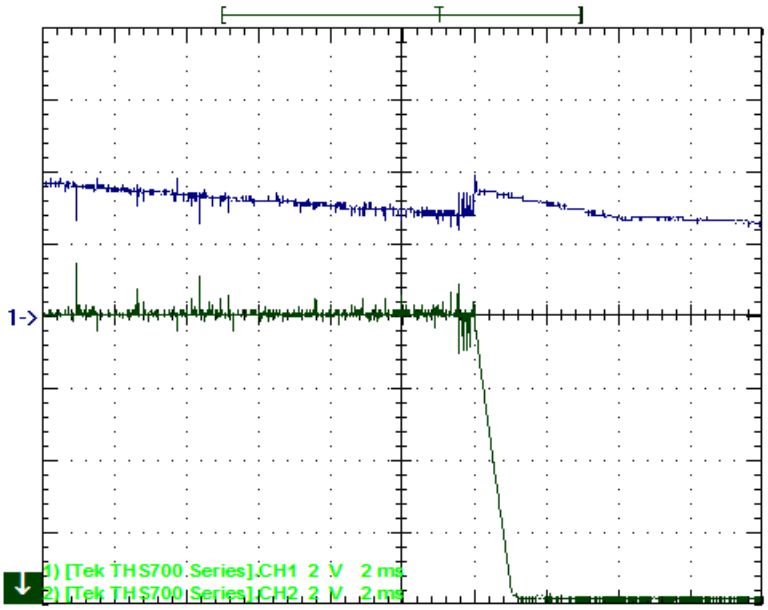
Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

2ms/div

Figure 9

The shutdown waveform is shown in the Figure 10. The input voltage was set at 6V, with 7A load on the output. Power supply output disabled.



Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

2ms/div

Figure 10

3 Efficiency

The efficiency is shown in the Figure 11 below.

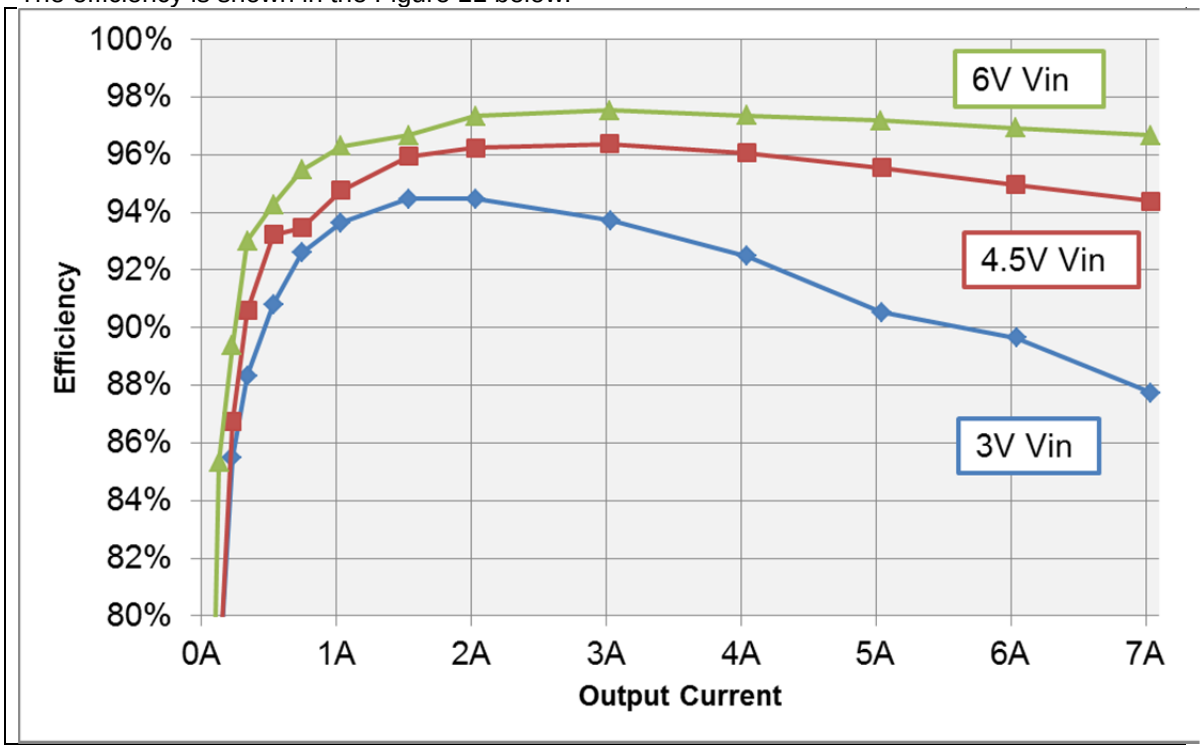


Figure 11

4 Load Regulation

The load regulation of the output is shown in the Figure 12 below.

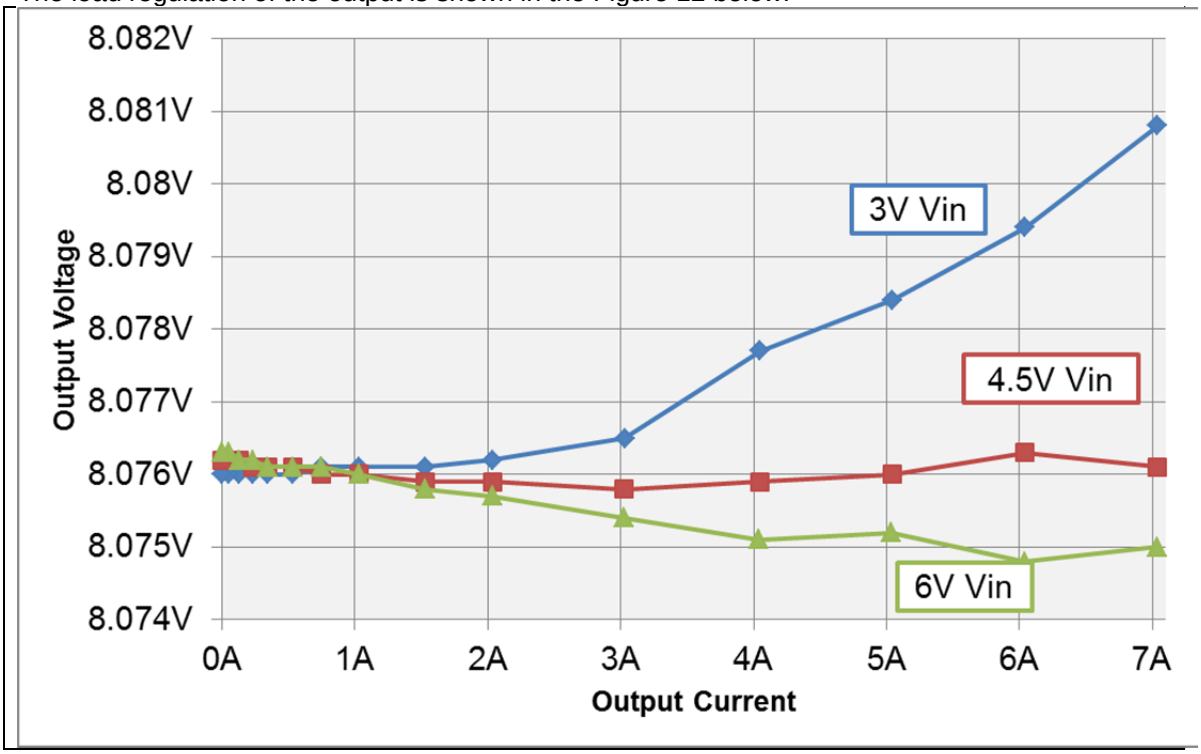


Figure 12

5 Line Regulation

Line regulation at 7A output current is shown in Figure 13

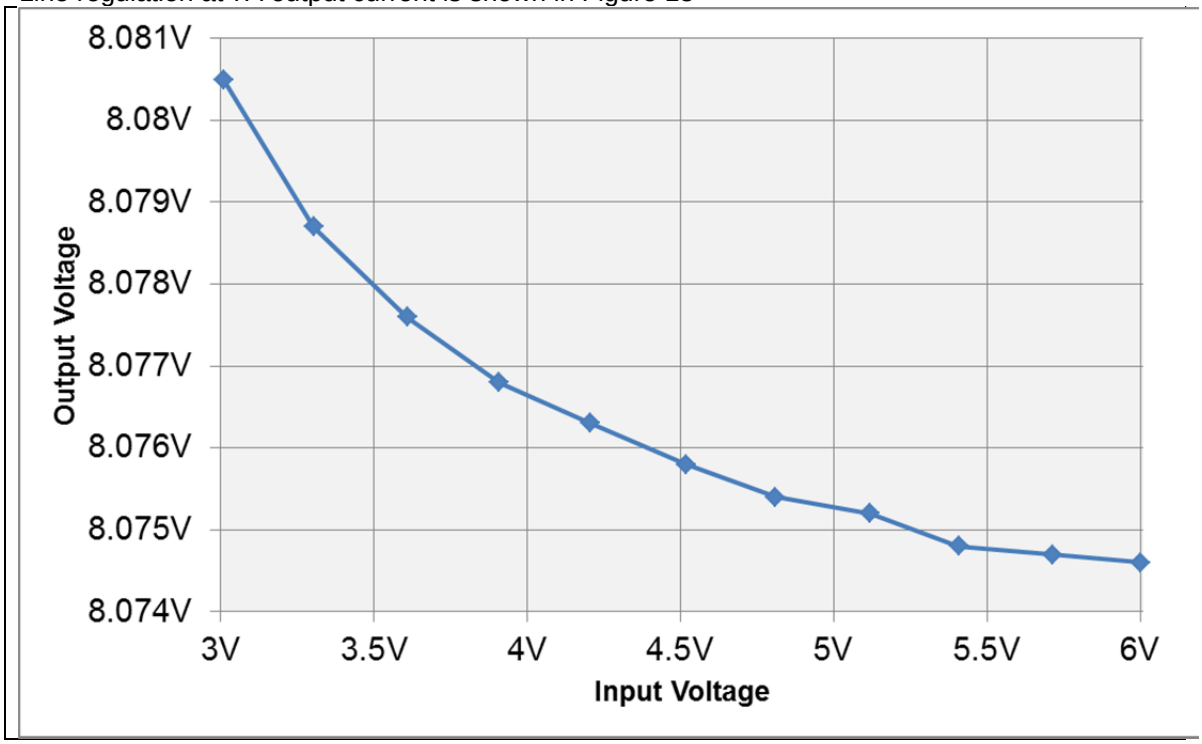


Figure 13

With the same measurement the full load efficiencies across input voltage were calculated

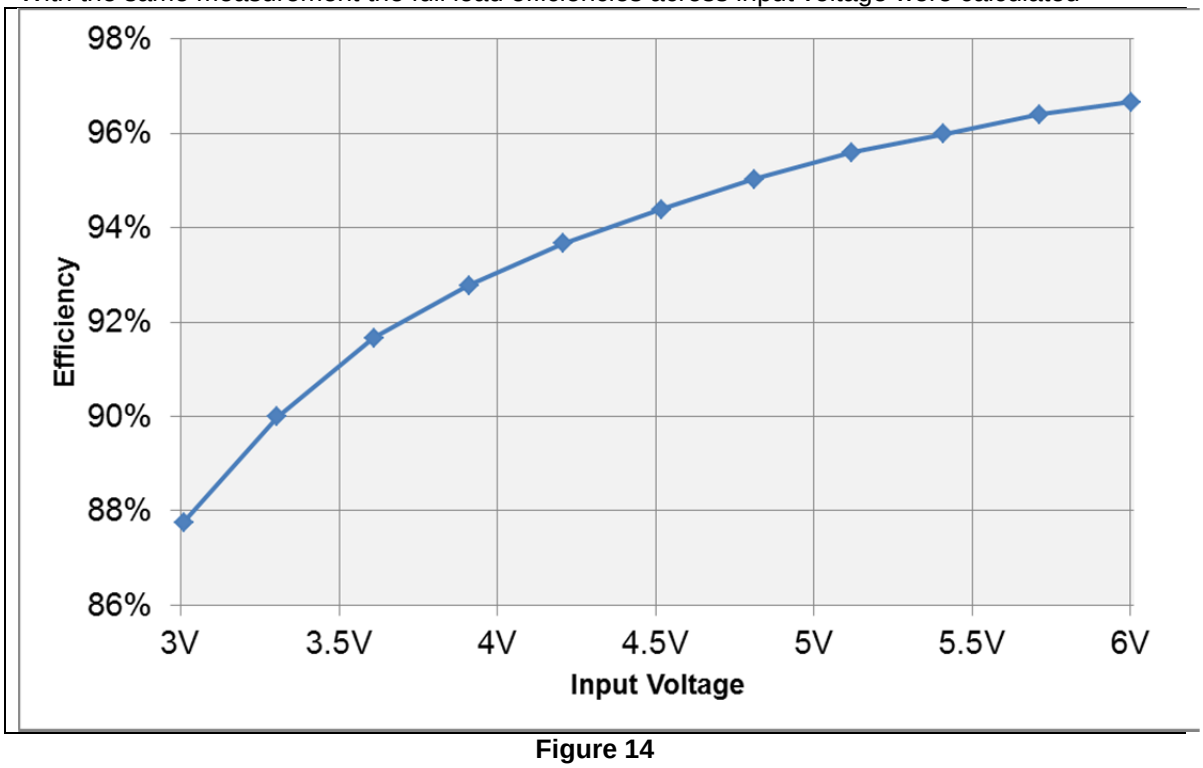
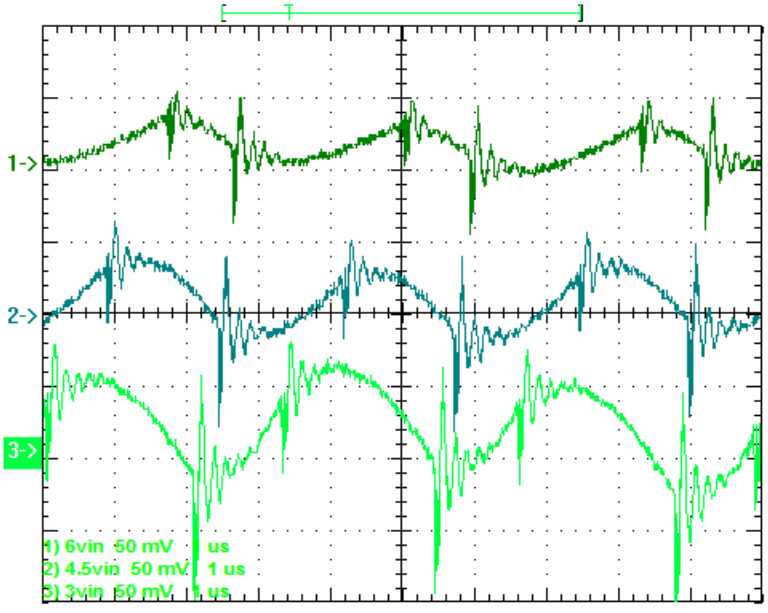


Figure 14

6 Ripple Voltage

6.1 Output

The output ripple voltage is shown in Figure 15. The image was taken with a 7A load and 3V, 4.5V and 6V at the input.



Ch1 => output voltage @ 6Vin

Ch2 => output voltage @ 4.5Vin

Ch3 => output voltage @ 3Vin

50mV/div

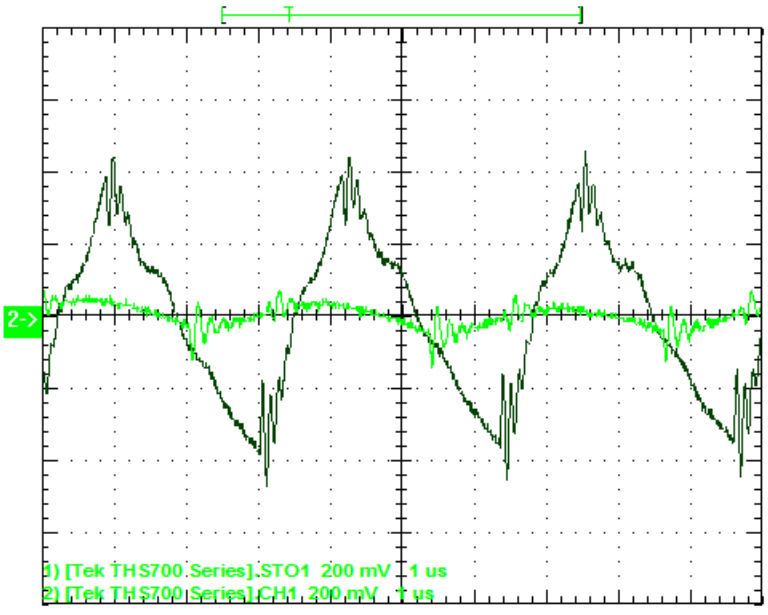
AC coupled

20MHz bandwidth setting

1µs/div

Figure 15

The output ripple voltage before filtering at L2 is shown in Figure 16. The image was taken with a 7A load 3V at the input.



Ch1 => output voltage (C6)

Ch2 => output voltage (C7)

200mV/div

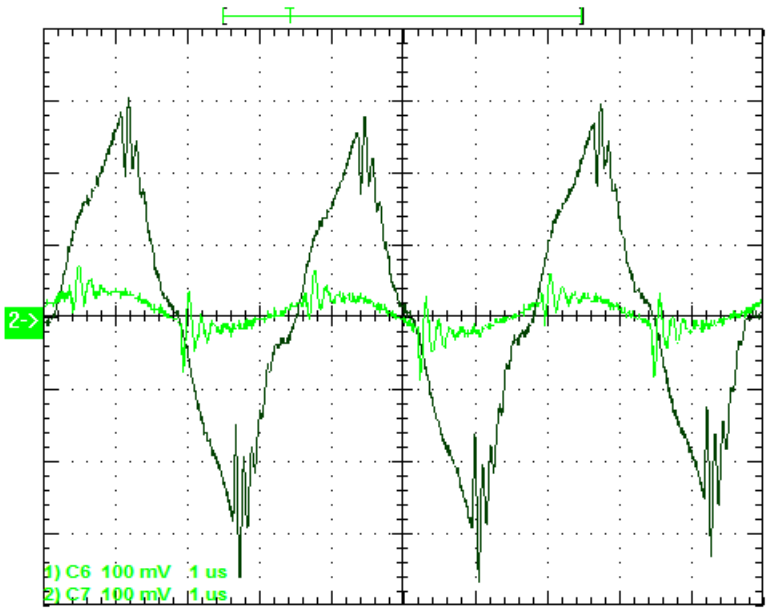
AC coupled

20MHz bandwidth setting

1µs/div

Figure 16

The output ripple voltage before filtering at L2 is shown in Figure 17. The image was taken with a 7A load 4.5V at the input.



Ch1 => output voltage (C6)

Ch2 => output voltage (C7)

100mV/div

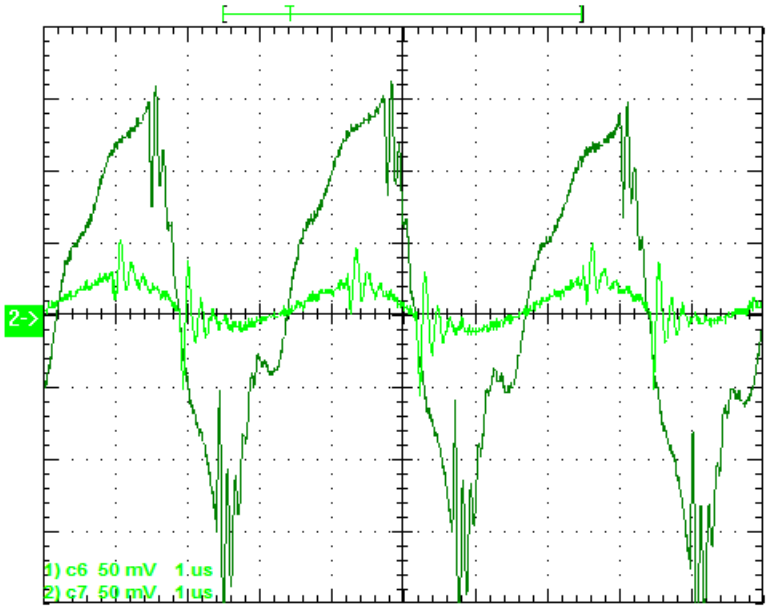
AC coupled

20MHz bandwidth setting

1µs/div

Figure 17

The output ripple voltage before filtering at L2 is shown in Figure 18. The image was taken with a 7A load 6V at the input.



Ch1 => output voltage (C6)

Ch2 => output voltage (C7)

50mV/div

AC coupled

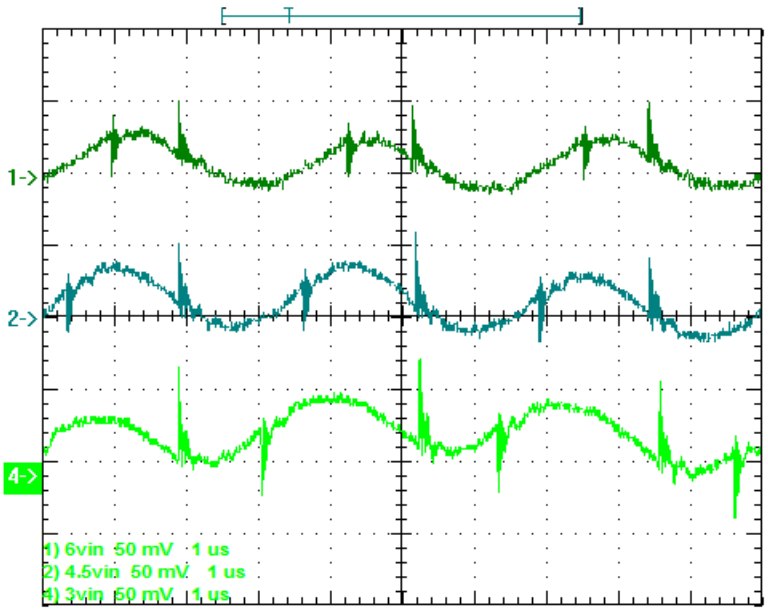
20MHz bandwidth setting

1µs/div

Figure 18

6.2 Input

The input ripple voltage is shown in Figure 19. The image was taken with a 7A load 35V at the input.



Ch1 => output voltage @ 6Vin

Ch2 => output voltage @ 4.5Vin

Ch4 => output voltage @ 3Vin

50mV/div

AC coupled

20MHz bandwidth setting

1µs/div

Figure 19

7 Control Loop Frequency Response

Figure 20 shows the loop response with 7A load and 3V input.

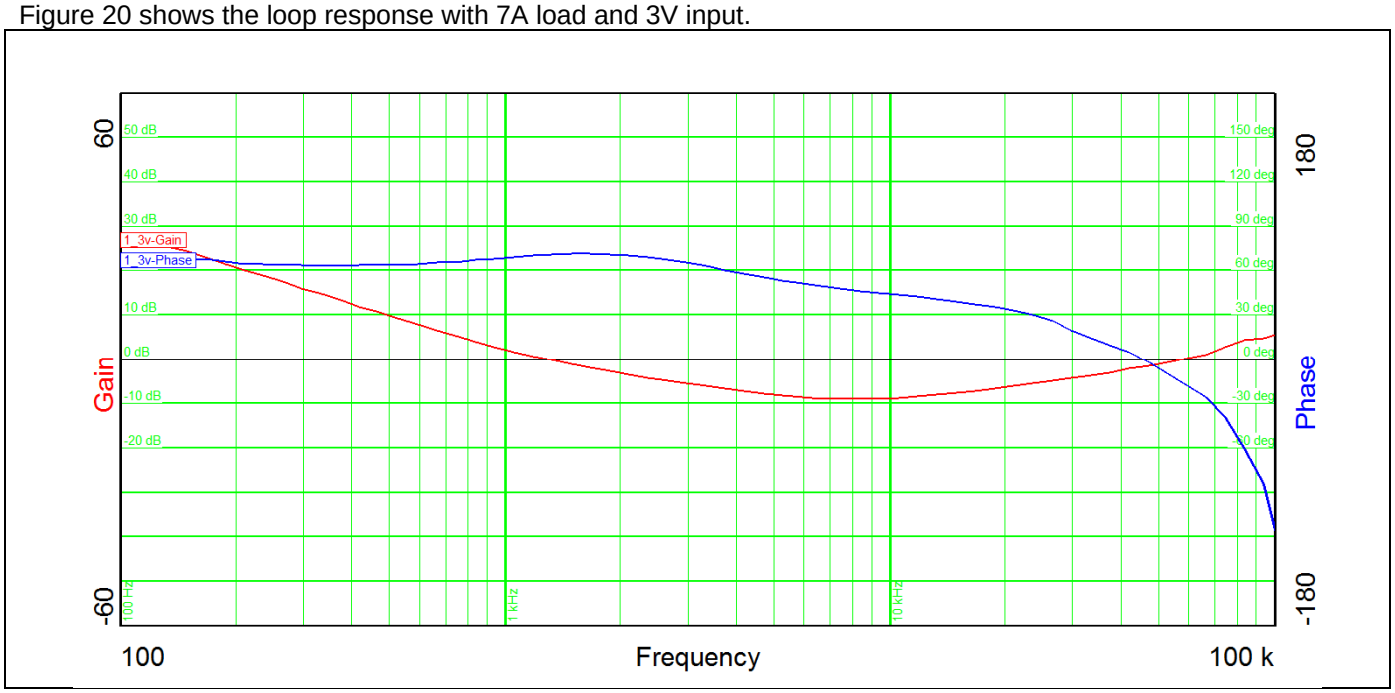


Figure 20

Figure 21 shows the loop response with 7A load and 4.5V input.

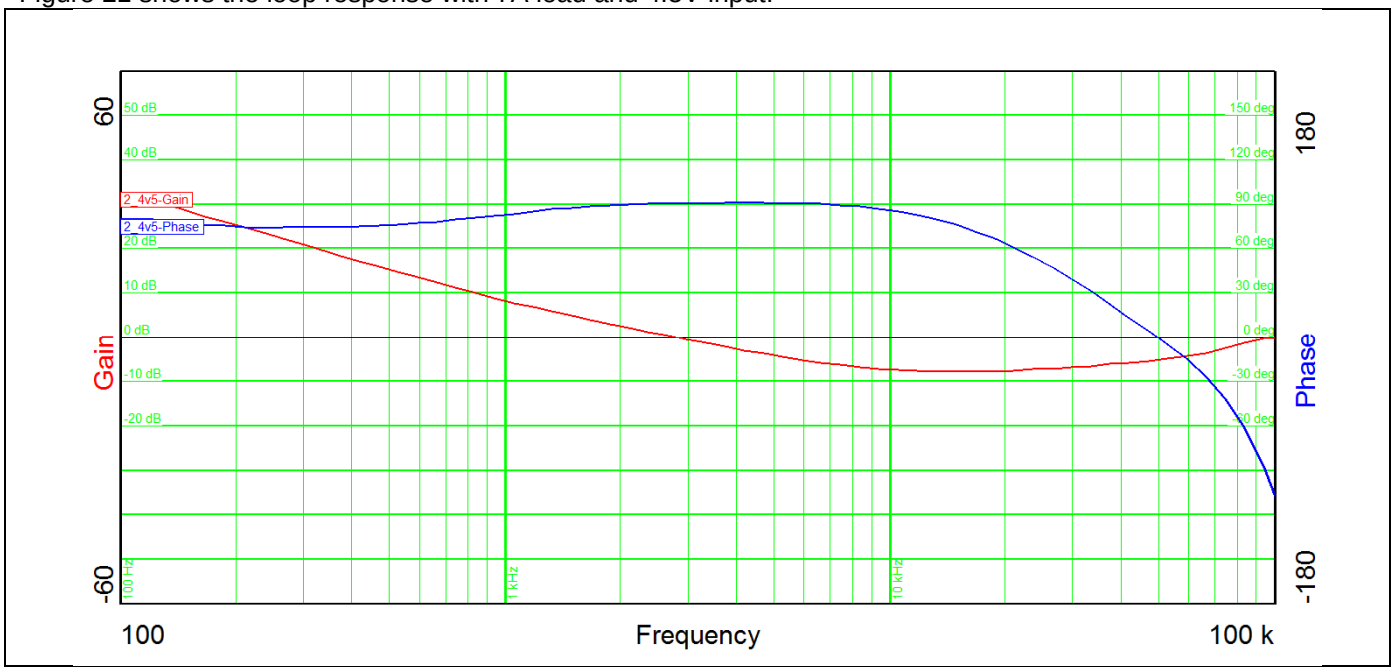


Figure 21

Figure 22 shows the loop response with 7A load and 6V input.

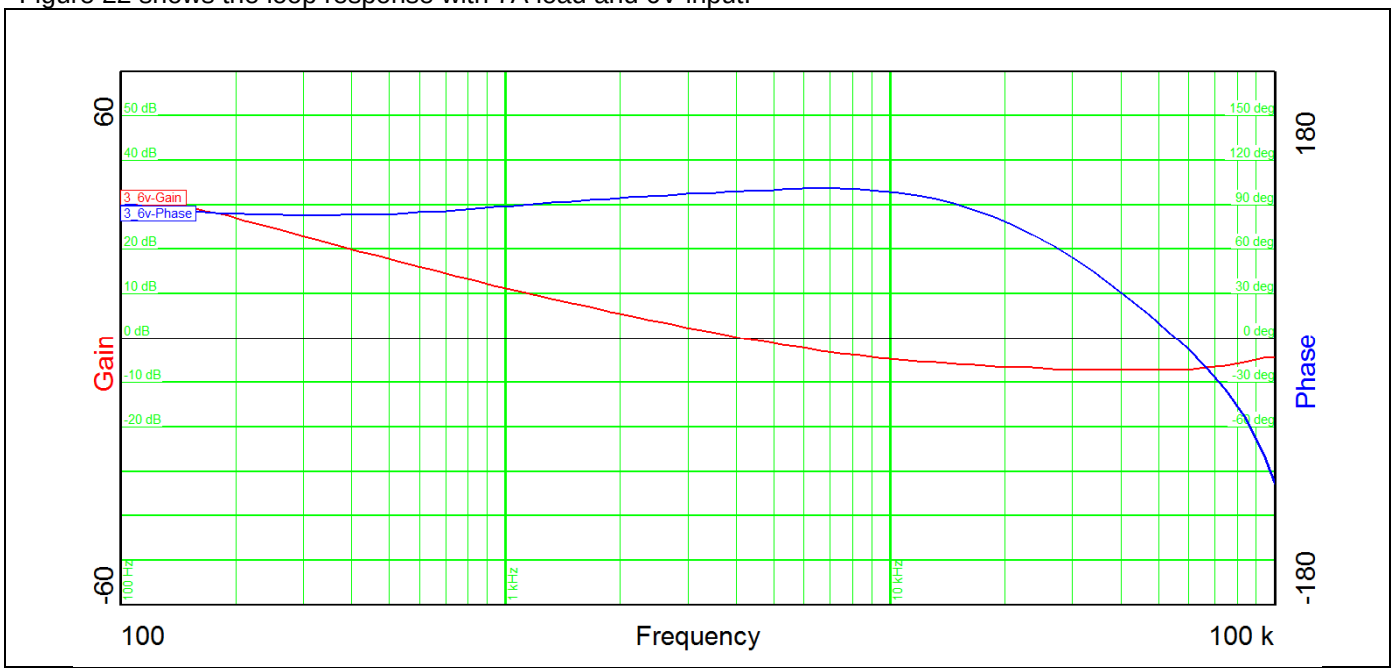


Figure 22

Table 1 summarizes the results

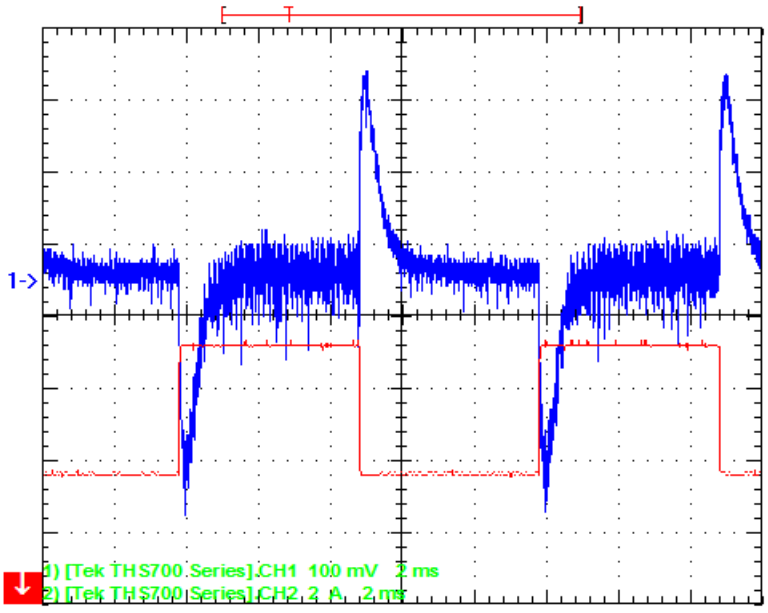
	3V	4.5V	6V
Bandwidth (kHz)	1.29	2.79	4.2
Phasemargin	71°	90°	99°
slope (20dB/decade)	-0.96	-0.87	-0.808
gain margin (dB)	-1.76	-5.29	-7.2
slope (20dB/decade)	+0.617	+0.486	+0.2
freq (kHz)	45.5	49.6	55

Table 1

Loop bandwidth drops by input voltage – see transient response:

8 Load Transients

The Figure 23 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to **3.2V – the deviation is 3%**



Ch1 => output voltage 100mV/div

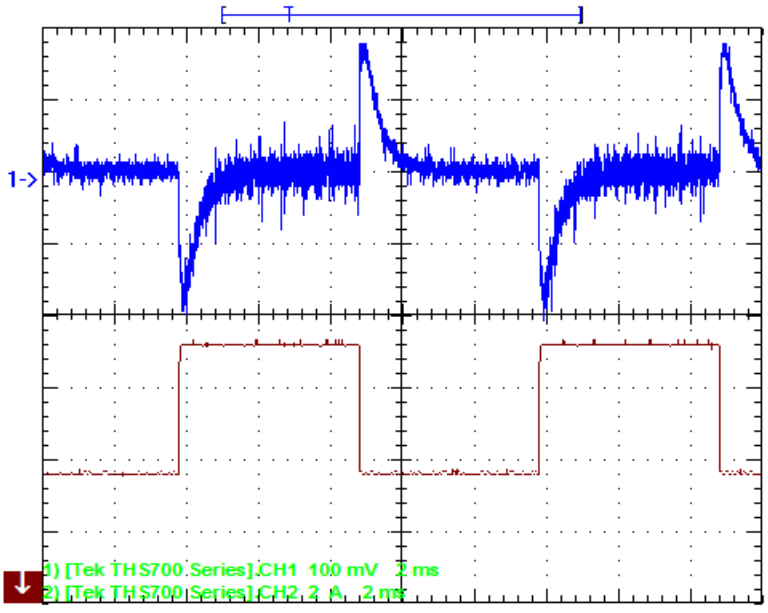
20MHz bandwidth setting

Ch2 => output current 2A/div

2ms/div

Figure 23

The Figure 24 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 4.5V – the deviation is below 3%



Ch1 => output voltage 100mV/div

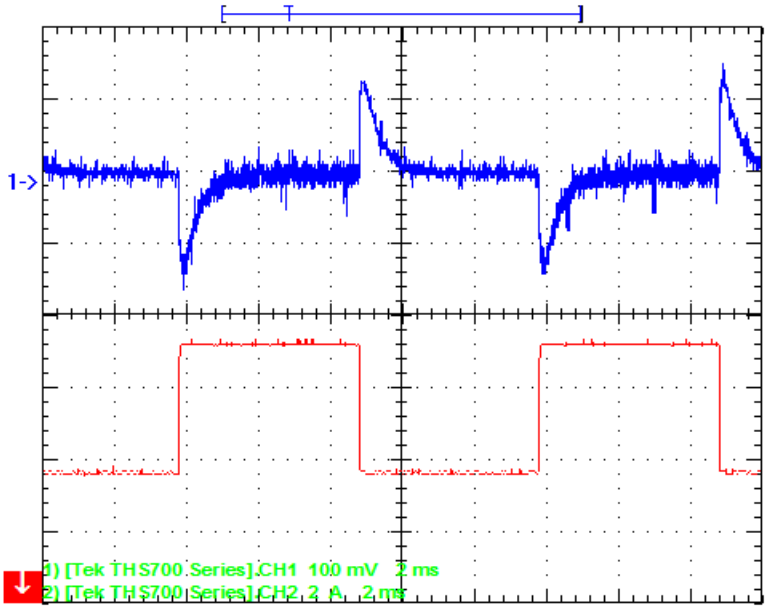
20MHz bandwidth setting

Ch2 => output current 2A/div

2ms/div

Figure 24

The Figure 25 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 6V



Ch1 => output voltage 100mV/div

20MHz bandwidth setting

Ch2 => output current 2A/div

2ms/div

Figure 25

9 Miscellaneous Waveforms

9.1 3V Input

9.1.1 Switch node (Low Side FET)

With input voltage set to 3V and 7A Iout results in the waveform shown in Figure 26

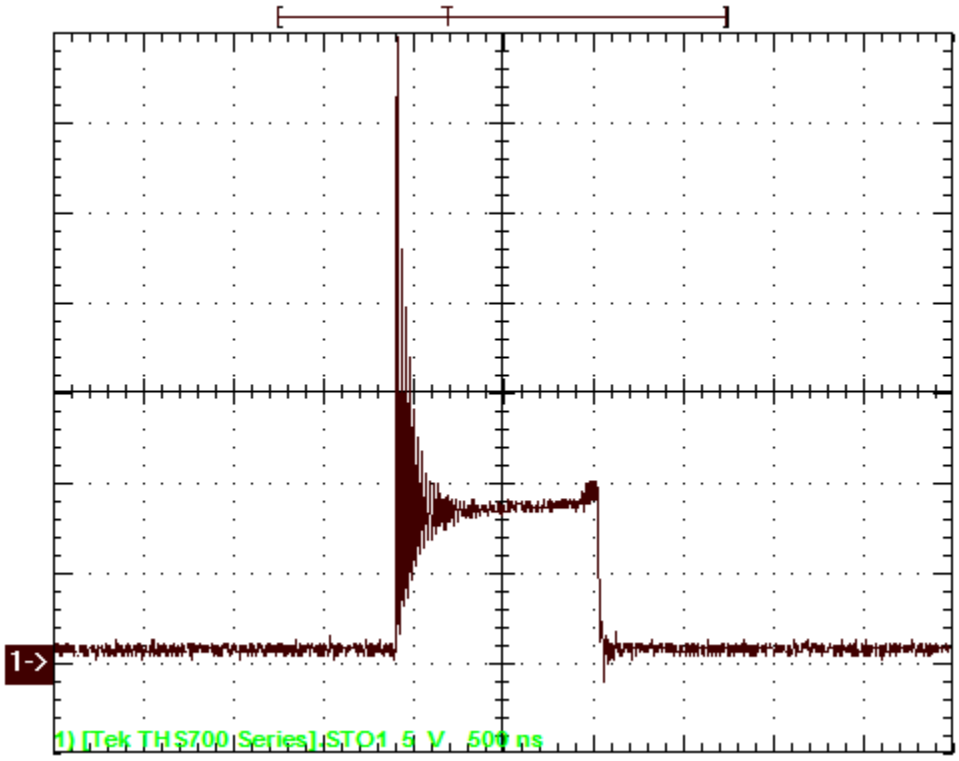
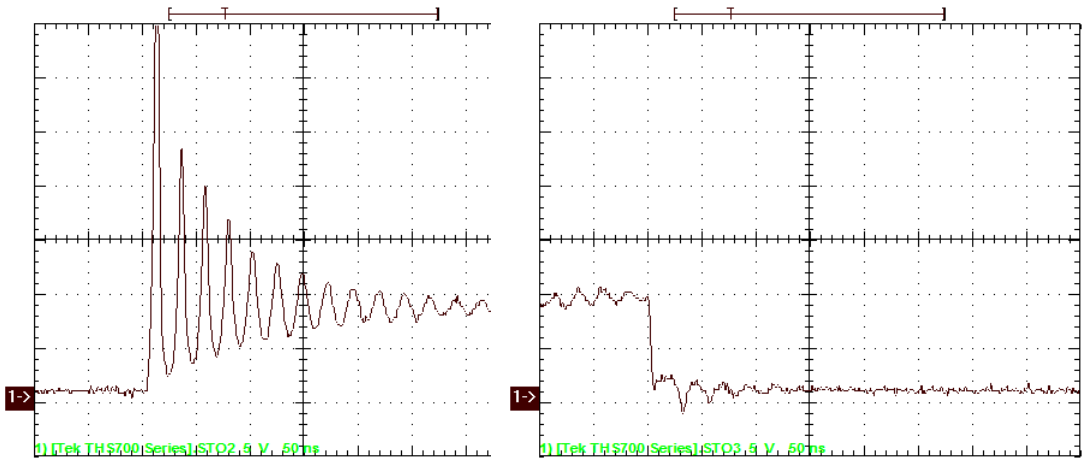
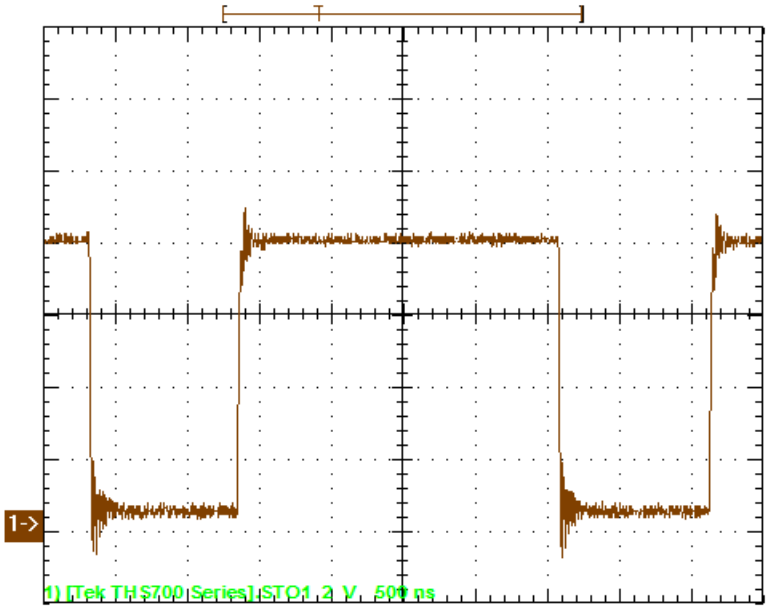
	Ch1 => 5V/div 500ns/div
	Ch1 => 5V/div 50ns/div

Figure 26

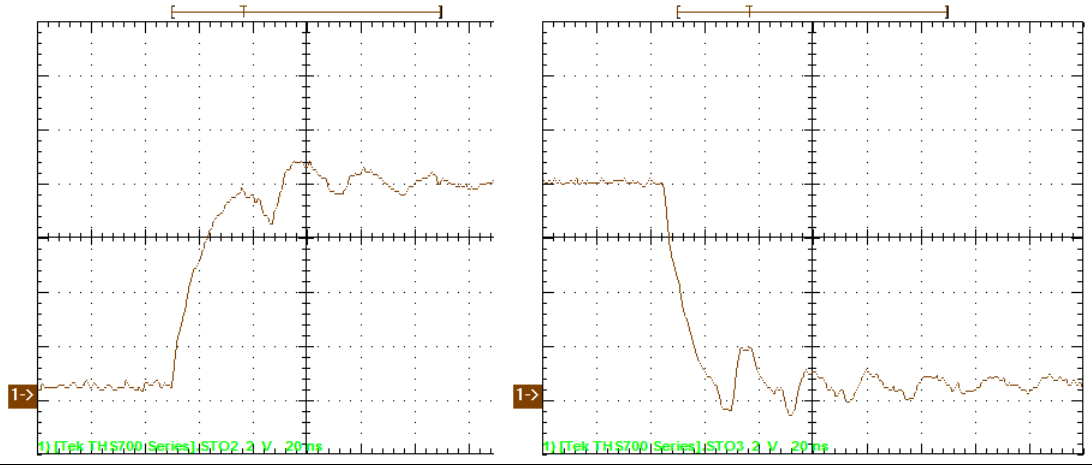
9.1.2 Gate of Low side MOS-FET

With input voltage set to 3V and 7A Iout results in the waveform shown in Figure 27.



Ch1 =>
2V/div

500ns/div

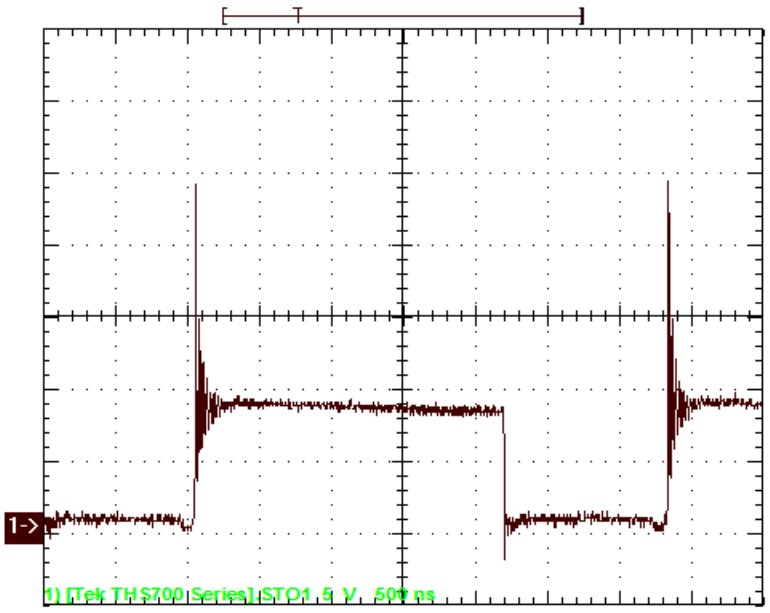


Ch1 =>
2V/div
20ns/div

Figure 27

9.1.3 Hi Side MOS FET

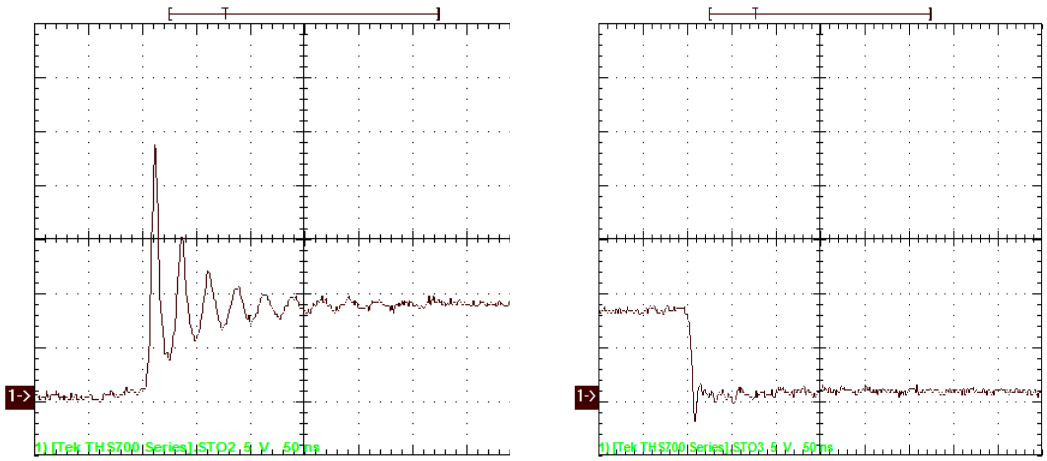
The waveform is shown in **Figure 28**.(the same setup as above)



Ch1 =>
5V/div

500ns/div

full bandwidth

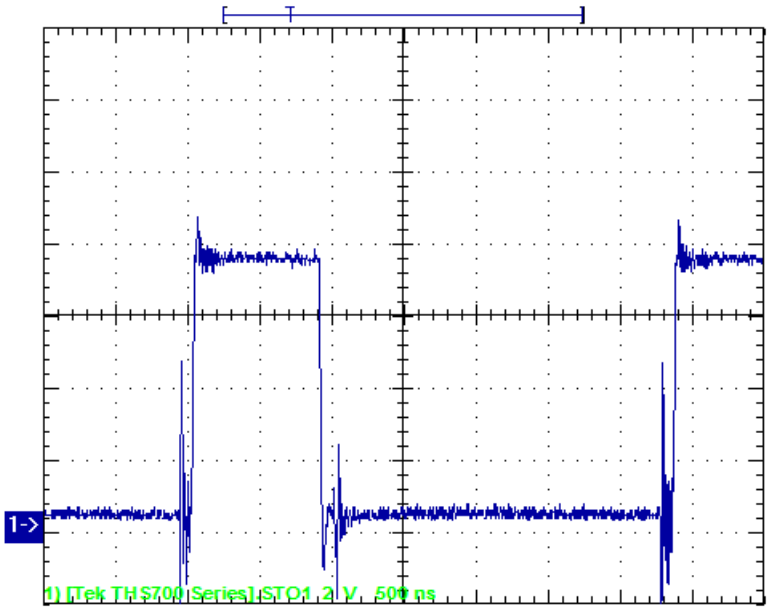


Ch1=>5V/div
50ns/div

Figure 28

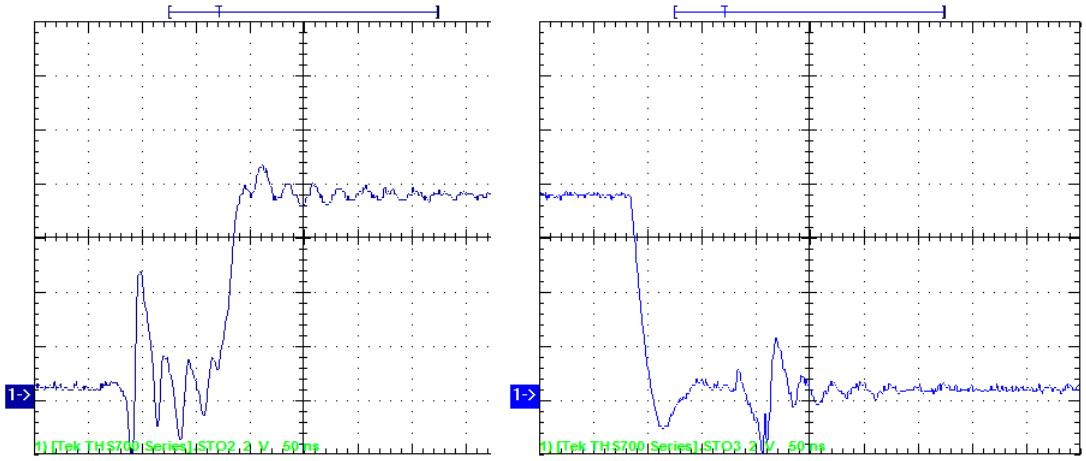
9.1.4 Hi Side MOS FET Gate

With input voltage set to 3V and 7A Iout results in the waveform shown in Figure 29.



Ch1 =>
2V/div

500ns/div



Ch1 =>
2V/div
50ns/div

Figure 29

9.2 4.5V Input

9.2.1 Switch node (Low Side FET)

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 30

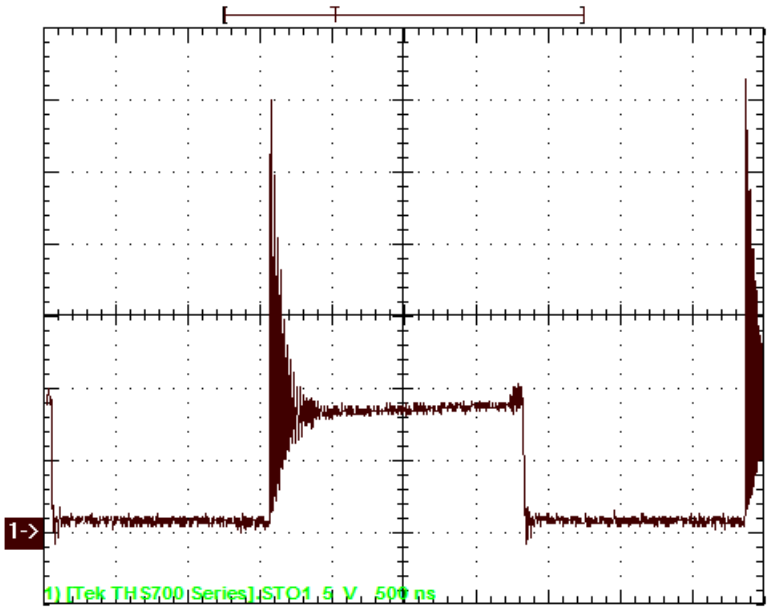
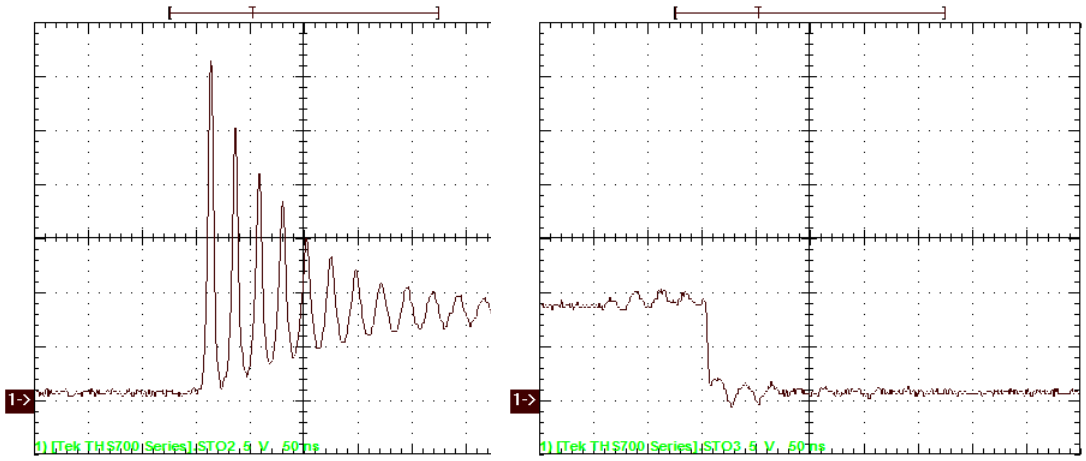
	Ch1 => 5V/div 500ns/div
	Ch1 => 5V/div 50ns/div

Figure 30

9.2.2 Gate of Low side MOS-FET

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 31.

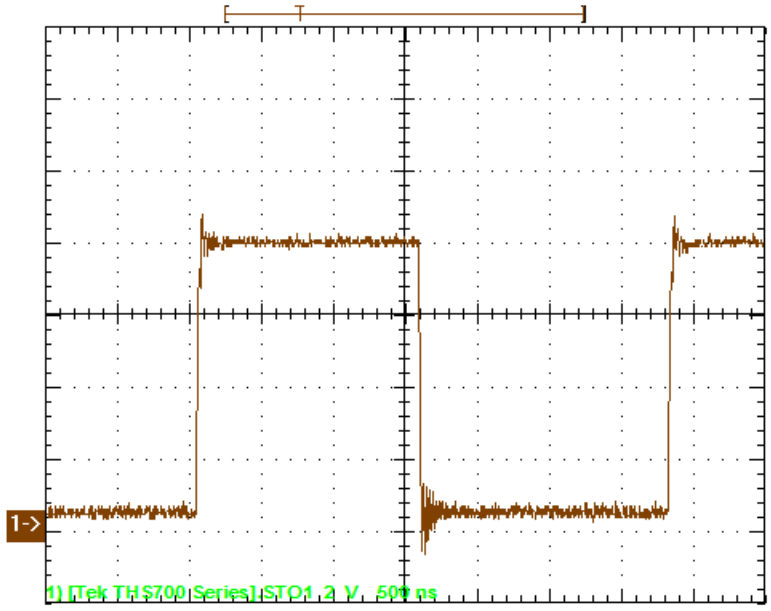
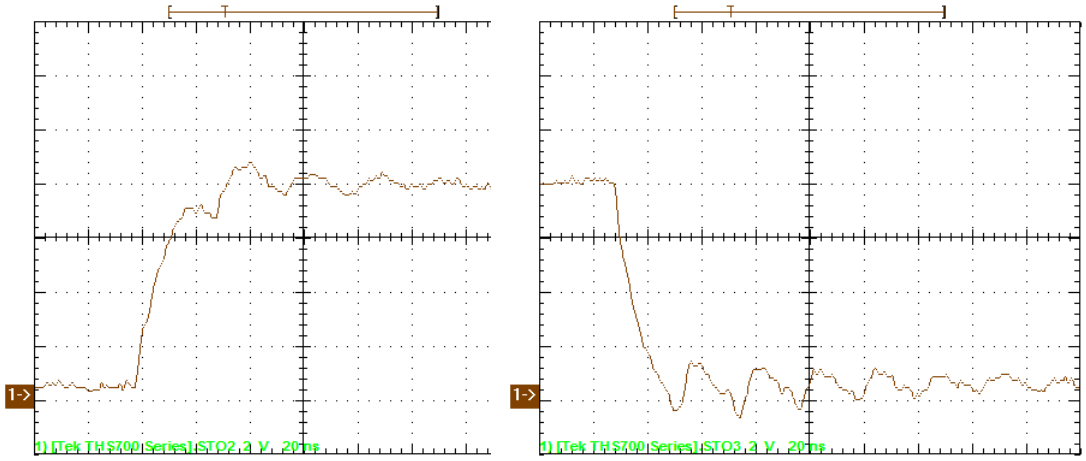
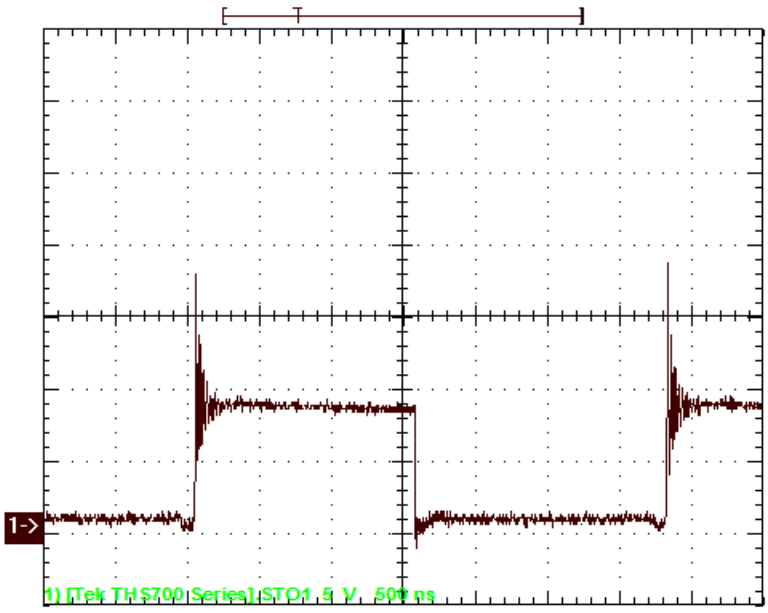
	Ch1 => 2V/div 500ns/div
	Ch1 => 2V/div 20ns/div

Figure 31

9.2.3 Hi Side MOS FET

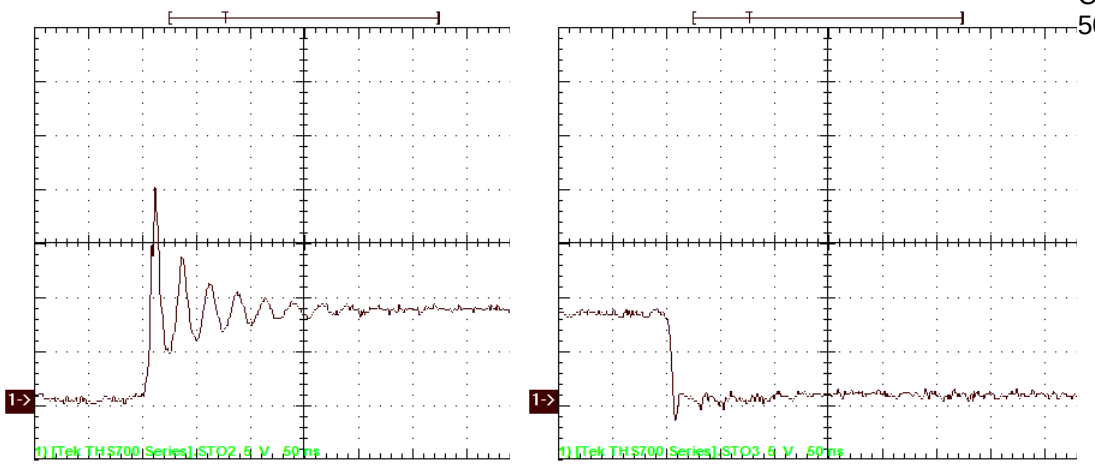
The waveform is shown in **Figure 32**.(the same setup as above)



Ch1 =>
5V/div

500ns/div

full bandwidth



Ch1=>5V/div
50ns/div

Figure 32

9.2.4 Hi Side MOS FET Gate

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 33.

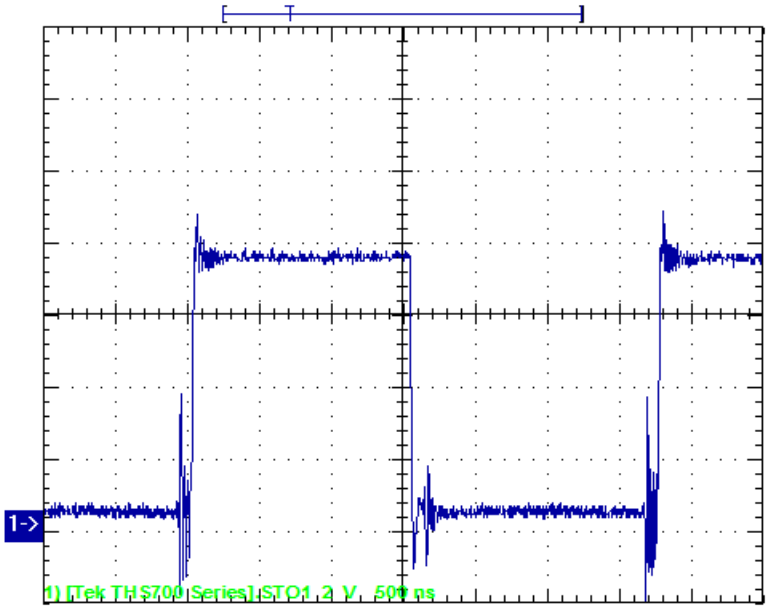
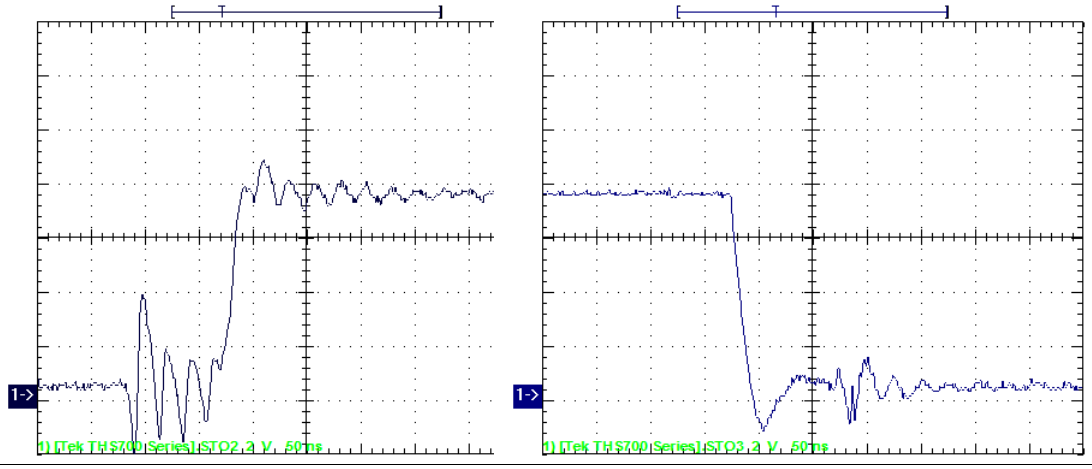
	Ch1 => 2V/div 500ns/div
	Ch1 => 2V/div 50ns/div

Figure 33

9.3 6V Input

9.3.1 Switch node (Low Side FET)

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 34

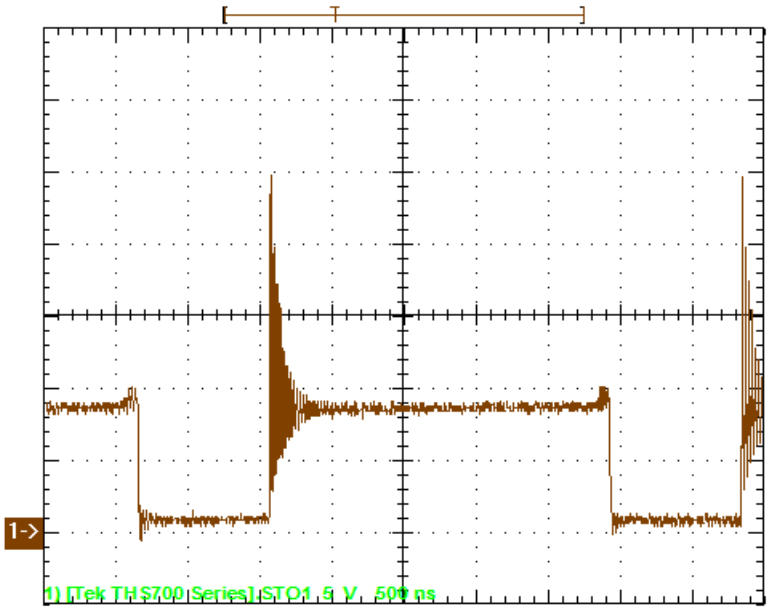
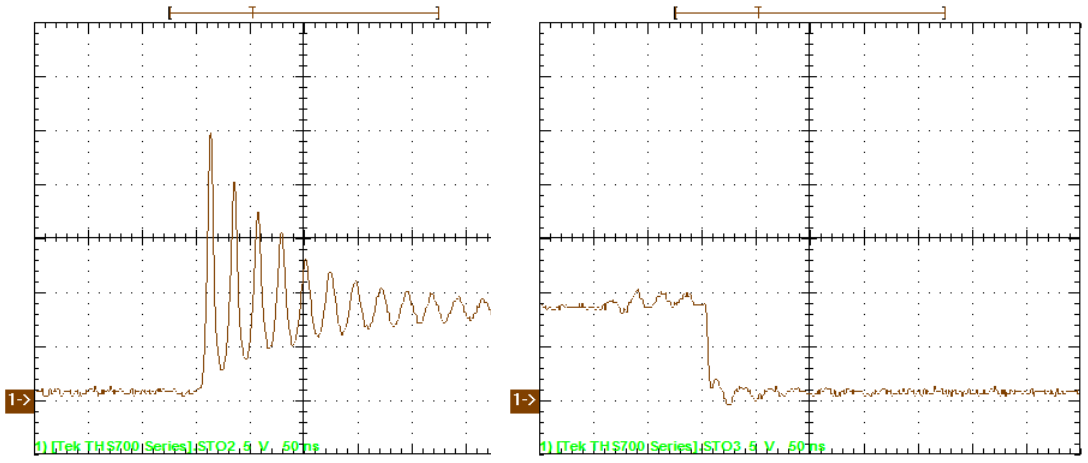
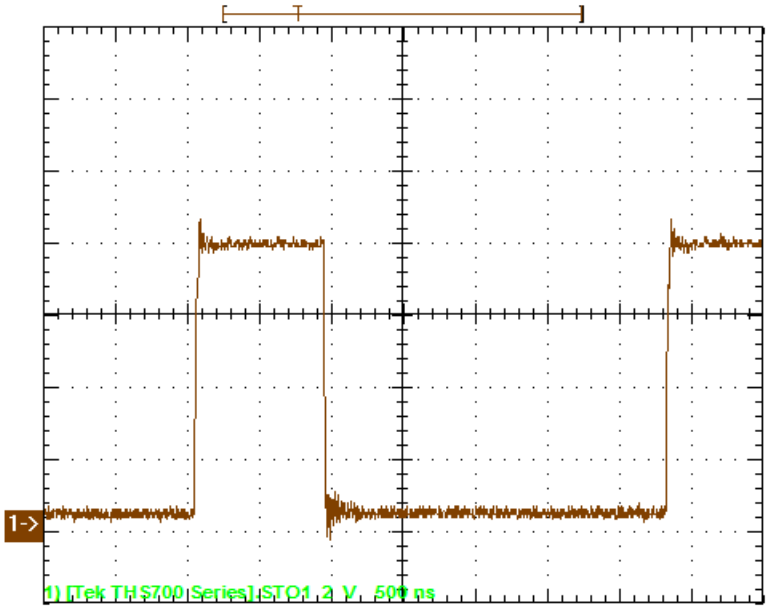
	Ch1 => 5V/div 500ns/div
	Ch1 => 5V/div 50ns/div

Figure 34

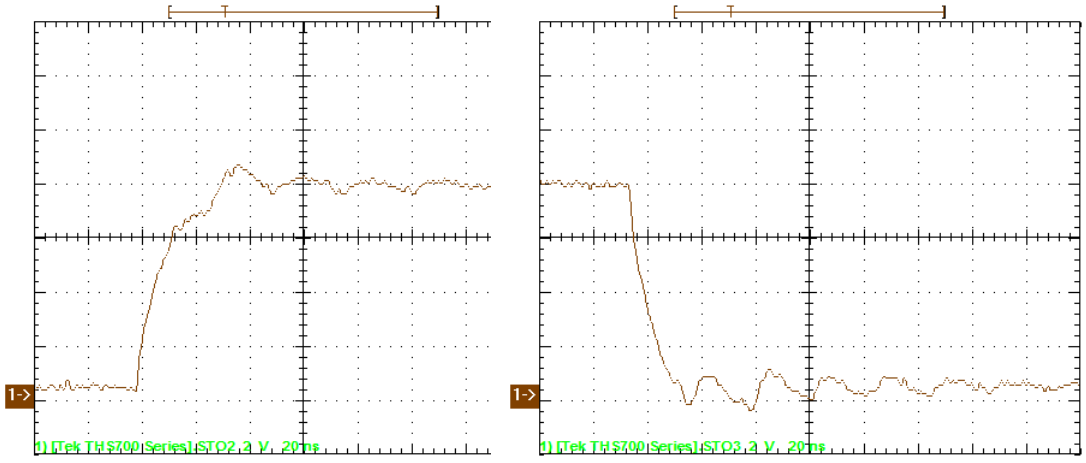
9.3.2 Gate of Low side MOS-FET

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 35.



Ch1 =>
2V/div

500ns/div

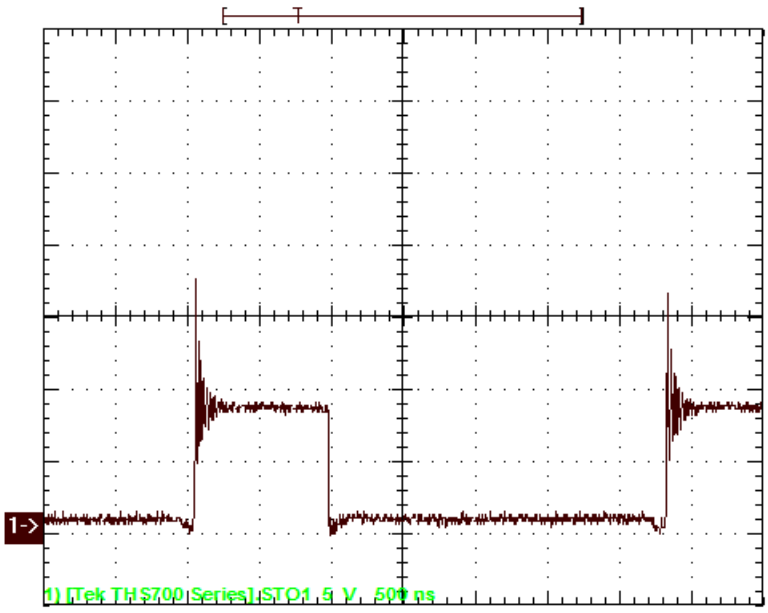


Ch1 =>
2V/div
20ns/div

Figure 35

9.3.3 Hi Side MOS FET

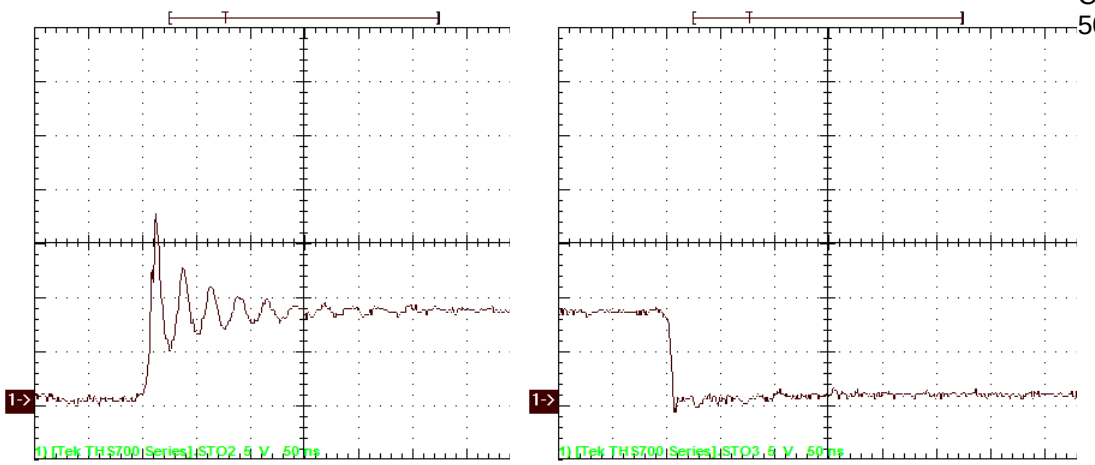
The waveform is shown in **Figure 36** (the same setup as above)



Ch1 =>
5V/div

500ns/div

full bandwidth



Ch1=>5V/div
50ns/div

Figure 36

9.3.4 Hi Side MOS FET Gate

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 37.

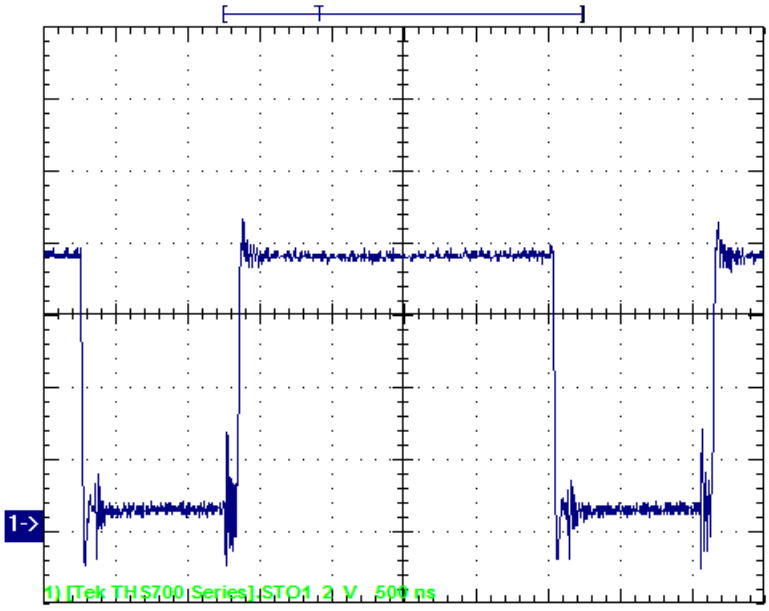
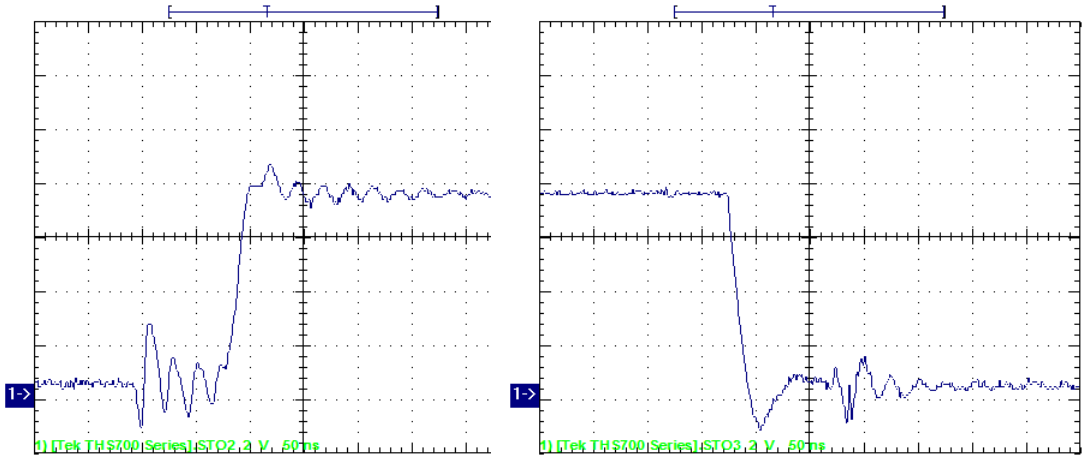
	Ch1 => 2V/div 500ns/div
	Ch1 => 2V/div 50ns/div

Figure 37

10 Thermal Image

Figure 38 shows the thermal image at 6V input and 7A output (no additional airflow)

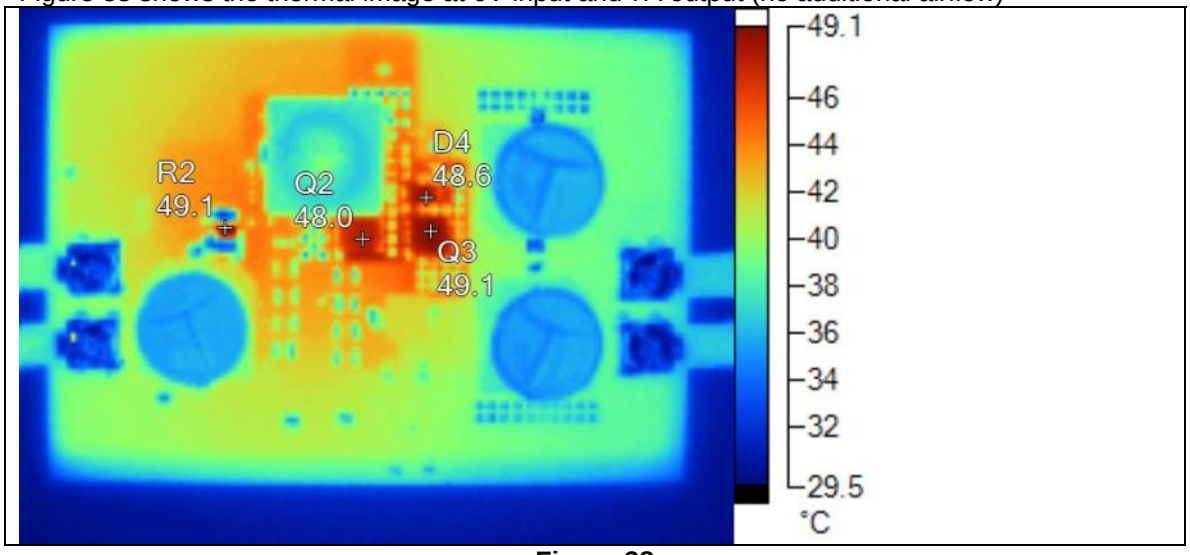


Figure 38

Name	Temperature
R2	49.1°C
Q2	48.0°C
Q3	49.1°C
D4	48.6°C

Table 2

Figure 39 shows the thermal image at 4.5V input and 7A output (no additional airflow)

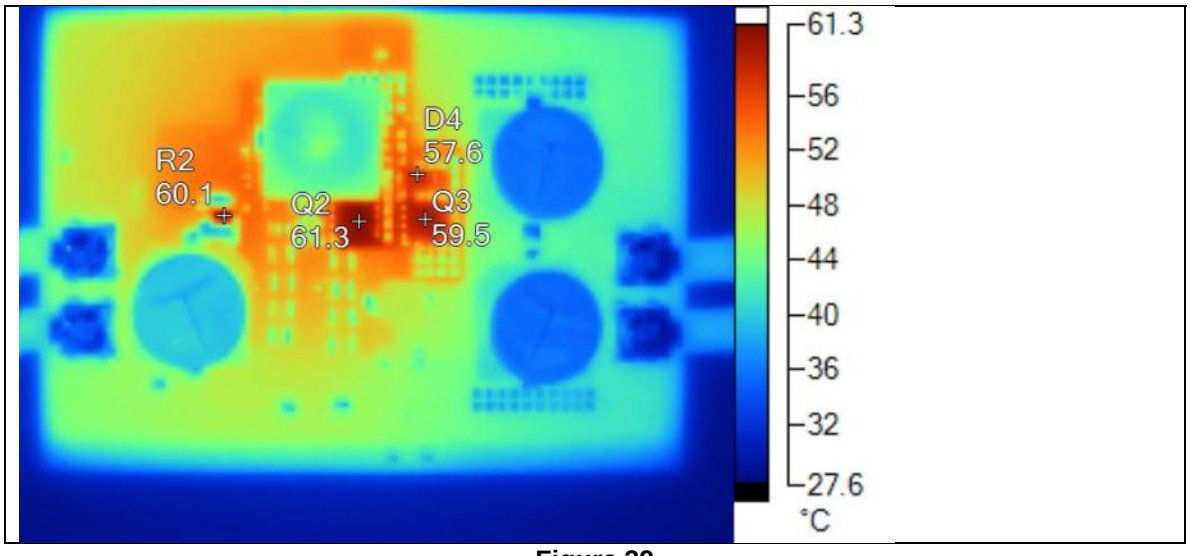


Figure 39

Name	Temperature
Q2	61.3°C
Q3	59.5°C
D4	57.6°C
R2	60.1°C

Table 3

Figure 40 shows the thermal image at 3V input and 7A output (no additional airflow)

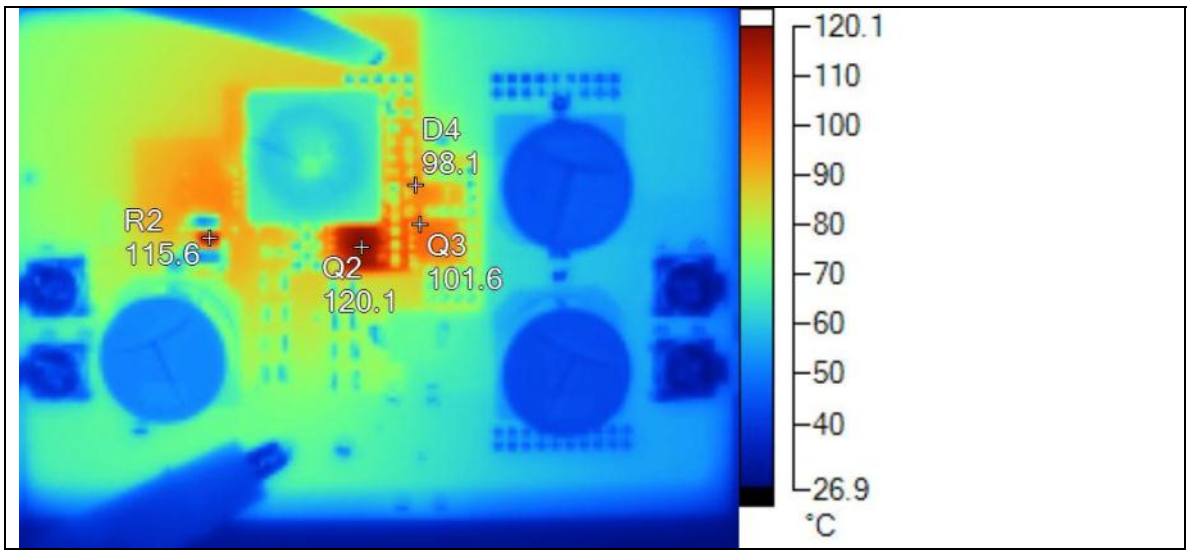


Figure 40

Name	Temperature
Q2	120.1°C
R2	115.6°C
Q3	101.6°C
D4	98.1°C

Table 4

Figure 40 shows the thermal image at 3V input and 7A output (with additional airflow)

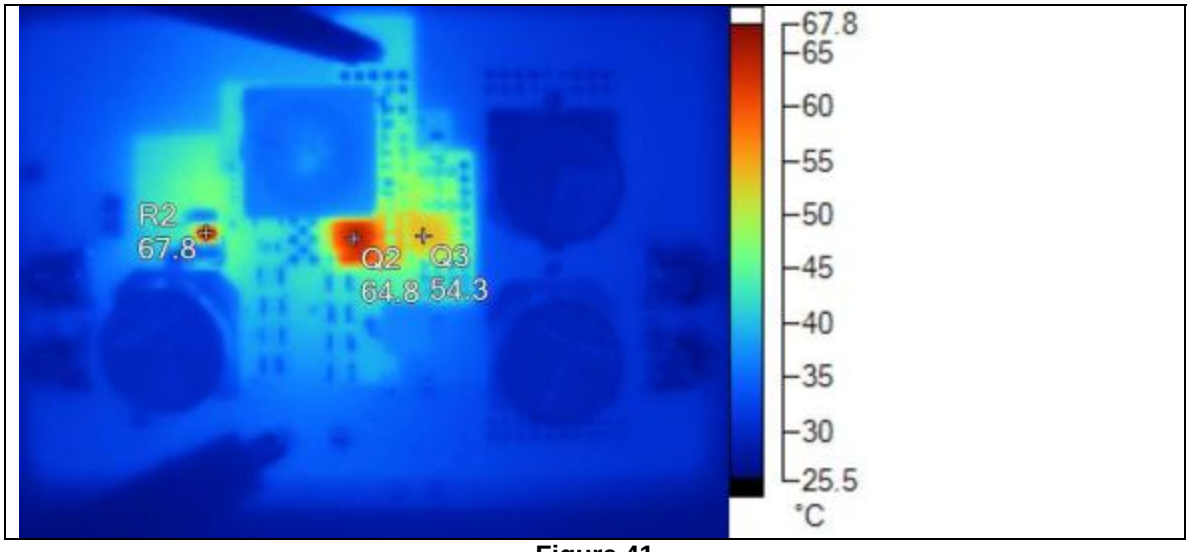


Figure 41

Name	Temperature
R2	67.8°C
Q2	64.8°C
Q3	54.3°C

Table 5

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265