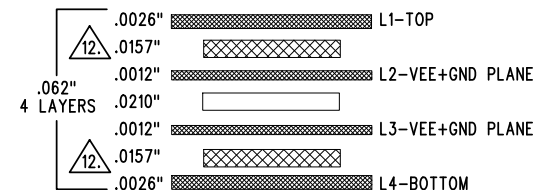


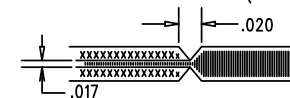
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	1	REBUILD WITH CHANGE	DILIAN R.	01-30-15

## LAYER STRUCTURE

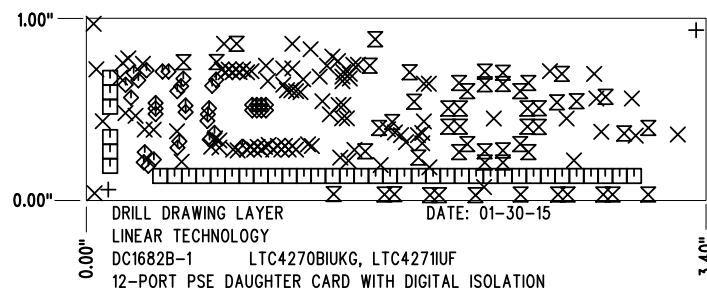


## NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.  
-FINISHED THICKNESS TO BE 0.062" +/- .005"  
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



SHOWN FROM TOP SIDE



SIZE	QTY	SYM	PLATED	TOL
0.07	2	+	NO	+/-0.003"
0.008	101	X	YES	+/-0.003"
0.035	40	□	YES	+/-0.003"
0.01	37	◇	YES	+/-0.003"
0.015	53	⊗	YES	+/-0.003"

UNLESS OTHERWISE SPECIFIED		APPROVALS			
DIMENSIONS ARE IN INCHES		PCB DES.	KIM T.		
TOLERANCES:		APP ENG.	DILIAN R.	TITLE: FABRICATION DRAWING	
0.XX" = ±0.01"				12-PORT PSE DAUGHTER CARD	
0.XXX" = ±0.005"				WITH DIGITAL ISOLATION	
INTERPRET DIM AND TOL				SIZE	IC NO. LTC4270BIUKG, LTC4271IUF
PER ASME Y14.5M-1994				N/A	DEMO CIRCUIT 1682B
THIRD ANGLE PROJECTION				REV	1
		SCALE = NONE	FILENAME: DC1682B-1.PCB	SHT 1 OF 1	

1630 MCCARTHY BLVD  
MILPITAS, CA 95035  
PH: (408)432-1900  
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