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Capacitor-Based Backup Power Supply for PLC Modules

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Design Resources

TIDA-00500	Design Folder
LM5001	Product Folder
LM5069	Product Folder
TPS7A4101	Product Folder
LM334	Product Folder
LMV331-N	Product Folder
OPA348	Product Folder

ASK Our E2E Experts
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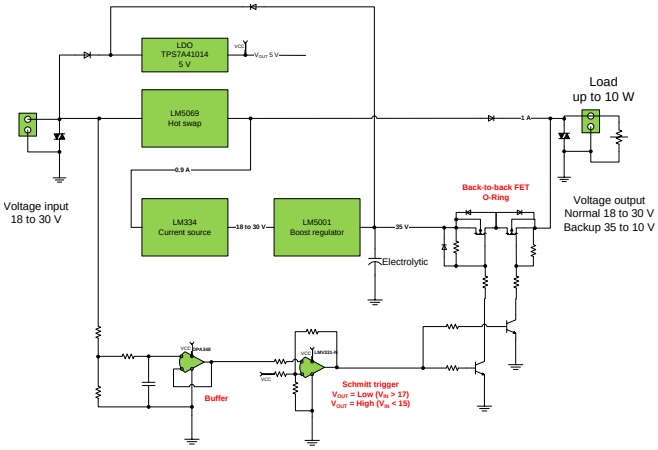
Design Features

- Backup Energy up to 6 Joules (J)
- Inrush Current Protection With Auto Retry
- Capacitor Charging Time Less Than 0.5 s
- Lower BOM Cost

Featured Applications

- PLC, DCS and PAC:
  - Backup Supply
  - I/O Module
  - CPU (PLC)



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1 Key System Specifications

Table 1. Key System Specifications

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage	Normal operation	18	24	30	V
I_Q	Quiescent current	No output load	—	—	40	mA
V_{J5}	Output voltage connector J5	Normal operation	18	24	30	V
V_{J5}	Output voltage connector J5	Backup operation	11	—	35	V
E	Stored energy		—	5	6	J
T_C	Charge time	V_{IN} = 18 V			0.45	S
T_D	Backup time	Power load = 5 W	—	—	1	S
		Power load = 10 W	—	—	0.5	S

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2 System Description

A programmable logic controller (PLC) is the heart of an automation line. PLC units are designed with multiple types of cards. PLCs need to analyze in real time, log data fields, and take corrective action by controlling any actuators.

PLC reliability is highly dependent on its power source. Factory process may demand the PLC to perform minimum functions after a complete power loss. In such an event, the PLC needs to perform quick data logging and latching of I/Os to safety state until power returns. Therefore, the PLC needs to be equipped with a backup power source to remain functional during a power loss.

The TIDA-00500 provides power to load for a short time after a power interrupt. Traditionally, PLCs are equipped with a recharge battery source for alternative power. This battery source often suffers from drawbacks like complex charging topologies, charging time, periodic maintenance, and eco-hazards. In scenarios where PLCs need to be functional for a short time after a power interrupt, a capacitor-based backup is a much simpler and more effective approach because of the higher power density in comparison to a standard battery-based solution.

Figure 1 emphasizes the power tree in a PLC unit.

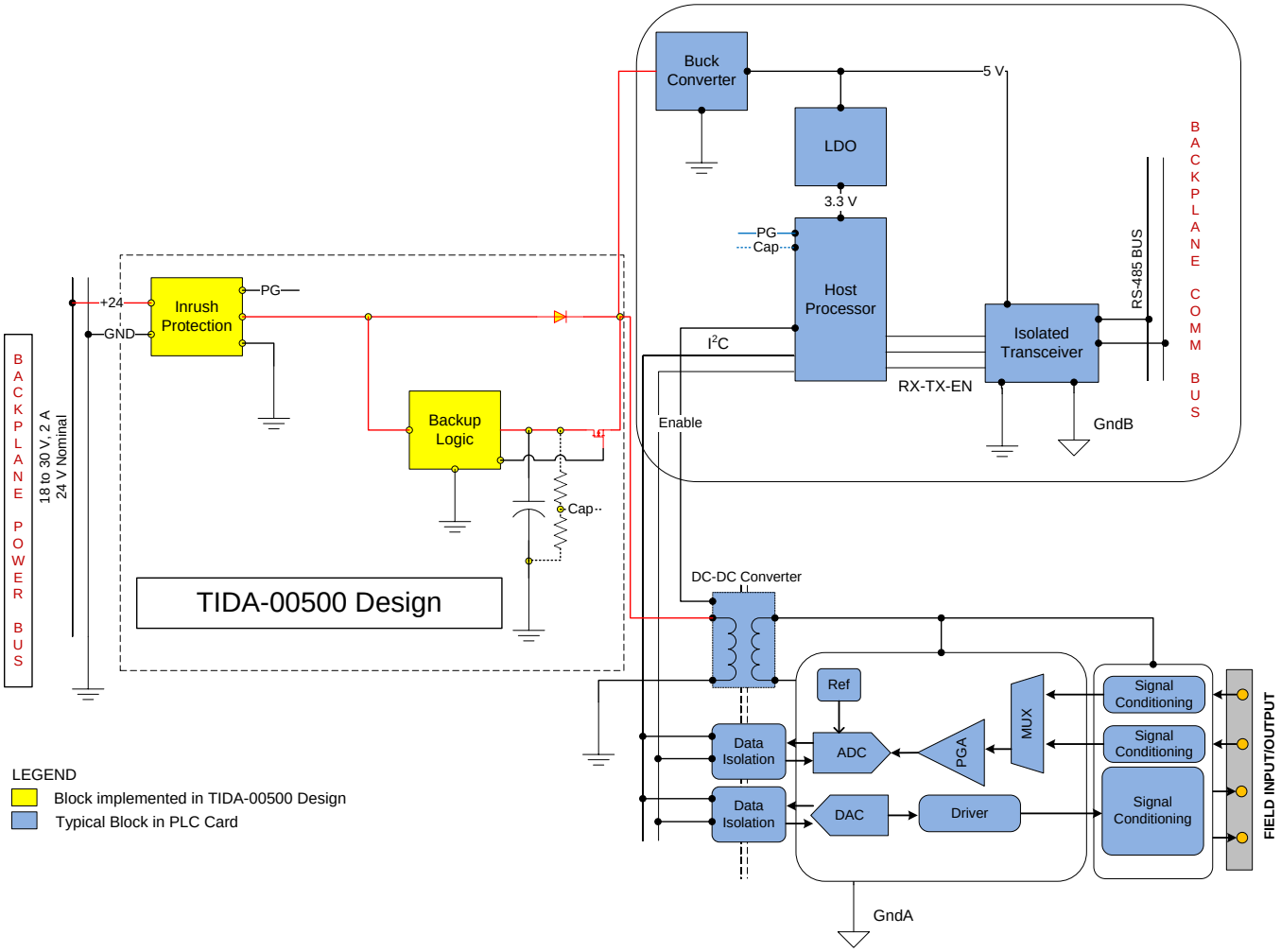

Figure 1. Generic Illustration of Power Block

As most PLCs are limited to a supply current up to 2 A, the charging network can sink only a difference of the source and load current (1 A). Also, the charging network should not affect the startup time.

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As shown in Figure 2, charging the network consists of an LM334-controlled current source and an LM5001 boost converter. The LM334 is an adjustable current source that can be programmed to set a current for charging the storage capacitor without affecting the load current. The LM5001 boost increases the input rail up to 36 V, which allows the backup capacitor to hold more energy. As backup voltage is greater than supply voltage, a simple diode O-Ring is not possible. The O-Ring logic is achieved by the inverting Schmitt trigger and P-Channel FET as shown in Figure 2. The inverting Schmitt trigger can be set to trigger at any particular threshold of an input range by just changing the input voltage divider range. The comparator is designed with a 100-mV hysteresis to prevent nuisance change over. This hysteresis window at the input voltage divider will be a multiple of the divider ratio. The LDO is required to provide a 5-V supply for O-Ring logic even in backup mode.

The LM5069 is a hot swap inrush current limiter. If any temporary short fault occurs, the power gets disconnected. The LM5069 also features undervoltage and overvoltage protection. The power good pin of the LM5069 can be monitored for power sequencing and backup mode.

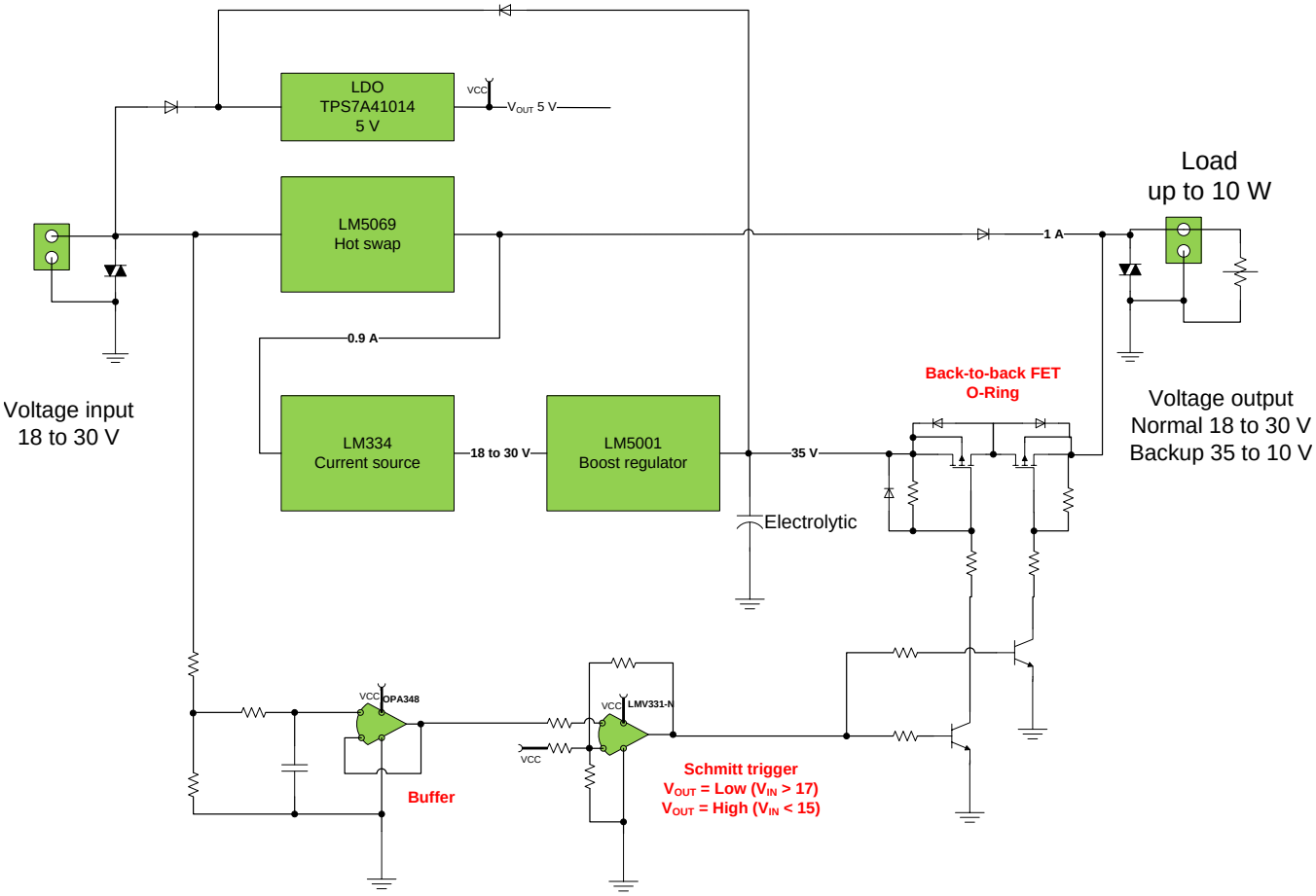

Figure 2. TIDA-00500 Block Diagram

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2.1 Highlighted Products

The TIDA-00500 provides a backup supply for PLC modules. The LM5001 boost charges the capacitor in less than half of second with controlled current. The LMV331 acts as an inverting Schmitt trigger to fast turn on the backup supply without a power delay. The LM5069 protects by limiting inrush current in case of short load, and it features an auto-retry option for system startup after a temporary short fault.

2.1.1 LM5001

The LM5001 high-voltage switch-mode regulator features all of the functions necessary to implement efficient high-voltage boost converters using few external components. This easy-to-use regulator integrates a 75-V N-Channel MOSFET with a 1-A peak current limit. Current mode control provides inherently simple loop compensation and line-voltage feed-forward for superior rejection of input transients. The switching frequency is set with a single resistor and is programmable up to 1.5 MHz. Additional protection features include current limit, thermal shutdown, undervoltage lockout, and remote shutdown capability.

2.1.2 LM5069

The LM5069 positive hot swap controller provides intelligent control of the power supply connections during the insertion and removal of circuit cards from a live system backplane or other "hot" power sources. The LM5069 controls inrush current to limit system voltage droop and transients. The current limit and power dissipation in the external series pass N-Channel MOSFET are programmable, ensuring operation within the safe operating area (SOA). The power good output indicates when the output voltage is within 1.25 V of the input voltage. The input undervoltage and overvoltage lockout levels and hysteresis are programmable as well as the initial insertion delay time and fault detection time.

2.1.3 TPS7A41014

The TPS7A41014 is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8) and is able to withstand continuous DC or transient input voltages of up to 50 V.

The TPS7A41014 is stable with any output capacitance greater than 4.7 µF and any input capacitance greater than 1 µF (over temperature and tolerance). Therefore, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and potentially small output capacitor.

2.1.4 LM334

The LM334 is an adjustable current source featuring 10,000:1 range in operating current, an excellent current regulation, and a wide dynamic voltage range of 1 to 40 V. Current is established with one external resistor, and no other parts are required. The initial current accuracy is ±3%.

The LM334 is a true floating current source with no separate power supply connections. The sense voltage used to establish the operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest external resistor connection then generates a current with a ≈ 0.33%/°C temperature dependence.

2.1.5 LMV331-N

The LMV331 are the most cost-effective solutions for applications where low-voltage operation, low power, and space saving are the primary specifications in circuit design for portable consumer products. It features typical very low propagation delay of 0.2 µs.

2.1.6 OPA338

The OPA338 op-amps provide low bias current, high-speed operation, high open-loop gain, and rail-to-rail output swing. They operate on a single supply with operation as low as 2.5 V while drawing only a 525-µA quiescent current. The OPA337 series is unity-gain stable. They are easy-to-use and are free from phase inversion and overload problems found in other op-amps. Performance is maintained as amplifiers swing to their specified limits.

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3 System Design Theory

Considering a backup time of 0.5 s for a 10-W load and efficiency of 80%, the design requires a minimum of 5 J of energy. As most PLCs are limited in a supply current of 2 A, to the design needs to have a low capacitive load for a backup source. Low capacitance requires a higher voltage margin to provide the required energy. This design uses the LM5001 boost converter to charge the backup capacitor up to 36 V. The LM5001 is slope compensated, current mode PWM controlled. Thus, the COMP voltage changes per load. Also, the LM5001 has an internal cycle-by-cycle current limiting up to 1.2 A. This current makes it ideal for charging the capacitor and running in light mode after charging.

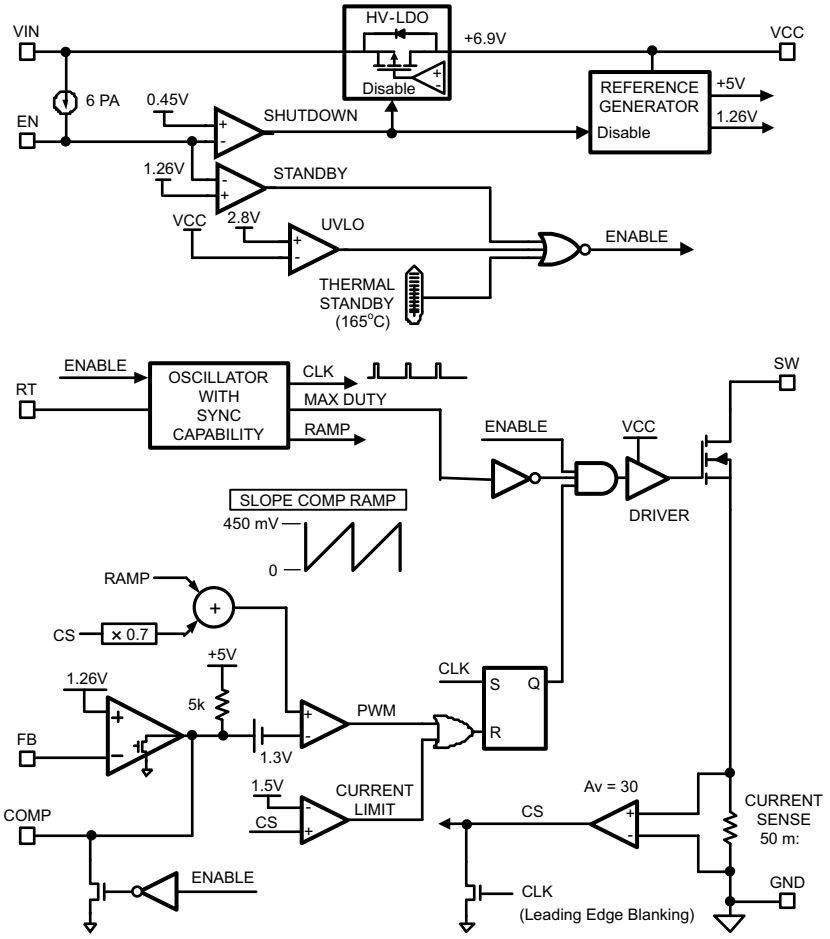

Figure 3. LM5001 Circuit Diagram

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3.1 Capacitor Calculation

The energy stored in the capacitor is given by Equation 1:

$$E = \frac{1}{2}C\left(V_a^2 - V_b^2\right) \quad (1)$$

V_a and V_b correspond to the initial and final voltage of the charged capacitor while discharging.

Considering a load of 10 W and backup time of 0.5 s, the energy storage for 80% efficiency as per Equation 2 is 5 J.

$$E = \frac{P \times t}{Eff} \quad (2)$$

The electric double-layer capacitor (EDLC) is limited to a rated voltage of 5.5 V, so multiple capacitors need to be connected in a series to provide a sufficient voltage margin. Consider five capacitors in a series, each having 5.5-V rated voltage. Thus, the voltage margin for backup will be from 25 V to 15 V. The required equivalent capacitor as per Equation 1 will be 25 mF.

The reciprocal of the equivalent capacitance of the capacitors connected in the series is the sum of the reciprocals of the individual capacitances. Therefore, each capacitor needs to be at least 125 mF.

To reduce the ESR, have an EDLC capacitance with a value greater than 1 F. This approach requires complex charging topology, cell balancing, and higher charging current for a low startup time.

The electrolytic capacitor has a rated voltage of 50 V. Considering a voltage margin of 35 V to 10 V (as per Equation 1), the required capacitor will be 8.8 mF. For an additional 20% tolerance, select a 10-mF/50-V capacitor. Electrolytic capacitors have very low ESR compared to EDLCs. Table 2 highlights the difference between an electrolytic capacitor and an EDLC.

Table 2. Electrolytic Capacitor versus EDLC

PARAMETER	ALUMINUM ELECTROLYTIC NICHICON UVR1H103MRD	EDLC CAP KEMET FT0H105ZF
Value	10 mF	1 F
Rated voltage	50 V	5.5 V
ESR	0.02 E 120 Hz	3.5 E 1 KHz
Ripple current	4.4 A	—
Five in series	No	Yes
Dimensions (mm)	25 × 40 (D × H)	21.5 × 13 (D × H)
Digi-Key pricing 1K	2.45$	10.95$

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3.2 LM5001 Calculations

The LM5001 is configured in boost mode by using the internal reference for regulation. The design needs an output voltage of 35 V at 1 A to charge the capacitor. The minimum input range for boost to enable will be 18 V. The switching frequency is set at 245 KHz. Table 3 details the calculations for boost configuration.

Table 3. Boost Calculations

PARAMETER	EQUATION	CALCULATED VALUE	SELECTED VALUE
Duty cycle minimum	$D_{MIN} = 1 - \frac{V_{IN\_MAX}}{V_O}$	0.14	—
Duty cycle maximum	$D_{MAX} = 1 - \frac{V_{IN\_MIN}}{V_O}$	0.48	—
Ripple current	$I_{RIPPLE} = 0.2 \times I_O \times \frac{V_O}{V_{IN\_MIN}}$	0.388	—
Inductor L2	$L = \frac{V_{IN\_MIN} \times (V_O - V_{IN\_MIN})}{(I_{RIPPLE} \times f_{SW} \times V_O)}$	91uH	150 µH Higher inductance will reduce ripple current
Oscillator resistor R45	$R = 13.1 \times 10^9 \times \left(\frac{1}{f_{SW}} - (83 \times 10^{-9}) \right)$	52.3 K	52.3K, 1%
Enable resistor R37 $I_{DIVIDER}$ = 0.501 mA	$R = \frac{V_{IN\_MIN} - 1.26}{I_{DIVIDER}}$	33.3 K	33.2K, 1%
Enable resistor R42	$R = \frac{1.26}{I_{DIVIDER} + 6\ \mu A}$	2.49 K	2.49K, 1%
Feedback resistor R39 I_{fb} = 530 µA	$R = \frac{V_O}{I_{FB}}$	66 K	66.5K, 1%
Feedback resistor R43	$R = \frac{1.26}{0.510\ \mu A}$	2.47 K	2.49K, 1%

3.3 LM5069 Calculations

The LM5069 is a single-voltage device capable of protecting line from undervoltage, overvoltage, and inrush current.

This single-chip solution also monitors the SOA region of series pass FET using a simple resistor selection. If a fault occurs, it latches in off state. The chip can be programmed for auto-retry using a simple capacitor based on the interval required.

The LM5069 is configured for UVLO and OVLO of 16 and 32 V. The inrush current is limited to 1.9 A to prevent loading to the power source of 24 V, 2 A. The SOA is limited to 37 W, which is less than the power dissipation of MOSFET. See Table 4 for detailed calculations.

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Table 4. LM5069 Calculations

PARAMETER	EQUATION	CALCULATED VALUE	SELECTED VALUE
Current sense resistor I_{LIMIT} = 2.2 A	$R_S = \frac{0.055}{I_{LIMIT}}$	0.020 E	0.020 E
Power limit resistor P_{FET} = 40°C	$R_{PWR} = 1.25 \times 10^5 \times R_S \times P_{FET}$	125 K	115 K
Insertion delay capacitor t = 7 ms	$C = t \times 1.38 \times 10^{-6}$	9.9 nF	10 nF
Undervoltage resistor R13 V_{UVHYS} = 1 V	$R = \frac{V_{UVHYS}}{21\,\mu A}$	47.62 K	47.5 K
Undervoltage resistor R6 V_{UVL} = 16 V	$R = \frac{(2.5 \times R13)}{(V_{UVL} - 2.5)}$	8.82 K	8.87 K
Overvoltage resistor R12 V_{OVHYS} = 1 V	$R = \frac{V_{OVHYS}}{21\,\mu A}$	47.62 K	47.5 K
Overvoltage resistor R15 V_{OVL} = 31 V	$R = \frac{(2.5 \times R12)}{(V_{OVL} - 2.5)}$	4.04 K	4.02 K

The LM5069 can be configured for reverse polarity protection as shown in Figure 4. With this approach, diode D2 will not be required for reverse polarity protection.

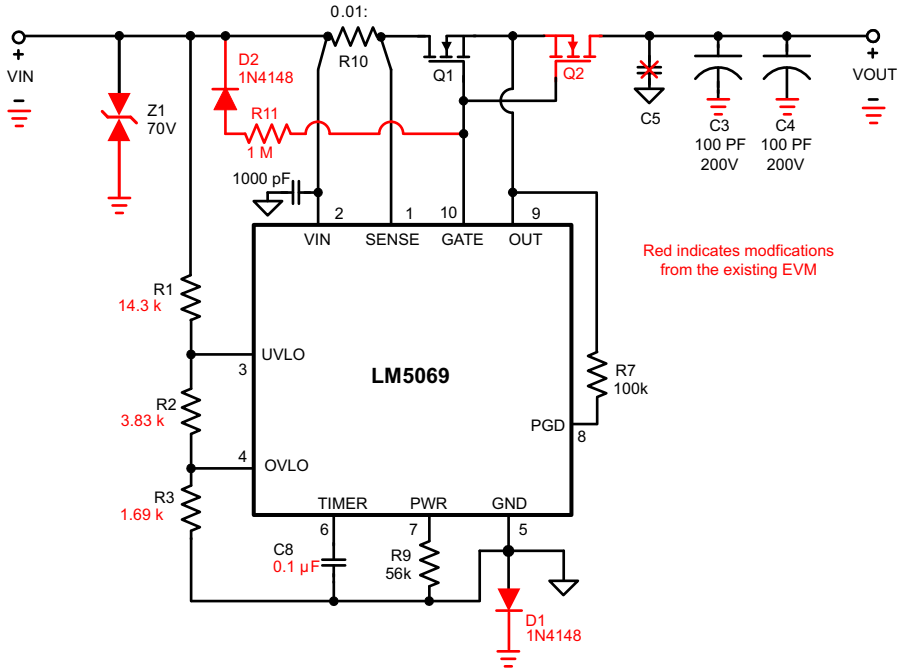

Figure 4. LM5069 With Reverse Polarity Protection

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3.4 LM334 Current Source Calculations

The LM334 is an adjustable floating current source without any additional power source requirement. The LM5001 operated in a non-synchronous boost mode due to which for a short duration the capacitive load draws maximum current.

In such an event, the LM5069 will enter in latch of state and shut-off power source. The delay timer logic of LM5069 will eventually result in more start up time. To limit the inrush current, the LM334 maintains a constant current irrespective of the load. In the transient state of LM5001, the storage capacitor will only draw controlled current for short duration. See Table 5 for detailed calculations.

Table 5. LM334 Calculations

PARAMETER	EQUATION	CALCULATED VALUE	SELECTED VALUE
Base current I_B = 6.7 mA	$R_{SET} = \frac{0.067}{I_B}$	10 E	10 E
Collector current I_B = 6.7 mA h_{fe} - 110 at 25°C MJD45H11 PNP	$I_C = h_{FE} \times I_B$	0.737 A	—

Figure 5 gives the DC current gain of transistor (MJD45H11), which is fairly constant at 110 for 25°C. Figure 6 shows, for DC operation the maximum collector current allowed for 30 V is 0.7 A, and for 5 ms it is at 1.4 A. As the capacitor charges to 1 V in less than 10 ms, the SOA of transistor is not violated.

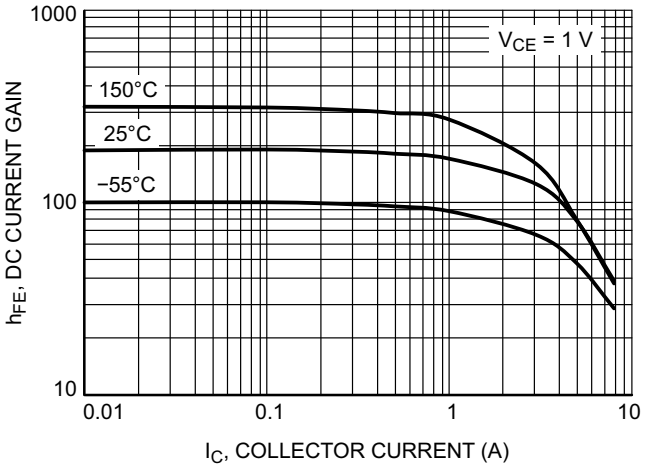

Figure 5. DC Current Gain

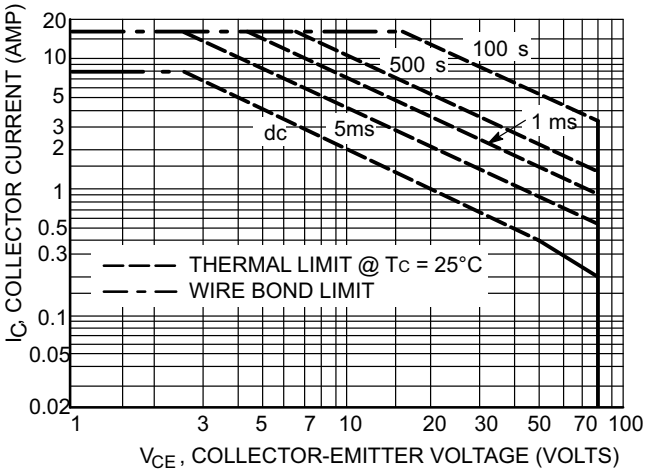

Figure 6. SOA of Transistor

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3.5 O-Ring Calculations

The backup capacitor C16 needs to source power to load in case of an input supply failure. The single supply inverting Schmitt trigger U3 continuously compares the input for a threshold of 18 V and immediately switches the transistors Q3 and Q4. As the transistor turns on the P-Channel MOSFET Q1, Q2 starts conducting. Diode D1 prevents the reverse current flow of the backup supply. LDO U4 provides constant supply of 5 V to both op-amp U1 and U3.

The inverting Schmitt trigger threshold is controlled by output. As output has two stable states, the threshold has two possible values. See Table 6 for calculations.

Table 6. Schmitt Trigger

PARAMETER	EQUATION	CALCULATED VALUE	SELECTED VALUE
R1 R6 = 10 K V_{TH} = 1 V at 18-V input	$R1 = \left(\frac{R6}{\frac{V_{TH}}{V_{IN\_MAX}}} \right) - R6$	170 K	169 K
$V_{IN(MIN)}$ V_{TL} = 0.9	$\frac{V_{TL}}{\frac{R6}{R6 + R1}}$	16.11	—
R24 V_{TH} = 1 V at 18-V input V_{CC} = 5 V R21 = 10 K, R22 = 100 K	$\frac{1}{R24} = \left(\frac{V_{CC} - V_{TH}}{V_{TH}} \right) \times \left(\frac{1}{R21} + \frac{1}{R22} \right)$	2.2 K	2.26 K
V_{TL} V_{CC} = 5 V	$\left(\frac{R24 \,\|\| R23}{(R24 \,\|\| R23) + R21} \right) \times V_{CC}$	0.904	—

Additionally, R4 of 5K is added to the source current as the op-amp U3 has an open collector output. The propagation delay of the op-amp highly depends upon the capacitive load at the output. As U3 is driving the transistor Q3 and Q4, the internal capacitance will affect the turn on time. The current DC gain for the transistor is given by Equation 3:

$$h_{fe} = \frac{\beta}{1 + jwr_n \times (C_\mu + C_\pi)} \tag{3}$$

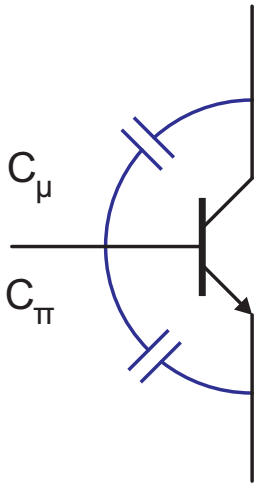

Figure 7. Internal Capacitance of BJT

The internal capacitance is in pF and can be neglected as the switching frequency is low.

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3.6 Monitoring

3.6.1 Power Supply

The host processor can monitor the PG pin of the LM5069 and take preventive backup action when power supply failure is observed.

3.6.2 Capacitor Failure

There are two main types of failure in capacitor: catastrophic failure like short or open, and degradation failure.

Degradation failure is mainly due to the operating condition of the capacitor and depends upon temperature changes due to ripple current and charge and discharge rates.

Temperature Changes Due to Ripple Current
The internal temperature change due to ripple current is given by Equation 4:

$$\Delta t = \frac{I_{RIPPLE}^2 \times R_{ESR}}{\beta \times A} \quad (4)$$

where β is heat radiation constant 10^{-3}W/°C.cm^2.

A is the surface area given by Equation 5:

$$A = \frac{\pi}{4} \times D \times (D + 4 \times L) \quad (5)$$

D and L are diameter and length of the capacitor. In discharge mode, the ripple current depends on the switching converter at the load side. As the ESR of the selected capacitor is less, heat generation will be low for a ripple current less than the maximum permissible value specified in the UVR1H103MRD capacitor datasheet.

Charge and Discharge Rate
If the capacitor is charged or discharged frequently, an oxide layer forms on the cathode foil, decreasing the overall capacitance. Also due to a continuous electro-chemical reaction, internal gas collects inside the capacitor, which increases the pressure. This may result in permanent failure of capacitor. Select a capacitor based upon the rate at which a power interrupt might occur. The capacitor's manufacturer provides a specialized capacitor for high charge and discharge rates.

The host processor can also monitor the charging and discharging rate and have an algorithm to predict the ESR change over time.

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4 Getting Started: Hardware

The design can be operated directly out of the box. The required test point has been populated to measure signals at each interface point of the design. Before powering up the board, check for jumper positions as described in Table 7.

Table 7. Jumper Settings

JUMPER REF	DESCRIPTION	DEFAULT VALUE
J4	Enable supply line	Short
J2	5-V V_{CC} select	Short
J1	Enable backup supply	Short
J14	Connect storage capacitor to boost	Short
J6	To test inrush current behavior of load capacitor	DNP

Table 8 provides test points to probe voltages at various nodes of the design.

Table 8. Test Points

TEST POINT NO	DESCRIPTION	VOLTAGE RANGE
TP1	Supply voltage	18 to 30 V
TP2	Buffer output	1 V at 18-V input 0.9 V at 16.5-V input
TP3	Output voltage	Normal 18 to 30 V Backup 35 to 10 V
TP8	Power good	5 V at 18 V < V_{IN} < 31 V Low at V_{IN} < 18 V
TP9	V_{CC} output	5 V
TP10, TP6, TP7	Schmitt trigger output	High at V_{IN} < 16.1 V Low at V_{IN} > 18 V
TP14	Input for boost	18 to 30 V
TP15	Boost output	36 V
TP16	Enable voltage	1.26 at 18 V
TP4, TP5, TP18	GND	0 V

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5 Test Setup

This design is tested for minimum input voltage of 18-V $V_{IN(MIN)}$. The test setup consists of the TIDA-00500 board, Keithley DC Supply, Tektronix MSO, and configurable electronic load as shown in Figure 8.

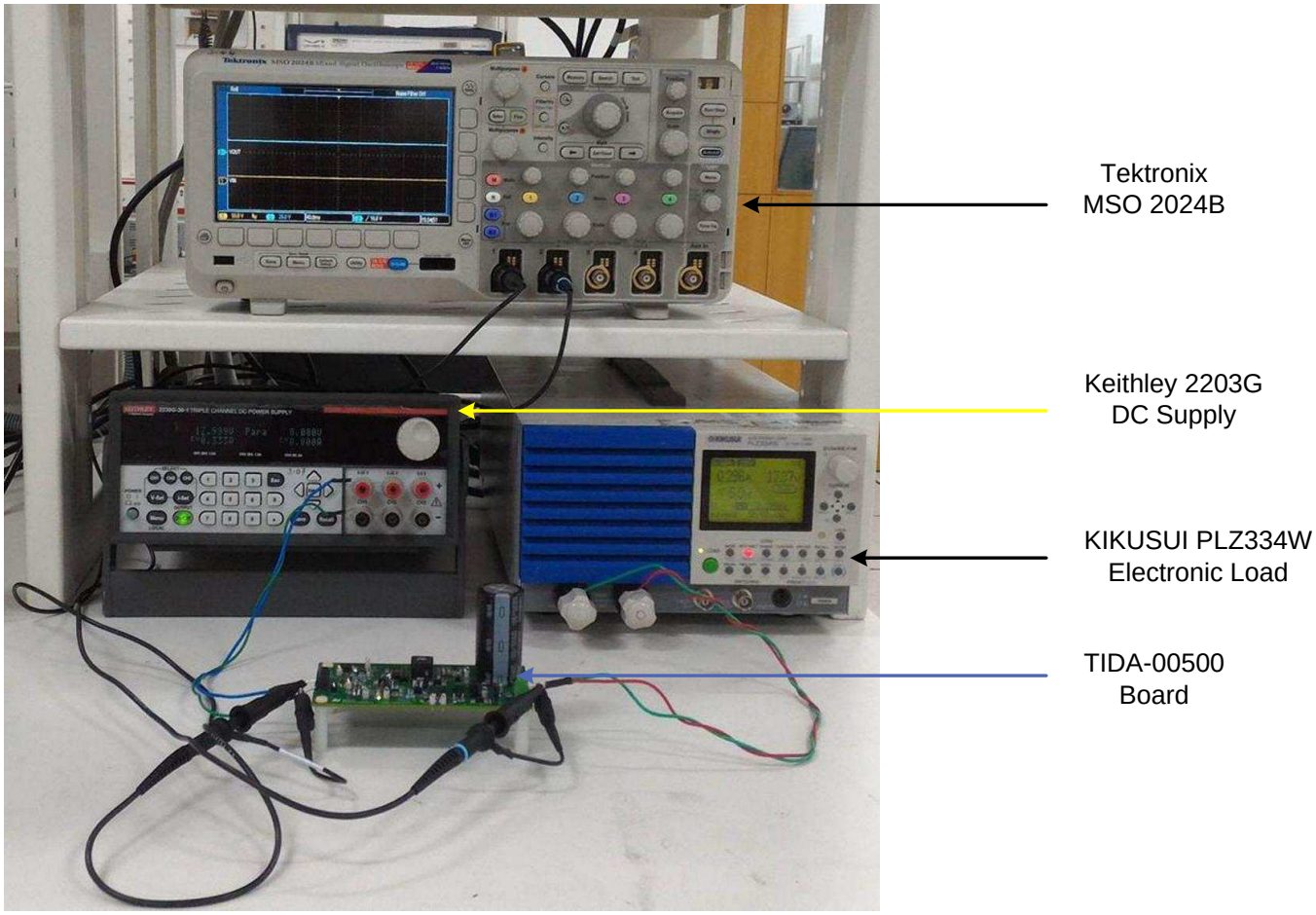

Figure 8. TIDA-00500 Test Setup

The design was tested under the following conditions:

1. Startup behavior at lowest input voltage
2. Backup capacitor charging time for minimum, nominal, and maximum voltage input
3. Power interrupts behavior for 5-W and 10-W loads

To test the above conditions, the electronic load is configured in constant current (CC) for the 10-W load during startup phase. A load of 10 W is set for all input voltage by changing CC to an appropriate current value.

The DC power is shut off to test the power interrupt scenario. During backup mode, the load is configured to CP mode for 5 W and 10 W.

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6 Tests Results

6.1 Test Table

Startup behavior is checked with 100% load for a 18-V input supply. The backup time is observed for 5-W and 10-W loads.

Table 9. Test Results

CHARGING PHASE		
INPUT VOLTAGE, V_{IN} (V)	OUTPUT LOAD (W)	CHARGING TIME (ms)
18	10	434
24	10	314
30	10	250
DISCHARGING PHASE		
LOAD (W)		**BACKUP TIME (s)**
5		1.14
10		0.634

6.2 Timing Plots

The following plots reflect the design behavior during start-up and backup mode.

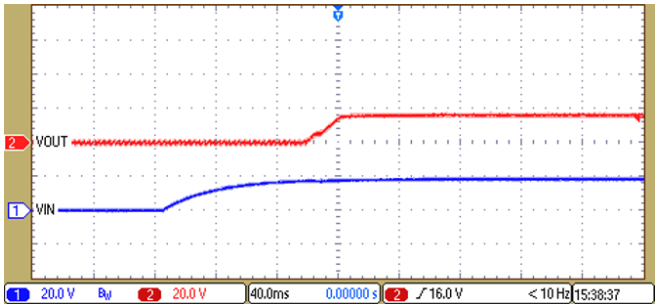

Figure 9. Startup at V_{IN} = 18 V, 10-W Load

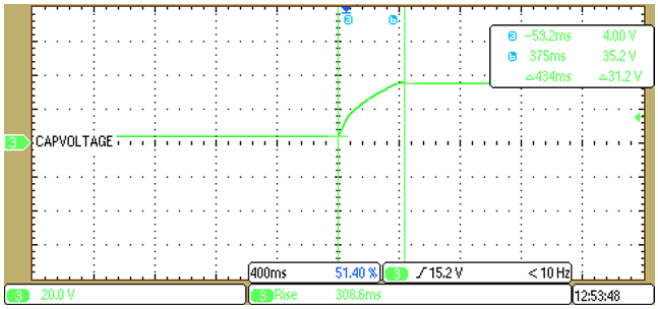

Figure 10. Capacitor Charging at V_{IN} = 18 V, 10-W Load

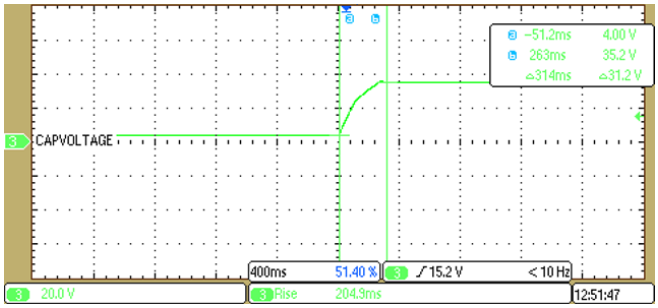

Figure 11. Capacitor Charging at V_{IN} = 24 V, 10-W Load

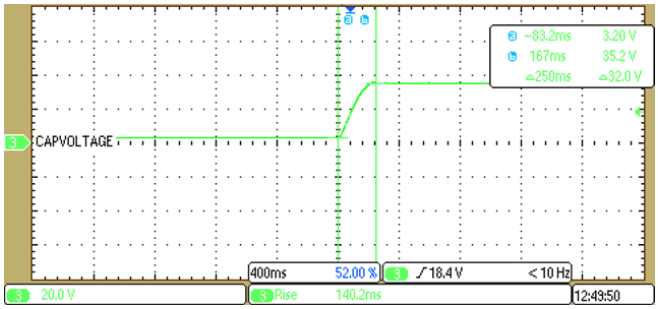

Figure 12. Capacitor Charging at V_{IN} = 30 V, 10-W Load

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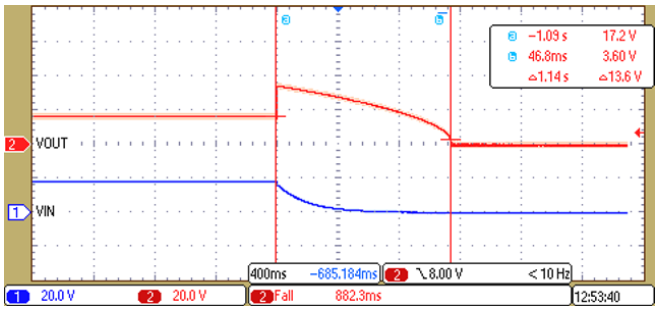

Figure 13. Backup for 5 W

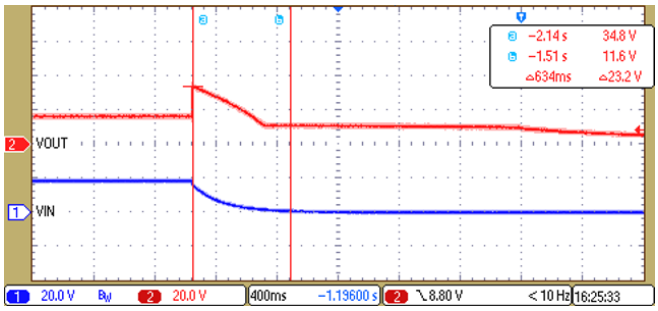

Figure 14. Backup for 10 W

6.3 Thermal Analysis

There are three modes of operation: Charging Mode, Light Charging Mode, and Backup Mode. Because Backup Mode lasts for a short time, thermal impact is not significant. Also, due to the very low I^2R drop across the P-Channel FET, heat dissipation is very low.

Figure 15 and Figure 16 have been captured with a FLUKE Ti400 at room temperature. The scale in the two figures has been adjusted so that the color coding matches.

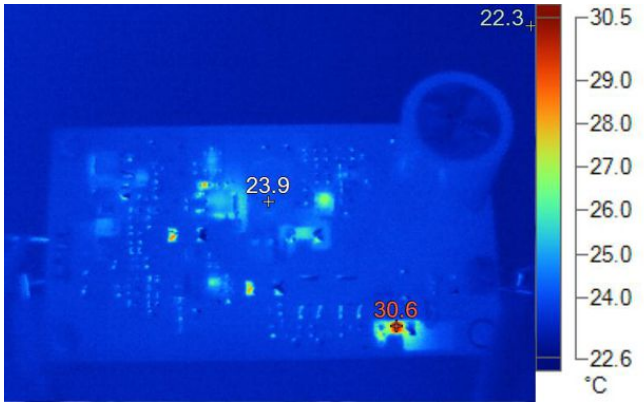

Figure 15. Thermal Analysis, Charging Mode With 10-W Load at V_{IN} = 18 V

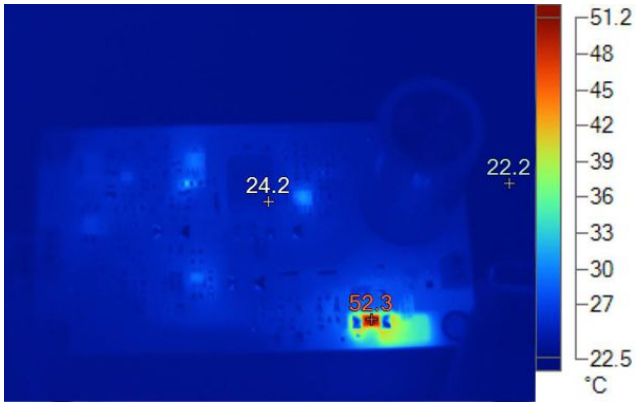

Figure 16. Thermal Analysis, Light Charging Mode With 10-W Load at V_{IN} = 18 V

Figure 15 and Figure 16 show the overall temperature is within 55°C. The thermal rise in diode D2 can be further reduced by implementing an FET O-Ring as described in Section 3.3.

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7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00500.

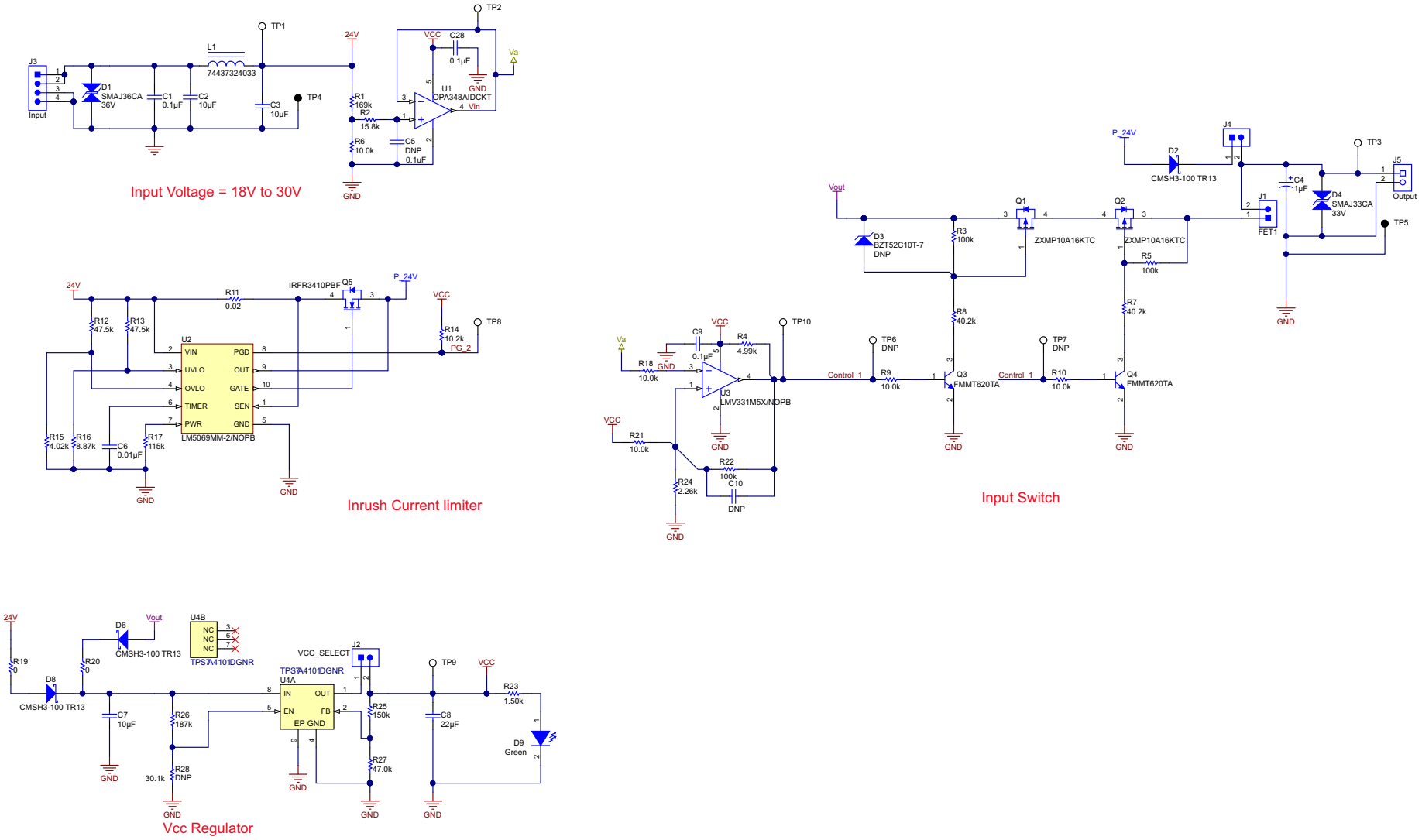

Figure 17. Input Switching Schematic

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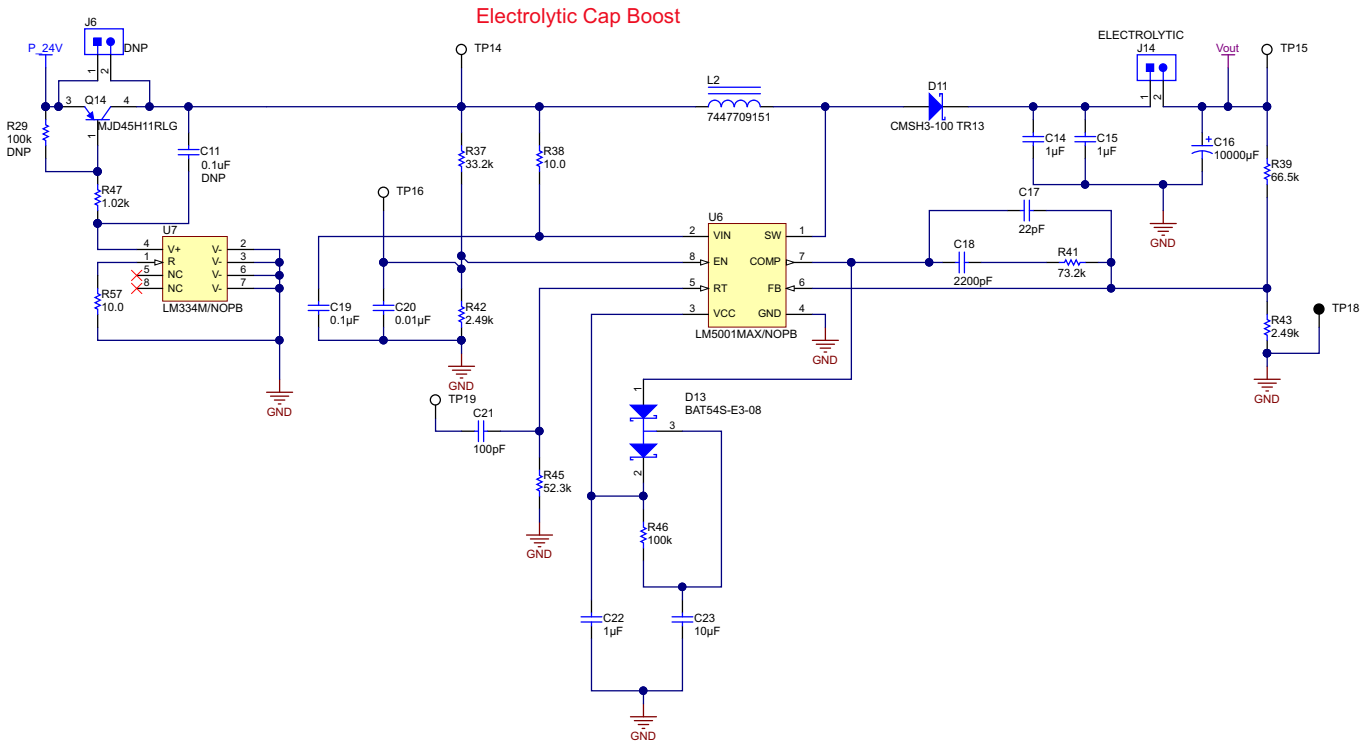

Figure 18. Boost Converter Schematic

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7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00500.

Table 10. BOM

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
1	1	!PCB1	Printed Circuit Board	Any	TIDA-00500	
2	1	R14	RES, 10.2 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210K2FKED	0402
3	1	R17	RES, 115 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402115KFKED	0402
4	1	C1	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0805	Kemet	C0805C104K1RACTU	0805
5	1	C17	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0805	Kemet	C0805C220J5GACTU	0805_HV
6	1	C18	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0805	TDK	C2012C0G1H222J	0805_HV
7	1	C20	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X7R, 0805	TDK	C2012X7R2A103K	0805_HV
8	1	C21	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0805	TDK	C2012C0G1H101J	0805_HV
9	1	C23	CAP, CERM, 10 µF, 16 V, +/- 10%, X5R, 0805	MuRata	GRM21BR61C106KE15L	0805_HV
10	1	R1	RES, 169 k, 0.1%, 0.125 W, 0805	Yageo America	RT0805BRD07169KL	0805_HV
11	1	R15	RES, 4.02 k, 1%, 0.125 W, 0805	Panasonic	ERJ-6ENF4021V	0805_HV
12	1	R16	RES, 8.87 k, 1%, 0.125 W, 0805	Panasonic	ERJ-6ENF8871V	0805_HV
13	1	R2	RES, 15.8 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080515K8FKEA	0805_HV
14	1	R23	RES, 1.50 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08051K50FKEA	0805_HV
15	1	R24	RES, 2.26 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08052K26FKEA	0805_HV
16	1	R25	RES, 150 k, 1%, 0.125 W, 0805	Panasonic	ERJ-6ENF1503V	0805_HV
17	1	R26	RES, 187 k, 1%, 0.125 W, 0805	Panasonic	ERJ-6ENF1873V	0805_HV
18	1	R27	RES, 47.0 k, 1%, 0.125 W, 0805	Panasonic	ERJ-6ENF4702V	0805_HV
19	1	R28	RES, 30.1 k, 1%, 0.125 W, 0805	Panasonic	ERJ-6ENF3012V	0805_HV
20	1	R37	RES, 33.2 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080533K2FKEA	0805_HV
21	1	R39	RES, 66.5 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080566K5FKEA	0805_HV
22	1	R4	RES, 4.99 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08054K99FKEA	0805_HV
23	1	R41	RES, 73.2 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080573K2FKEA	0805_HV
24	1	R45	RES, 52.3 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080552K3FKEA	0805_HV
25	1	R47	RES, 1.02 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08051K02FKEA	0805_HV

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Table 10. BOM (continued)

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
26	2	C6, C10	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0805	TDK	C2012X7R1H103K	0805_HV
27	2	R12, R13	RES, 47.5 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080547K5FKEA	0805_HV
28	2	R19, R20	RES, 0, 5%, 0.125 W, 0805	Yageo America	RC0805JR-070RL	0805_HV
29	2	R38, R57	RES, 10.0, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080510R0FKEA	0805_HV
30	2	R42, R43	RES, 2.49 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08052K49FKEA	0805_HV
31	2	R7, R8	RES, 40.2 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080540K2FKEA	0805_HV
32	5	C5, C9, C11, C19, C28	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0805	TDK	C2012X7R1H104K	0805_HV
33	5	R3, R5, R22, R29, R46	RES, 100 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805100KFKEA	0805_HV
34	5	R6, R9, R10, R18, R21	RES, 10.0 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080510K0FKEA	0805_HV
35	1	C8	CAP, CERM, 22 µF, 10 V, +/- 20%, X5R, 1210	TDK	C3225X5R1A226M	1210
36	2	C2, C3	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210	MuRata	GRM32ER71H106KA12L	1210
37	3	C14, C15, C22	CAP, CERM, 1 µF, 100 V, +/- 10%, X7R, 1210	TDK	C3225X7R2A105K200AA	1210
38	1	R11	RES, 0.02, 1%, 0.33 W, 1210	Panasonic	ERJ-L14KF20MU	1210M
39	1	C7	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1210	TDK	C3225X5R1H106K250AB	1210_280
40	1	U1	1 MHz, 45 uA, RRIO, Single Operational Amplifier, 2.1 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DCK0005A), Green (RoHS & no Sb/Br)	Texas Instruments	OPA348AIDCKT	DCK0005A_N
41	1	U4	Single Output LDO, 50 mA, Adjustable 1.175 to 48 V Output, 7 to 50 V Input, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS7A4101DGNR	DGN0008B_N
42	1	Q14	Transistor, PNP, 80 V, 8 A, DPAK	ON Semiconductor	MJD45H11RLG	DPAK
43	1	Q5	MOSFET, N-CH, 100 V, 31 A, DPAK	International Rectifier	IRFR3410PBF	DPAK
44	2	Q1, Q2	MOSFET, P-CH, -100 V, 3 A, DPAK	Diodes Inc.	ZXMP10A16KTC	DPAK
45	3	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial10-20
46	3	TP4, TP5, TP18	Test Point, Compact, Black, TH	Keystone	5006	Keystone5006
47	10	TP1, TP2, TP3, TP8, TP9, TP10, TP14, TP15, TP16, TP19	Test Point, Compact, White, TH	Keystone	5007	Keystone5007
48	2	TP6, TP7	Test Point, Compact, White, TH	Keystone	5007	Keystone5007

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Table 10. BOM (continued)

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
49	4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Keystone_1902C
50	1	D9	LED, Green, SMD	OSRAM	LG L29K-G2J1-24-Z	LG L29K_GREEN
51	1	U6	High Voltage Switch Mode Regulator, 8-pin Narrow SOIC, Pb-Free	Texas Instruments	LM5001MAX/NOPB	M08A_N
52	1	U7	3-Terminal Adjustable Current Source, 8-pin Narrow SOIC, Pb-Free	Texas Instruments	LM334M/NOPB	M08A_N
53	1	U3	Single General Purpose, Low Voltage, Tiny Pack Comparator, 5-pin SOT-23	Texas Instruments	LMV331M5X/NOPB	MF05A_N
54	1	U2	Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free	Texas Instruments	LM5069MM-2/NOPB	MUB10A_N
55	4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	NY PMS 440 0025 PH
56	1	J5	Conn Term Block, 2POS, 3.81mm, TH	Phoenix Contact	1727010	PhoenixConact_1727010
57	1	D1	Diode, TVS, Bi, 36 V, 400 W, SMA	Littelfuse	SMAJ36CA	SMA
58	1	D4	Diode, TVS, Bi, 33 V, 400 W, SMA	Littelfuse	SMAJ33CA	SMA
59	4	D2, D6, D8, D11	Diode, Schottky, 100 V, 3 A, SMC	Central Semiconductor	CMSH3-100 TR13	SMC
60	1	C4	CAP, AL, 1 µF, 50 V, +/- 20%, 5 ohm, SMD	Panasonic	EEE-FC1H1R0R	SM_RADIAL_B
61	1	D3	Diode, Zener, 10 V, 300 mW, SOD-523	Diodes Inc.	BZT52C10T-7	SOD-523
62	1	D13	Diode, Schottky, 30 V, 0.2 A, SOT-23	Vishay-Semiconductor	BAT54S-E3-08	SOT-23
63	2	Q3, Q4	Transistor, NPN, 80 V, 1.5 A, SOT-23	Diodes Inc.	FMMT620TA	SOT-23
64	1	J3	Terminal Block, 6A, 3.5mm Pitch, 4-Pos, TH	On-Shore Technology	ED555/4DS	TERM_BLK_ED555-4DS
65	1	C16	CAP, AL, 10000 µF, 50 V, +/- 20%, ohm, TH	Nichicon	UVR1H103MRD	VR_2500x5000
66	1	L1	Inductor, Shielded Drum Core, Powdered Iron, 3.3 µH, 2.5 A, 0.069 ohm, SMD	Wurth Elektronik	74437324033	WE-LHMI_4020
67	1	L2	Inductor, Shielded Drum Core, Ferrite, 150 µH, 2.1 A, 0.2 ohm, SMD	Wurth Elektronik	7447709151	WE-PD_1210
68	1	J1	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	WURTH_61300211121
69	1	J14	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	WURTH_61300211121
70	1	J2	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	WURTH_61300211121
71	1	J4	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	WURTH_61300211121
72	1	J6	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	WURTH_61300211121

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7.3 PCB Layout Recommendations

The PCB layout recommendation is driven by low EMI and good thermal performance. The layout has been implemented on a two-layer board with 35-µm copper. Each IC is provided enough copper heat sink area to limit the device temperature below 85°C.

Figure 19 shows the current path for inrush protection. Place the sense resistor R11 and series pass FET very near to the LM5069. Signal P_24V is routed as shape to support a higher current load.

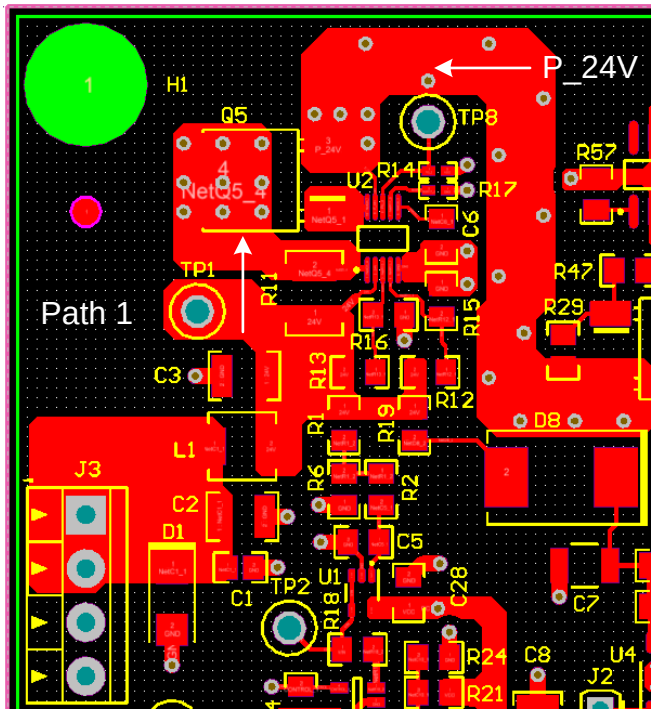

Figure 19. LM5069 Inrush Placement

As shown in Figure 20, the SW pin of the LM5001, switching inductor L2, diode D11, and capacitors C14, C15 are placed in close proximity to minimize the effective loop area as shown by Path 2. The boost charging current Path 3 is routed as shape to effectively reduce impedance for charging the backup capacitor C16.

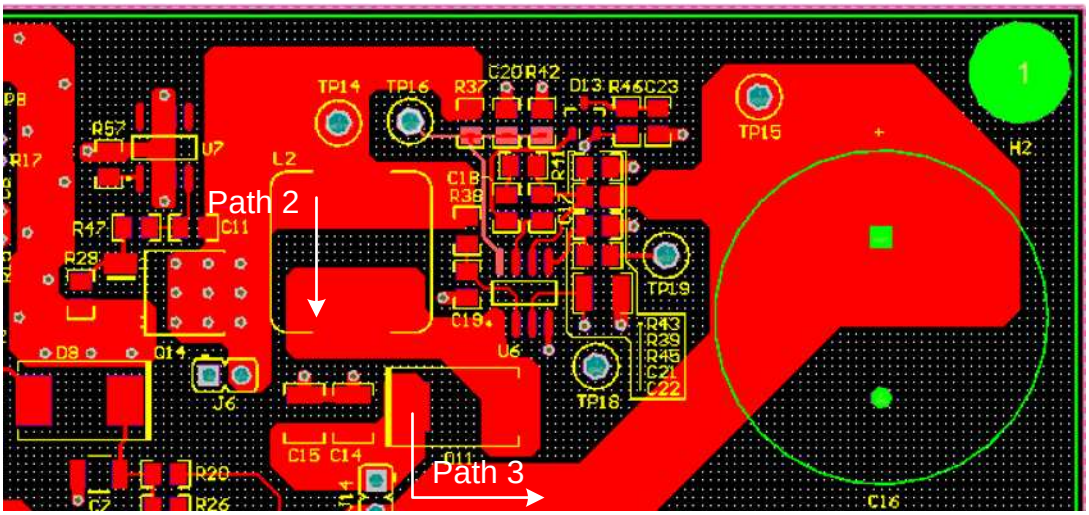

Figure 20. LM5001 Boost

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As shown in Figure 21, P-Channel FETs Q1 and Q2 are placed close to backup capacitor C16 and load connector J5 to have a short impedance path. The O-Ring diode D2 is also placed near the load connector J5. Thermal vents are provided to Q1 and Q2 for better heat dissipation.

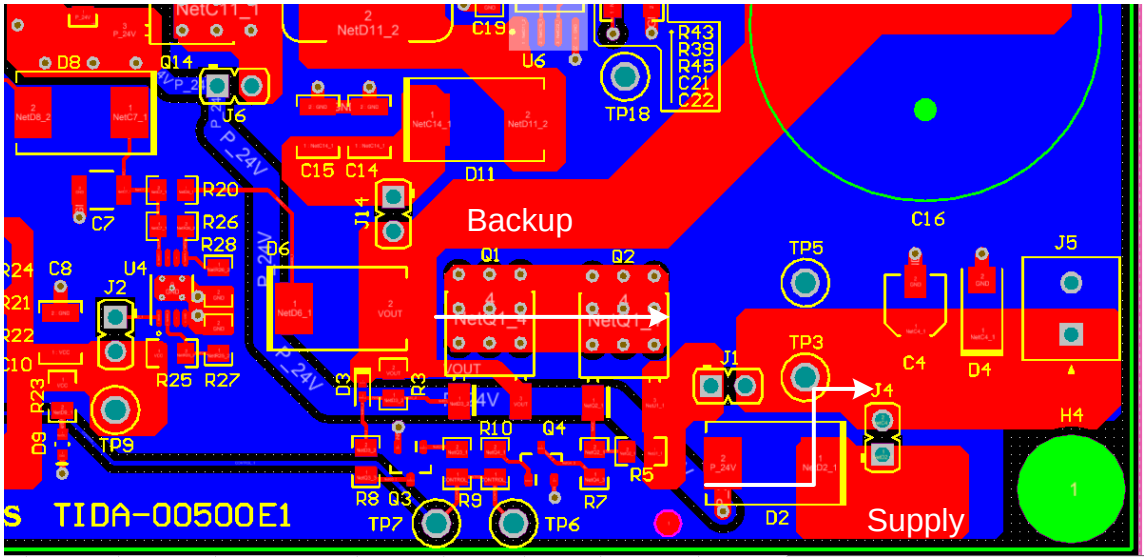

Figure 21. Power O-Ring FET

7.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00500.

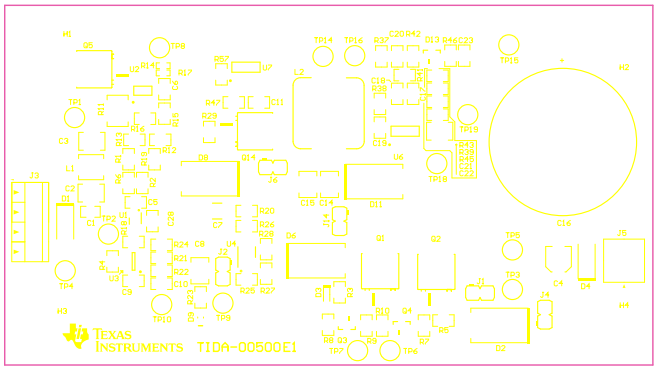

Figure 22. Top Overlay

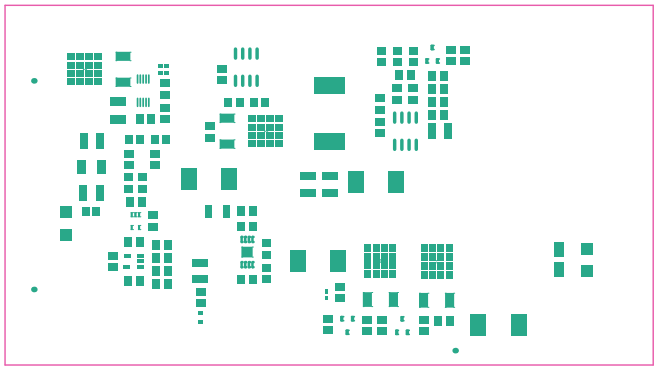

Figure 23. Top Paste

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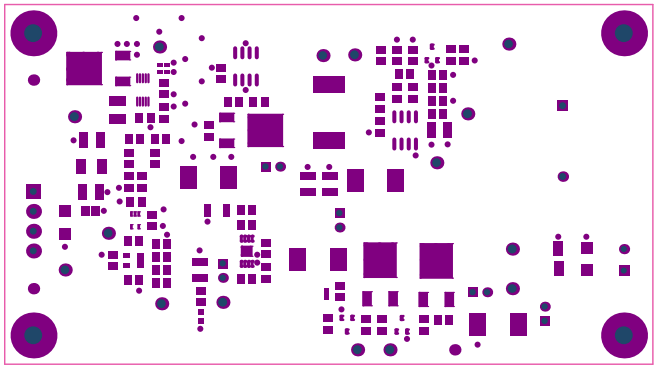

Figure 24. Top Solder

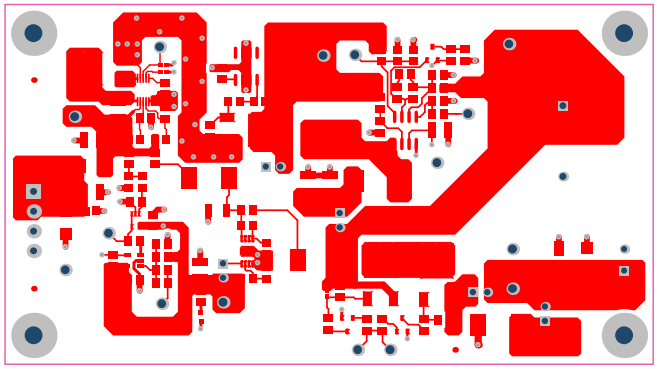

Figure 25. Top Layer

Figure 26. Bottom Paste

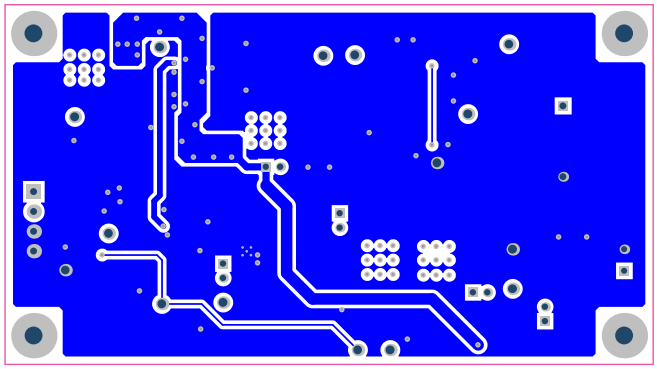

Figure 27. Bottom Layer

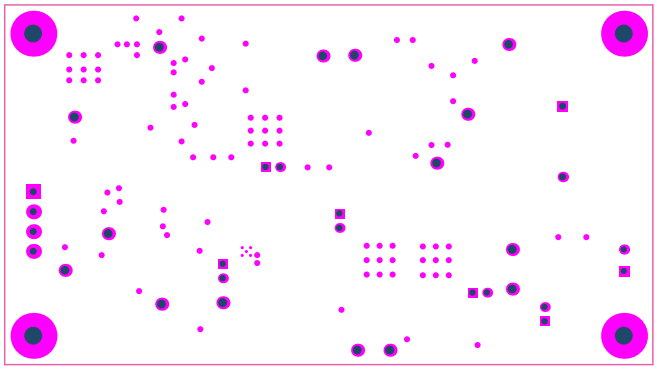

Figure 28. Bottom Solder

Figure 29. Bottom Overlay

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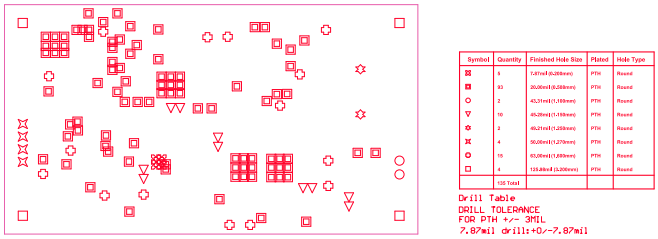

Figure 30. Drill Drawing

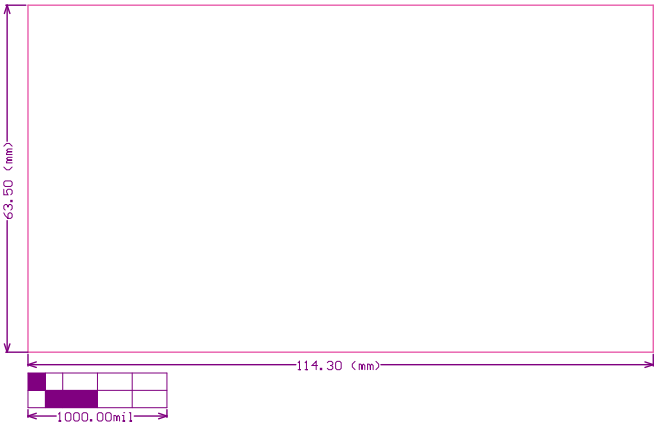

Figure 31. Board Dimensions

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00500.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00500.

8 References

1. Texas Instruments, *High-Efficiency Backup Power Supply*, Application Report (SLVA676)
2. Nichicon, *General Descriptions of Aluminum Electrolytic Capacitors* (PDF)
3. ON Semiconductor, *Using MOSFETs in Load Switch Applications* (PDF)

9 About the Author

SRINIVASAN IYER is a Systems Engineer at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Srinivasan has four years of experience in analog circuit designs for field transmitters and signal chains.

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Revision History

Changes from Original (September 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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