TI Designs

HART Field Transmitter for RTD Temperature Design Guide

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDM-HRTTRANSMITTER	Tool Folder Containing Design Files
MSP-EXP430FR5969	Tool Folder
ADS1220	Product Folder
DAC161S997	Product Folder
OPA2342	Product Folder
TPS7A1601	Product Folder

TI E2E™ Community

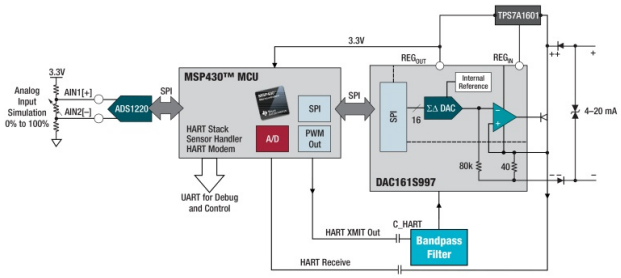
ASK Our E2E Experts
WEBENCH® Calculator Tools

Design Features

- BoosterPack Design Enables Easy LaunchPad™ Development
- Input Power Supply Range: 7-V to 33-V DC
- Operating Temperature Range -40°C To 85°C
- Sensor Input Compatible With 2-, 3-, or 4-wire Resistance Temperature Detector (RTD) Probes
- Connects To Any RTD From PT100 To PT1000
- Implements Ratiometric Measurement
- RTD Temperature Range -200°C to 850°C
- Maximum Measured Error: 0.2°C
- 4- to 20-mA Current Loop Output Signal
- Output Resolution: 0.76 µA
- Designed To Meet FieldComm Group HART Requirements
- Full HART v7.3 Protocol Implementation

Featured Applications

- Factory Automation And Process Control
- Sensors And Field Transmitters



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

4- to 20-mA current-loop systems are popular worldwide. The majority of smart field devices are HART-enabled. The HART (Highway Addressable Remote Transducer) Protocol remains a global standard for sending and receiving digital information across analog wires.

This design takes advantage of the peripherals and low-power capabilities of the MSP430FR5969 to achieve a self-powered (2-wire) HART field transmitter design. The traditional HART modem functionality is integrated into the MCU using the MSP430™ on-chip timer and 12-bit ADC (Analog-to-Digital Converter) modules. This HART functionality is then superimposed onto a current-loop system involving the ADS1220 and the DAC161S997, which share a serial peripheral interface (SPI) bus for data transfer and configuration.

1.1 MSP-EXP430FR5969

The MSP430FR5969 LaunchPad™ serves as a simple development platform and an easy form factor to highlight applications requiring HART protocol. The LaunchPad ecosystem provides a standard pin-out for prototyping and designing BoosterPacks for different sensors and applications. The LaunchPad also provides an easy method for debugging and communicating to the application device. This design was built and tested on Revision 2.0 of the MSP-EXP430FR5969. Any revision of the MSP-EXP430FR5969 equal to or more recent than this revision will be compatible with this design. Although the LaunchPad ecosystem was selected for this design, standalone MSP430FR5xx devices may also be used for a similar application.

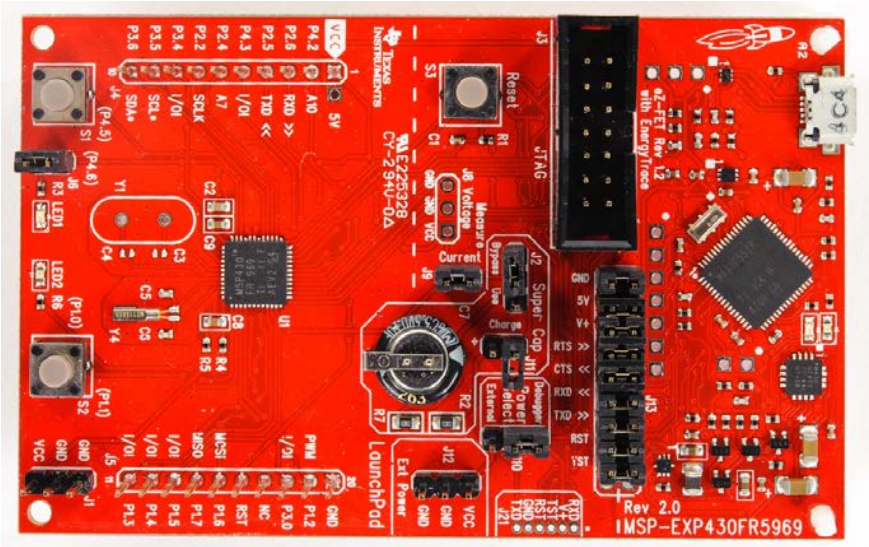


Figure 1. MSP-EXP430FR5969

The MSP430FR5969 on board the LaunchPad serves as the field transmitter main microcontroller. This microcontroller employs the eUSCI modules to communicate to the ADS1220 and DAC161S997 via the SPI. The MSP430™ also uses its timer modules to modulate and demodulate the HART FSK signals. More specifically, one timer module is operated via software to create a PWM to modulate the FSK tones. For demodulation purposes, the loop DC bias is filtered out and the HART tones themselves are put into the ADC12_B of the MSP430. Software is then used to extract whether the tone represents a “0” or a “1.” Finally, the MSP430FR5969 is also in charge of the HART stack. The HART stack takes the raw data coming from the loop and interprets it per the HART protocol, allowing the field transmitter device to properly respond to the master.

1.2 ADS1220 RTD BoosterPack™

The ADS1220 RTD BoosterPack conforms to the LaunchPad Ecosystem standard pin-out and has a silkscreen label for each used pin to discern which signals are placed where. The ADS1220 RTD BoosterPack contains the TI ADS1220 as well as passive components and connectors. This BoosterPack serves as the front end for the system and is designed to be compatible with 2-, 3-, or 4-wire RTD operation.

Figure 2. ADS1220 RTD BoosterPack

The ADS1220 receives communication via an SPI module and derives its power from either the MSP-EXP430FR5969 LaunchPad, or the power derived from the 4-20-mA current loop. The ADS1220 on board the BoosterPack is set up per the applications documentation in the ADS1220 Datasheet for RTD Measurement. The ADS1220 RTD BoosterPack is not currently available on the TI estore, but all design files for the hardware are included on the TI Design webpage, so the BoosterPack may be produced at the user's discretion.

1.3 DAC161S997 + HART-FSK BoosterPack™

The DAC161S997 + HART-FSK BoosterPack (DAC + HART BP) also conforms to the same LaunchPad Ecosystem standard pin-out and also has a silkscreen label for each pin used similar to the ADS1220 RTD BoosterPack. The DAC + HART BP contains the TI TPS7A1601 Low-Dropout Regulator, TI DAC161S997, TI OPA2342, and the appropriate passive components. This BoosterPack serves as the communications portion of the design, including filtering for HART transmit and receive signals as well as transmitting the analog current value.

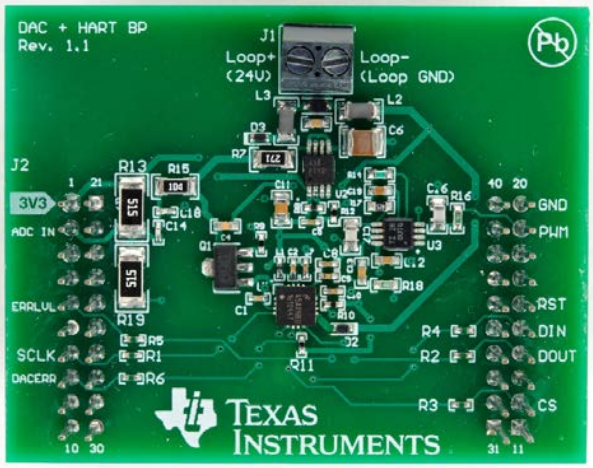


Figure 3. DAC161S997 + HART FSK BoosterPack

Similar to the ADS1220, the DAC161S997 receives communication via an SPI module and derives its power either from the MSP-EXP430FR5969 LaunchPad™ or the power derived from the TPS7A1601 (and the 4-20-mA current loop). The DAC161S997 on the DAC + HART BP receives communication via the SPI to drive the loop current. Additionally, a timer PWM output from the MSP430FR5969 is routed to an active filter (using the OPA2342) to generate HART FSK tones, which are then capacitively coupled into

the DAC161S997 per the DAC161S997 Datasheet application information for the HART signal injection. To receive HART signals, a passive filter is present on the DAC + HART BP to filter the loop signal and bias it for measurement by the ADC12_B module on the MSP430FR5969. The DAC + HART BP is not currently available on the TI eStore, but all design files for the hardware are included on the TI Design webpage, so the BoosterPack may be produced at the user's discretion.

2 Block Diagram

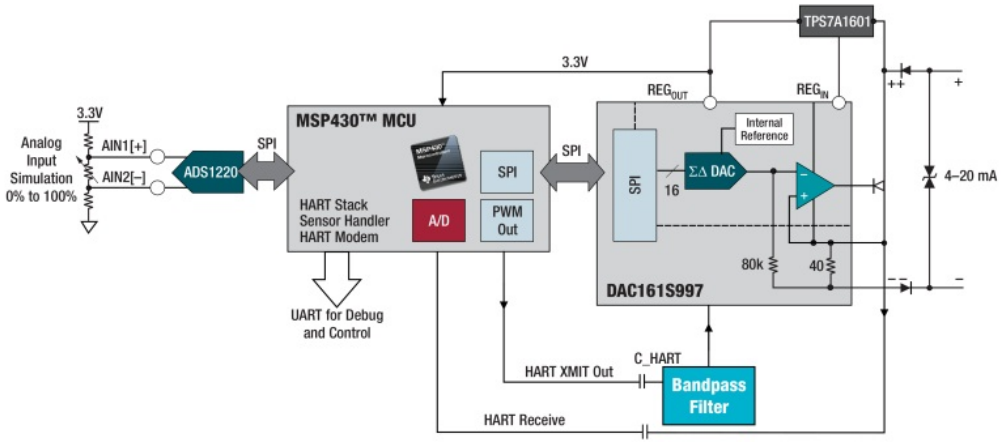


Figure 4. HART Field Transmitter Block Diagram

2.1 Highlighted Products

2.1.1 MSP-EXP430FR5969 LaunchPad™

- MSP430 ULP FRAM technology based MSP430FR5969 16-bit MCU
  - 64KB FRAM / 2KB SRAM
  - 16-Bit RISC Architecture up to 8-MHz FRAM access / 16-MHz system clock speed
  - 5 Timer Blocks
  - Analog: 16-Ch 12-Bit differential ADC, 16-Ch Comparator
  - Digital: AES256, CRC, DMA, HW MPY32
- EnergyTrace + [CPU State] + [Peripheral State] available for ultra-low-power debugging
- 20-pin LaunchPad standard leveraging the BoosterPack ecosystem
- 0.1-F SuperCap for standalone power
- Onboard eZ-FET emulation
- 2 buttons and 2 LEDs for user interaction
- Back-channel UART via USB to PC
- Available in TI eStore

2.1.2 ADS1220

- Low current consumption:
- Duty-cycle mode: 120 µA
- Normal mode: 415 µA
- Wide supply range: 2.3 V to 5.5 V
- Programmable gain: 1 V / V to 128 V / V
- Programmable data rates: up to 2 kSPS
- 50-Hz and 60-Hz rejection at 20 SPS
- Low-noise PGA: 90 nVRMS at 20 SPS
- Dual matched programmable current sources: 10 µA to 1500 µA
- Internal temperature sensor: 0.5°C error (max)
- Low-drift internal reference
- Low-drift internal oscillator
- Two differential or four single-ended inputs
- SPI™-compatible interface
- 3.5 mm × 3.5 mm × 0.9 mm QFN Package

2.1.3 DAC161S997

- 16-bit resolution
- Very-low supply current of 100 µA
- 5 ppmFS / °C gain error
- Pin-programmable power-up condition
- Loop-error detection and reporting
- Programmable output-current error levels
- Simple HART modulator interfacing
- Highly integrated feature set in small footprint WQFN-16 (4- × 4-mm, 0.5-mm pitch)

2.1.4 OPA2342

- Low quiescent current: 150 µA typ
- Rail-to-rail input
- Rail-to-rail output (within 1 mV)
- Single supply capability
- Low cost
- *Micro*SIZE package options:
  - SOT23-5
  - MSOP-8
  - TSSOP-14
- Bandwidth: 1 MHz
- Slew rate: 1 V / µs
- THD + noise: 0.006%

2.1.5 TPS7A1601

- Wide input voltage range: 3 V to 60 V
- Ultra-low quiescent current: 5 µA
- Quiescent current at shutdown: 1 µA
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed-output voltage: 3.3 V, 5.0 V
  - Adjustable version from ~1.2 V to 18.5 V
- Power good with programmable delay
- Current-limit and thermal shutdown protections
- Stable with ceramic output capacitors: ≥ 2.2 µF
- Package: high thermal performance MSOP-8 PowerPAD™
- Operating temperature range: –40°C to +125°C

3 System Design Theory

This system comprises three main facets:

1. Precision measurement of an RTD
2. Analog communications via 4- to 20-mA current loop
3. Digital communications via HART-FSK superimposed on the current loop

Additionally, this design accounts for robust filtering of signals, precise calculations, and overall low active power.

3.1 4- to 20-mA Current Loop – At a Glance

Typically, a current loop system consists of four major components (as shown in Figure 5).

- Sensor (e.g. RTD temperature sensor)
- 4- to 20-mA current loop sensor transmitter
- Loop power supply
- Loop receiver

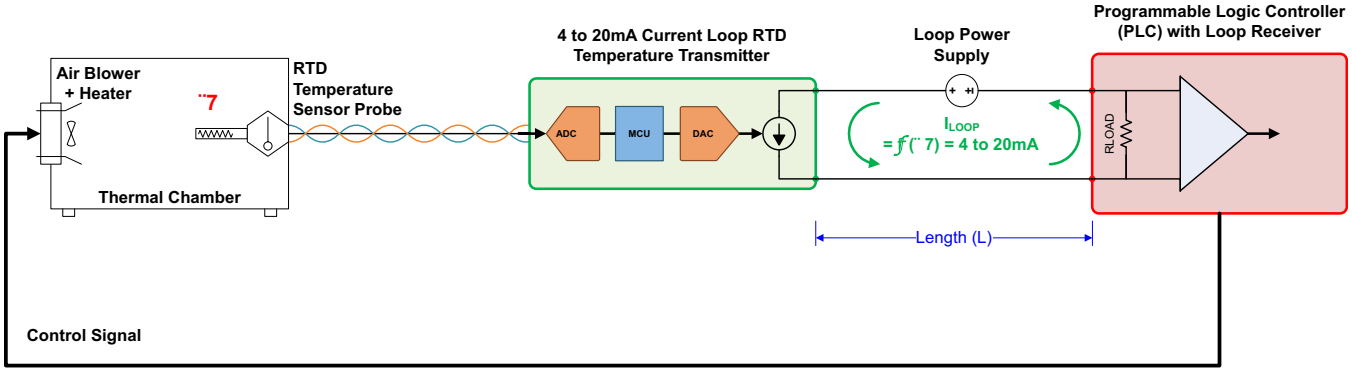


Figure 5. Typical Block Diagram of a Current Loop System

The sensor converts a physical parameter into an equivalent voltage output. In this case, the RTD and associated circuitry converts temperature into this voltage. By regulating the current drawn from the loop power supply, the sensor transmitter converts the sensor's output into a proportional 4- to 20-mA DC current. The zero-value process variable, which is the lowest possible sensed physical parameter of the sensor (-200°C), is represented by a current draw of 4 mA. The full-scale process variable, which is the highest possible sensed physical parameter of the sensor (850°C), is represented by a current draw of 20 mA. This 16-mA span represents the entire spectrum of the sensor's information range. The current returns to the power supply after flowing through a precision-load resistor of the loop resistor. This current is translated back into a voltage that is easily measured by the analog-input module of the programmable logic controller (PLC) system and processed further.

3.2 HART-FSK—At a Glance

The HART Protocol is a digital solution to transforming sensor transmitters into intelligent field devices. This protocol superimposes digital signals atop the analog 4- to 20-mA current loop system, enabling two-way communication to take place and allowing additional information to be passed from the field transmitter to the PLC system.

The HART protocol makes use of the Bell 202 Frequency Shift Keying (FSK) standard. This standard communicates at 1200 bps and shifts between tones of 1200 Hz and 2200 Hz. As Figure 6 shows, a cycle of 1200 Hz represents a logic "1" or a "mark" in the protocol, while a cycle of 2200 Hz represents a logic "0" or a "space" in the protocol. This communication is phase continuous, so there is no interference with the 4- to 20-mA signal.

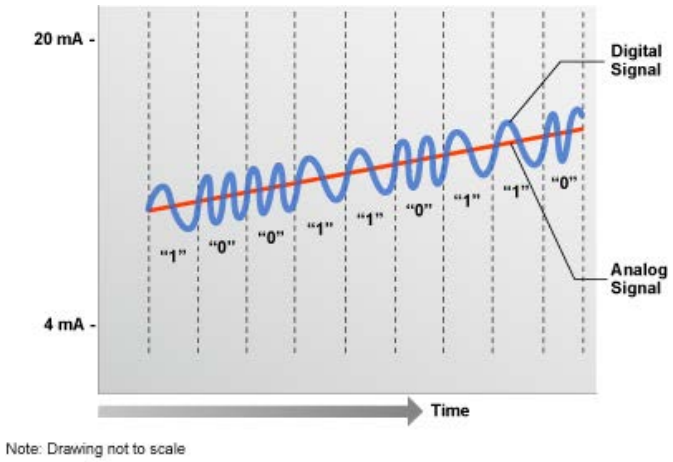


Figure 6. HART Frequency Shift Keying [2]

The HART protocol provides two channels of simultaneous communication. The 4- to 20-mA analog current signal (as described in the previous section) communicates the primary measured value. The digital signal (the HART-FSK) contains information from the device including device status, diagnostics, additional measured or calculated values, and more. Together, these communication channels provide a robust, low-cost field communication solution that is easy to use and configure.

HART technology runs on a master-slave protocol. This means that a smart field (slave) device, such as the one described in this design, will only speak when spoken to by a master device. HART communication occurs between two HART-enabled devices, typically a smart field device and a control system (PLC, for example). The HART protocol provides for up to two masters (primary and secondary), which allows secondary masters such as handheld communicators to be used without interfering with communications to or from the primary master device. Additionally, the HART protocol permits digital communication in either point-to-point or multidrop network configurations.

For more details on how HART works and its specifications, please refer to the HART Communication Foundation website.

3.3 RTD Overview and the Callendar-Van Dusen Equation

An RTD is a thin-metal-film element whose resistance characteristics are predictable over temperature. Therefore, the temperature of an RTD is calculated by measuring the RTD's resistance. RTD sensors are chosen for their wide temperature ranges, good linearity, and excellent long-term stability and repeatability, which makes an RTD an ideal candidate for precision temperature measurement applications.

Most RTD applications use a current source as an excitation for the RTD element. By driving a known current through the RTD, a voltage potential is created that is proportional to the resistance of the RTD and the excitation current, per Ohm's Law. This voltage is then amplified and then fed into the inputs of an ADC. The ADC converts this analog voltage into a digital output code that can be used to calculate the resistance value of the RTD. A simplified circuit for RTD sensing is shown in Figure 7.

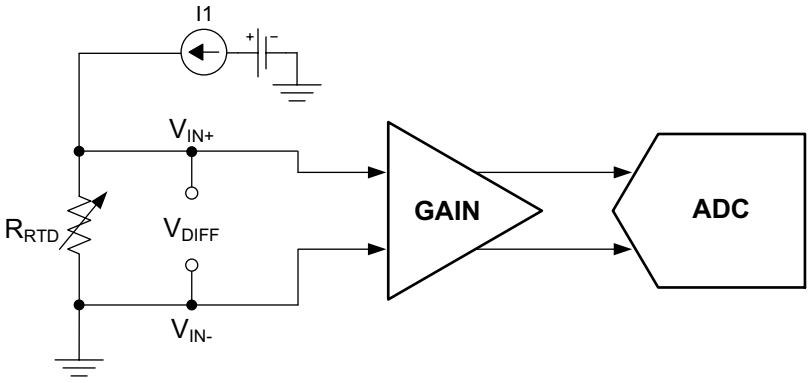


Figure 7. Simplified RTD Application Circuit

The basic principle for RTD operation is that all metals exhibit a positive change in resistance with increase in temperature. Metals which have high resistivity, high melting point, and high corrosion resistance are generally preferred for making RTDs. These characteristics equate to the stipulation that a high-nominal resistance value can be achieved with less material. Platinum is by far the best material for RTDs due to its high resistivity and long term stability. Platinum also follows a very linear resistance-temperature relationship compared to other metals. Additionally, as a noble (chemically inert) metal, platinum is less susceptible to contamination. Platinum is one of the leading choices for metal for temperature measurement applications. A PT100 RTD has a nominal resistance of 100 Ω at 0°C and an approximate change of 0.385 Ω per 1°C change in temperature. This impedance results in 18.52 Ω at –200°C and 390.481 Ω at 850°C. However, higher-valued RTDs such as PT200, PT500, or PT1000 can be used for increased sensitivity and resolution at little extra cost.

Class-A RTDs are a good choice for this application to provide good pre-calibration accuracy and long-term stability. A Class-A RTD has less than 0.5°C of error at 100°C without calibration, and the long-term stability makes accurate and infrequent calibration possible. Table 1 shows the tolerance, initial accuracy, and resulting error at 100°C for the five main classes of RTDs.

Table 1. RTD Class Tolerance Information

TOLERANCE CLASS (DIN-IEC 60751)	TOLERANCE VALUES (°C)	RESISTANCE AT 0°C (Ω)	ERROR AT 100°C
AAA(1)	±(0.03 + 0.0005 × T)	100 ± 0.012	± 0.08
AA	±(0.01 + 0.0017 × T)	100 ± 0.04	± 0.27
A	±(0.15 + 0.002 × T)	100 ± 0.06	± 0.35
B	±(0.3 + 0.005 × T)	100 ± 0.12	± 0.8
C	±(0.6 + 0.01 × T)	100 ± 0.24	± 1.6

(1)AAA is not included in the DIN-IEC 60751 specification but is an industry-accepted tolerance for performance demanding applications.

The relationship between the resistance and temperature of platinum RTDs is defined by a nonlinear mathematical model known as the Callendar-Van Dusen (CVD) equation. The coefficients in the Callendar-Van Dusen equation are defined by the IEC-60751 standard.

For T > 0°C, the CVD equation is a second-order polynomial as given in Equation 1:

$$RTD(T) = R_0 \times \left[1 + A(T) + B(T)^2\right] \quad (1)$$

For T < 0°C, the CVD equation expands to a fourth-order polynomial as given in Equation 2:

$$RTD(T) = R_0 \times \left[1 + A(T) + B(T)^2 + C(T)^3(T - 100)\right] \quad (2)$$

The linear approximation model is as follows:

$$RTD(T) = R_0 \times [1 + \alpha(T)] \quad (3)$$

where

- T = Temperature of RTD element in °C
- RTD (T) = resistance of RTD element as a function of temperature
- R0 is the resistance of the RTD element at 0°C
- α = Sensitivity of RTD element = 0.00385 Ω / Ω / °C
- A = 3.9083×10^{-3} °C^{-1}
- B = -5.7750×10^{-7} °C^{-2}
- C = -4.1830×10^{-12} °C^{-4}

The behavior of resistance for PT100 RTD from –200°C to 850°C is shown in Figure 8.

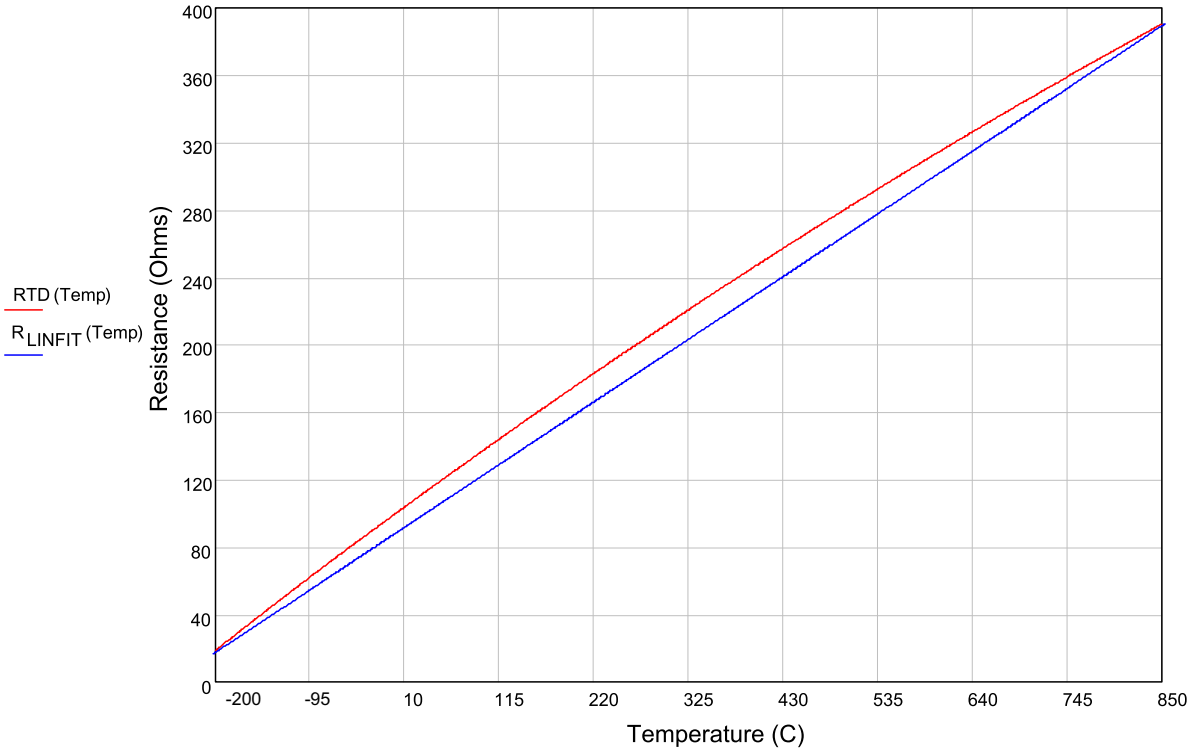


Figure 8. RTD Resistance and Linear Fit Line versus Temperature

The change in RTD resistance is piecewise linear over small temperature ranges. An endpoint curve fitting shows RTDs have second order non-linearity of approximately 0.375% as shown in Figure 9. Therefore, it is necessary to implement a digital linearization technique to correct this nonlinearity error. Table 2 compares three digital linearization techniques.

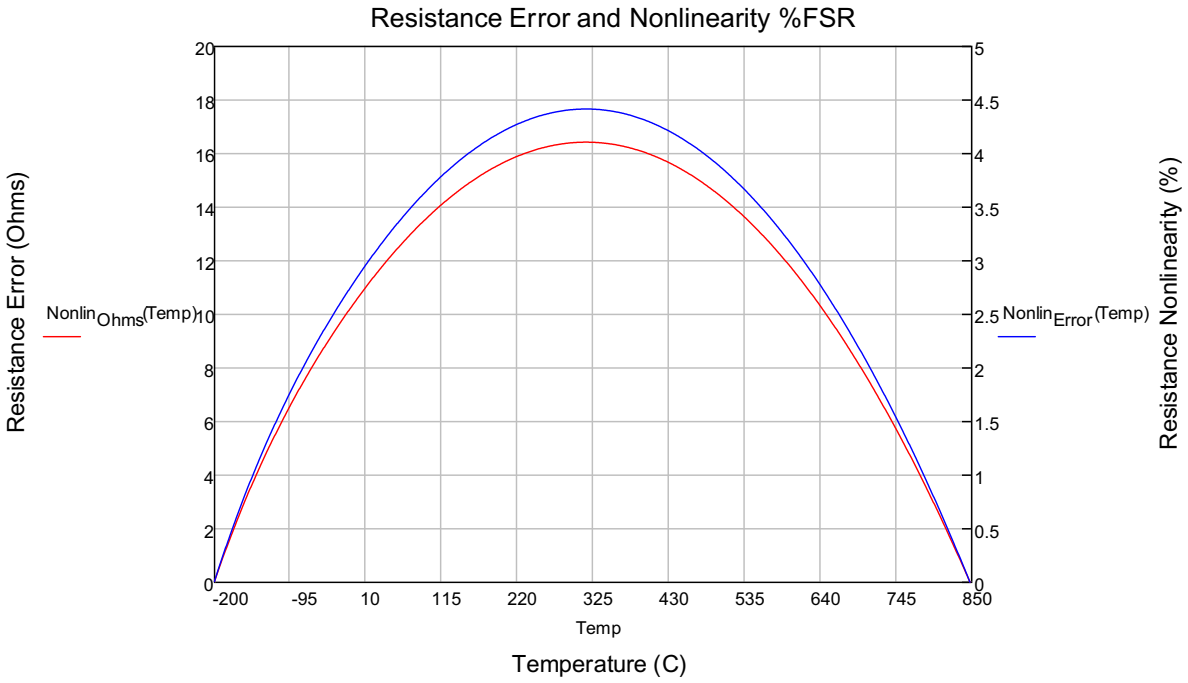


Figure 9. PT100 RTD Nonlinearity from –200°C to 850°C

Table 2. Comparison of Linear Approximation Methods

METHOD	ADVANTAGE	DISADVANTAGE	OTHER REMARKS
Simple Linear Approximation	Easy to implement Fast execution Accurate over small temperature ranges Smaller code size	Least accurate over wide temperature range	Simple method when memory size is limited and temperature range is smaller
Piecewise Linear Approximation	Accuracy depends on the entries in the lookup table Fast execution	High accuracy More entries in lookup table Bigger code size	Most practical method implemented by most embedded systems
Callendar-Van Dusen Equation	Most Accurate	Extremely processor intensive Time consuming Requires complex mathematical calculations	Not practical in most applications

In this reference design, a look-up table with a resolution of 1°C is used for a piecewise linear approximation solution. The RTD value is computed after offset and gain calibration. Then the RTD value calculated using a linear interpolation of the two adjacent values in the look-up table. If additional accuracy is desired, a table with higher precision (more points) may be used.

3.4 ADC Operation (3-Wire RTD Measurement)

The first focus of this reference design is the analog front end, the ADS1220. The ADS1220 integrates all required features (current source for sensor excitation, buffered reference inputs, PGA, and more) to ease the implementation of proper ratiometric 2-, 3-, and 4-wire RTD measurements.

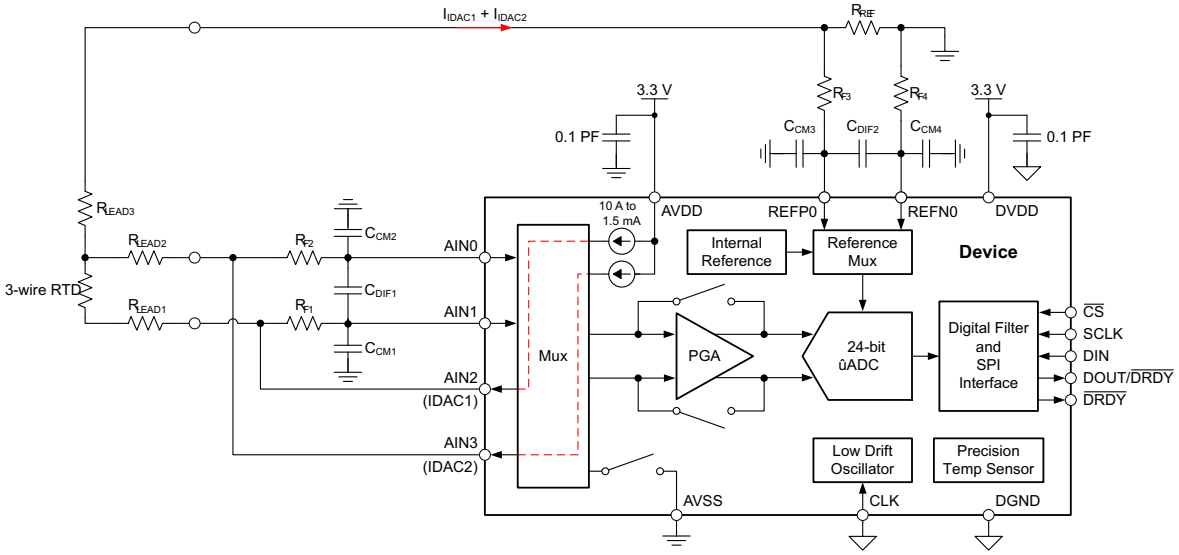


Figure 10. 3-Wire RTD Measurement

The circuit in Figure 10 depicts such a ratiometric approach for measuring a 3-wire RTD. In other words, the sensor signal (voltage across the RTD) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise cancel out because these errors are common to both the sensor signal and the reference.

To implement a ratiometric 3-wire RTD measurement, the ADS1220 provides two integrated digital-to-analog converter (IDAC) current sources capable of outputting currents from 10 µA to 1.5 mA. IDAC1 is routed to one of the excitation leads of the RTD. IDAC2 is routed to the second excitation lead as shown in Figure 10. By setting the corresponding IxMUX [2:0] configuration bits in configuration register 0x03, each IDAC is routed to the appropriate excitation lead. Both currents have the same value, which is programmable via the IDAC [2:0] configuration bits in configuration register 0x02.

The design of the ADS1220 ensures that both IDAC values are closely matched, even across temperature. The excitation current of 1 mA or less is generally preferred for industrial applications in order to minimize the error due to self-heating. In this application, each IDAX is programmed for an excitation current of 250 µA.

The sum of both currents, 500 µA, flows through a reference resistor, R_{REF}. The voltage developed across R_{REF} is fed into the positive and negative reference pins (REFP0 and REFN0) of the ADS1220, which is configured to use this voltage V_{REF} for the analog-to-digital conversions. The R_{REF} resistor and excitation current are sized to produce an external reference of mid-supply (AVDD + AVSS) / 2.

$$\text{ADC CODE} \propto \frac{V_{RTD} \times PGA_{GAIN}}{V_{REF}} \tag{4}$$

$$\text{ADC CODE} \propto \frac{V_{RTD} \times PGA_{GAIN}}{2 \times V_{REF}} \tag{5}$$

From Equation 5, it is apparent that the accuracy of the measurement depends on the reference resistor. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter. However, because the value of the reference resistor directly impacts the measurement result, the accuracy can be set to a higher level by choosing a high-precision, low-drift reference resistor R_{REF}.

3.4.1 Selecting R_{REF}

The following equations show the process of selecting the value for R_{REF} for this reference design.

$$V_{REF} = (IDAC1 + IDAC2) \times R_{REF} \quad (6)$$

Because IDAC1 = IDAC2 = 250 µA,

$$V_{REF} = (2 \times IDAC) \times R_{REF} \quad (7)$$

If AVDD = 3.3 V and AVSS = 0 V, we desire V_{REF} = 3.3 V / 2 = 1.67 V, giving

$$R_{REF} = \frac{V_{REF}}{(2 \times IDAC)} = \frac{1.67\ V}{500\ \mu a} = 3.34\ k\Omega \quad (8)$$

3.4.2 Selecting PGA Gain

The voltage produced across the RTD needs to be amplified by the PGA prior to reaching the ΔΣ for conversion. The gain should be chosen so that ADC input signal is still less than V_{REF} at maximum RTD temperature. The largest possible gain will yield the best resolution per °C.

R_{RTD} at 850°C = 390.48 Ω, giving

V_{RTD} at 850°C = 390.48 Ω × 250 µA = 97.62 mV, thus

$$PGA_{GAIN} = \frac{V_{REF}}{V_{RTD}\ \text{at}\ 850°C} = \frac{1.62\ V}{97.62\ mV} = 16.6\ V / V \quad (9)$$

The closest PGA setting to this value is 16 V / V.

3.4.3 Common Mode Voltage Compliance Check

The allowed common-mode input voltage range is specified in the ADS1220 datasheet and copied to Figure 11.

ANALOG INPUTS			
Full-scale input voltage (V_{IN} = ADCINP – ADCINN)		$\pm V_{REF}/PGA$ (1)	V
Common-mode input range		$AVSS + 0.2\ V + \frac{(V_{IN})(Gain)}{2}$ $AVDD - 0.2\ V - \frac{(V_{IN})(Gain)}{2}$	V

Figure 11. Specification for Common Mode Input Range

Calculating for the highlighted equation in Figure 11, the maximum and minimum limits equate to

$$AVSS + 0.2\ V + \frac{(V_{IN})(PGA\_GAIN)}{2} \le V_{CM} \le AVDD + 0.2\ V + \frac{(V_{IN})(PGA\_GAIN)}{2}$$

$$0\ V + 0.2\ V + \frac{0.09762\ V \times 16\ V / V}{2} \le V_{CM} \le 3.3\ V + 0.2\ V + \frac{0.09762\ V \times 16\ V / V}{2}$$

$$0.981\ V \le V_{CM} \le 2.32V \quad (10)$$

Applying the actual common-mode input voltage generated by the reference design shows the following:

$$V_{CMI} = (IDAC \times R_{LEAD}) + \frac{IDAC \times R_{RTD}}{2} + 2 \times IDAC \times (R_{LEAD} + R_{REF}) \quad (11)$$

Assuming R_{LEAD} = 10 Ω,

V_{CMI} with R_{RTD} @ -200°C ≤ V_{CMI} ≤ V_{CMI} with R_{RTD} @ 850°C

$$1.63\ V \le V_{CM} \le 1.68\ V \quad (12)$$

This result is well within the maximum allowed common-mode input voltage range.

3.4.4 Excitation Current Compliance Voltage Check

When designing the circuit, take care to meet the compliance-voltage requirement of the IDACs. The IDACs require a minimum headroom of (AVDD – 0.9 V) to operate accurately.

EXCITATION CURRENT SOURCES (IDACs)			
Current settings		10, 50, 100, 250, 500, 1000, 1500	µA
Compliance voltage	All currents	AVDD – 0.9	V

Figure 12. Specification for Excitation Current Source Compliance Voltage

For IDAC1:

$$AVSS + [IDAC1 \times (R_{LEAD1} + R_{RTD})] + [(IDAC1 + IDAC2) \times (R_{LEAD3} + R_{REF})] + V_{DIODE} \leq AVDD - 0.9\ V \quad (13)$$

2.12512 V ≤ 2.4 V

For IDAC2:

$$AVSS + [IDAC2 \times (R_{LEAD1} + R_{RTD})] + [(IDAC1 + IDAC2) \times (R_{LEAD3} + R_{REF})] + V_{DIODE} \leq AVDD - 0.9\ V \quad (14)$$

2.12512 V ≤ 2.4 V

This means that the excitation current compliance voltages for IDAC1 and IDAC2 are met.

3.4.5 Analog Input and Reference Low-Pass Filter Design

RTD voltage output signal is typically in the millivolt range, which makes the signals susceptible to noise. First-order differential and common-mode RC filters (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) are placed on the ADC inputs and on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and C_{CM4}) to eliminate high-frequency noise in RTD measurements. The differential cut-off frequency of the analog-input filter must be designed to be at least ten times higher than the ADC bandwidth at the selected data rate. The cut-off frequency chosen for this design is higher to account for a faster sampling rate.

If the corner frequencies are not matched, noise appearing on analog input will be different from noise on the reference, which will not get cancelled in ratiometric measurement. For best performance, match the corner frequencies of the analog-input and reference low-pass filters. For more details on how to match corner frequencies of analog input and reference filters, refer to *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* (SBAA201).

3.4.6 Excitation Current Chopping

The two current sources must be perfectly matched to successfully cancel the lead resistance of the RTD wires. While initial matching of the current sources is important, any remaining mismatch in the two sources can be minimized by swapping (or chopping) the two current sources between the two inputs. Taking a measurement in both configurations and averaging the two readings will greatly reduce the effects of mismatched current sources (see Equation 13 and Equation 14). Realizing current chopping technique could become possible by the use of an integrated, digitally-controlled input multiplexer inside the ADS1220.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITATION CURRENT SOURCES (IDACs)					
Current settings			10, 50, 100, 250, 500, 1000, 1500		µA
Compliance voltage	All currents			AVDD – 0.9	V
Accuracy	All currents, each IDAC	–6%	±1%	6%	
Current match	Between IDACs (not valid for 10-µA setting)		±0.3%		
Temperature drift	Each IDAC (not valid for 10-µA setting)		50		ppm/°C
Temperature drift matching	Between IDACs (not valid for 10-µA setting)		10		ppm/°C

Figure 13. Specification for Excitation Current Source Mismatch and Temperature Drift

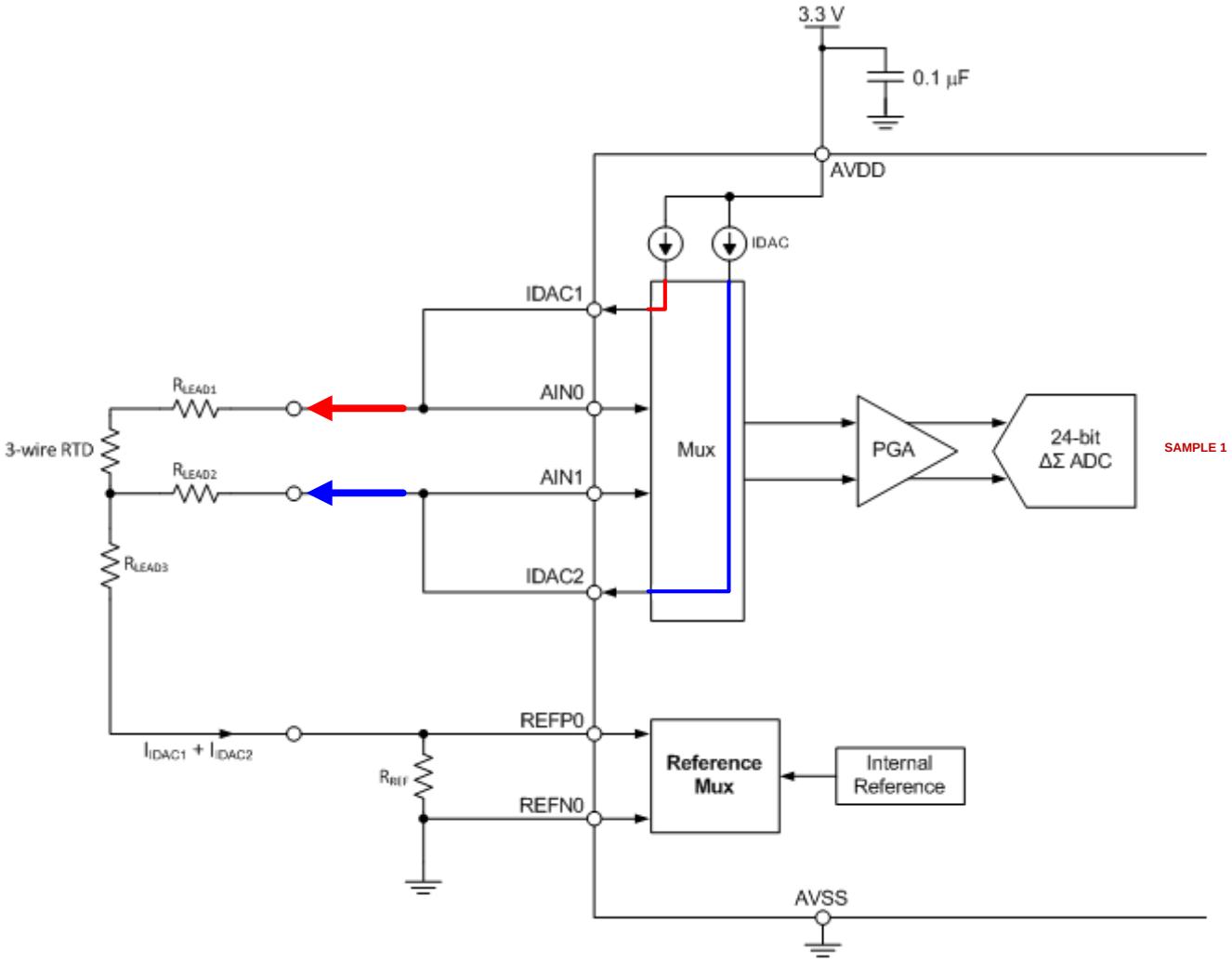


Figure 14. Measurement Before Excitation Current Swap

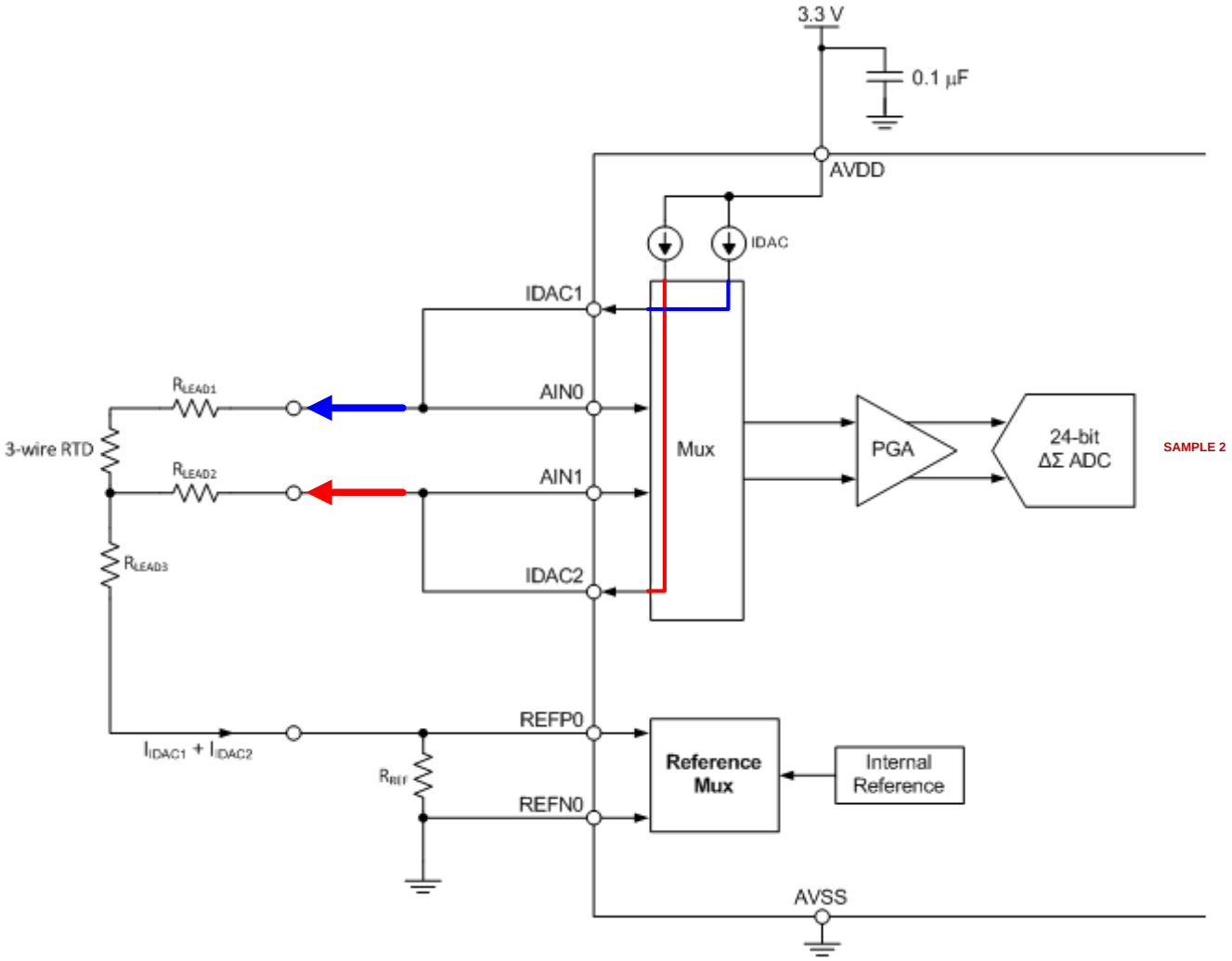


Figure 15. Measurement After Excitation Current Swap

$$\text{IDAC Mismatch Corrected Reading} = \frac{\text{SAMPLE 1} + \text{Sample 2}}{2} \quad (15)$$

3.5 MCU Operation

The MCU is the brain of the entire sensor transmitter, and for more than one reason. The MCU manages all calculations and communications required for the analog 4- to 20-mA current loop representation of the primary variable (temperature in this design) and all digital communications to and from the HART master device. The MCU also runs the full HART Protocol stack.

3.5.1 Converting ADC Output Code to RTD Resistance (R_{RTD})

ADS1220 provides 24-bit data in binary twos to complement format. The positive full-scale input produces an output code of 7FFFFFh, and the negative full-scale input produces an output code of 800000h. The output clips at these codes are for signals that exceed full-scale (FS).

Table 3. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE
≥ +FS (2^{23} – 1) / 2^{23}	7FFFFFh
+FS / 2^{23}	000001h
0	0
–FS / 2^{23}	FFFFFFh
≤ –FS	800000h

$$1\ \text{LSB} = \frac{\text{Full Scale Range}}{(2^{24} - 1)} = \frac{2 \times \text{FS}}{(2^{24} - 1)} = \frac{2 \times V_{REF}}{\text{GAIN} \times (2^{24} - 1)} \tag{16}$$

In ratiometric measurement, $V_{IN} = R_{RTD} \times IDAC$ and $V_{REF} = 2 \times R_{REF} \times IDAC$, then

$$V_{IN} = 1\text{LSB} \times (\text{ADC\_CODE})_{DEC} = \frac{2 \times V_{REF} \times (\text{ADC\_CODE})_{DEC}}{\text{GAIN} \times (2^{24} - 1)} \tag{17}$$

$$R_{RTD} = \frac{4 \times R_{REF} \times (\text{ADC\_CODE})_{DEC}}{\text{GAIN} \times (2^{24} - 1)} \tag{18}$$

Where, R_{REF} = 3240 Ω and GAIN = 16 V / V

3.5.2 Converting R_{RTD} to Equivalent Temperature (T_{RTD})

To convert the resistance (R_{RTD}) to its equivalent temperature (T_{RTD}), a linear interpolation is required, which takes advantage of a look-up table characteristic of the RTD sensor. To perform a linear interpolation using a look-up table, first compare the measured R_{RTD} values with resistance values (R_{LT}) given in the look-up table, until the look-up table value exceeds the measured value that is being converted. Then, use Equation 19 to convert the measured R_{RTD} value to temperature value (T_{RTD}). This operation involves four additions, one multiplication, and one division step, respectively. This operation can be done easily on a 16-bit MSP430FR5969 MCU.

$$T_{RTD} = T_{LT[n-1]} + \left(R_{RTD} - R_{LT[n-1]}\right) \times \left[\frac{\left(T_{LT[n]} - T_{LT[n-1]}\right)}{\left(R_{LT[n]} - R_{LT[n-1]}\right)}\right] \tag{19}$$

3.5.3 Converting T_{RTD} to Equivalent DAC Input Code

To convert T_{RTD} to its equivalent DAC input code, first convert the temperature value (T_{RTD}) to its equivalent loop current using Equation 20 (see also Figure 21).

$$I_{LOOP} = 4\ \text{mA} + \left(T_{RTD} + 200°\text{C}\right) \times \left[\frac{16\ \text{mA}}{1050°\text{C}}\right] \tag{20}$$

Then, convert this loop current into the DAC input code using Equation 21.

$$I_{LOOP} = 24\ \text{mA} \times \left[\frac{\text{DAC\_CODE}}{2^{16}}\right] \tag{21}$$

To find out the relation between T_{RTD} and DAC_CODE, substitute the value of I_{LOOP} from Equation 20 in Equation 21,

$$DAC\_CODE = DEC2HEX\left[\frac{\left[4\,mA + (T_{RTD} + 200°C) \times \left[\frac{16\,mA}{1050°C}\right]\right] \times 2^{16}}{24\,mA}\right] \quad (22)$$

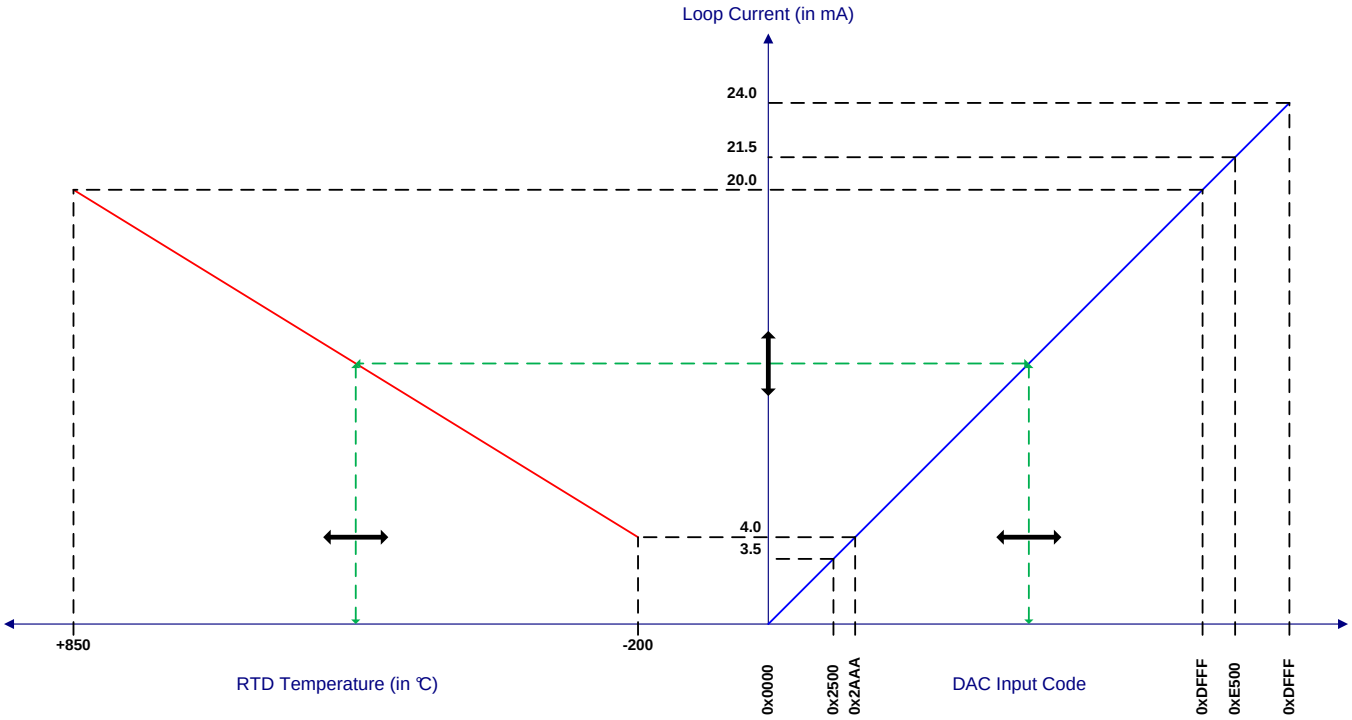


Figure 16. Mapping RTD Temperature to Loop Current to DAC Input Code

3.5.4 HART FSK Soft Modem

For HART FSK SoftModem design and documentation, please refer to *HART SoftModem and Protocol Stack* (Smart Embedded Systems).

3.5.5 HART Protocol Stack

Similarly, for HART Protocol Stack design and documentation, please refer to *HART SoftModem and Protocol Stack* (Smart Embedded Systems).

3.6 HART FSK Filtering

For HART communications, users must ensure that the FSK modulation output is compliant with the waveshape specifications in the HART FSK Physical Layer Specification. Users must also ensure that all received modulations are properly handled, and signals outside the digital FSK band are sufficiently suppressed.

3.6.1 FSK Modulation Filtering

To design for the HART Physical Layer Specification, an active filter was designed using the OPA2342 low-cost, low-power, rail-to-rail operational amplifier. This amplifier was used in the configuration shown in Figure 17. The resulting AC frequency response of the filter is shown in Figure 18. The pivotal aspects of this filter are two fold: ensuring that the amplitude response of the two FSK tones (1200 Hz and 2200 Hz) are as close as possible, and that all out-of-band noise >10 kHz is suppressed sufficiently.

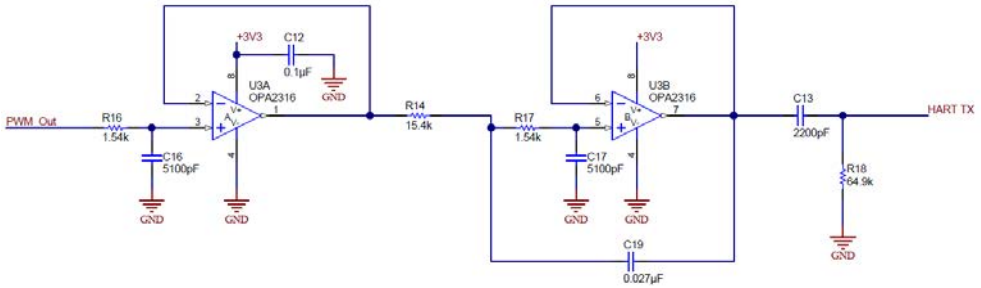


Figure 17. HART FSK Modulation Filter

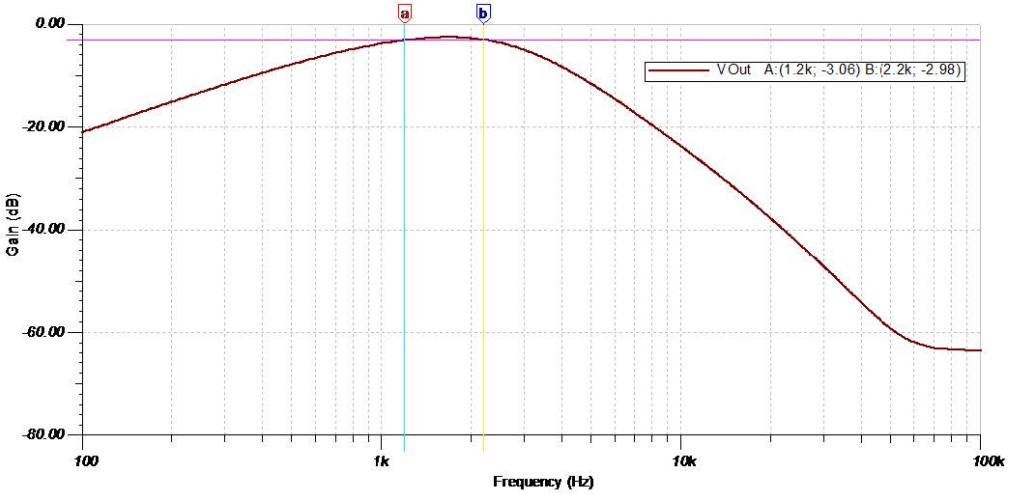


Figure 18. HART FSK Modulation Filter Frequency Response

3.6.2 FSK Demodulation Filtering

As with the modulation filter, the demodulation filter has two key components: ensuring the 1200-Hz and 2200-Hz bands have as similar attenuation as possible (and as little attenuation as possible), and that all out-of-band signals are sufficiently suppressed. One prime example of an out-of-band signal needing suppression is the +24-V DC carrier for the 4- to 20-mA current loop. It is thus imperative to have a high-pass filter stage in the demodulation filter.

For this filter design, a simple 2-stage RC bandpass filter was designed. The high-pass portion of this filter was biased up to ½ VCC to align the input to be demodulated with the center of the range of the ADC on the MSP430FR5969 MCU (ADC reference voltage is equal to VCC). The circuit diagram for this filter is shown in Figure 19, and its frequency response is shown in Figure 20.

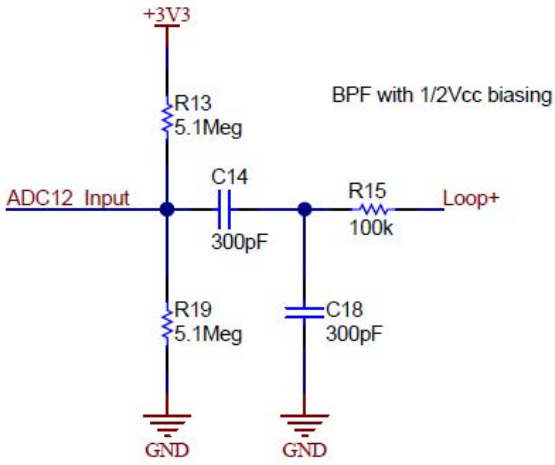


Figure 19. HART FSK Demodulation Filter

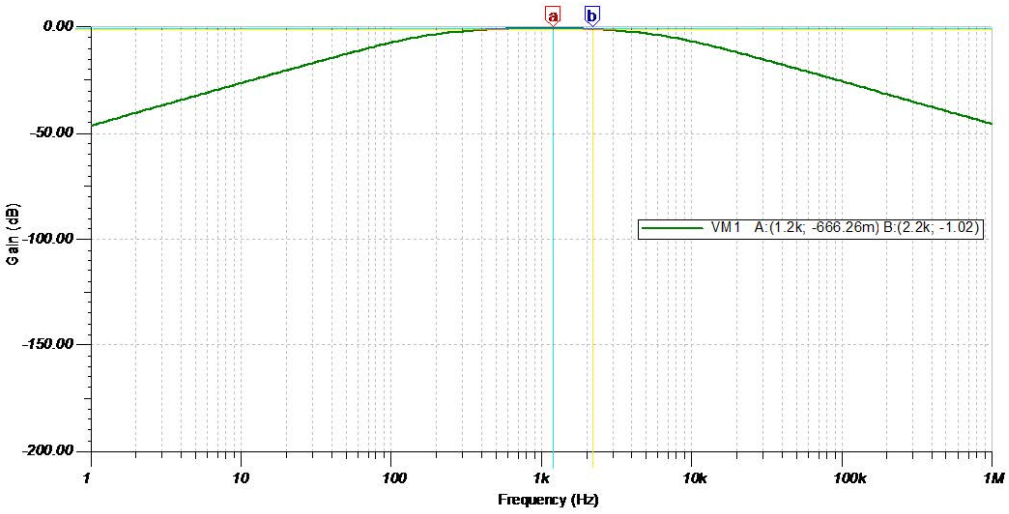


Figure 20. HART FSK Demodulation Filter Frequency Response

3.7 DAC Operation

Another focus of this reference design is the analog interface to the loop communications, the DAC161S997. This device converts a 16-bit input code in the DAC_CODE register to an equivalent current output over the loop. The ΔΣ DAC output is a current pulse that is then filtered by a third-order RC low-pass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin. Figure 21 shows the principle of operation of the DAC161S997 in the loop-powered transmitter. The I_{LOOP} has a number of component currents as given in Equation 23.

$$I_{LOOP} = I_{DAC} + I_D + I_A + I_E = 24\ mA \times \left[\frac{DAC\_CODE}{2^{16}}\right] \quad (23)$$

where

- I_{DAC} = f(DACCODE),
- I_D and I_A represent the supply currents of internal digital and analog blocks,
- I_{AUX} represents the supply current of companion devices present in the system,
- I_E is the only component which is regulated by the control loop to ensure that the actual loop current corresponds to the DAC input code applied by the MCU.

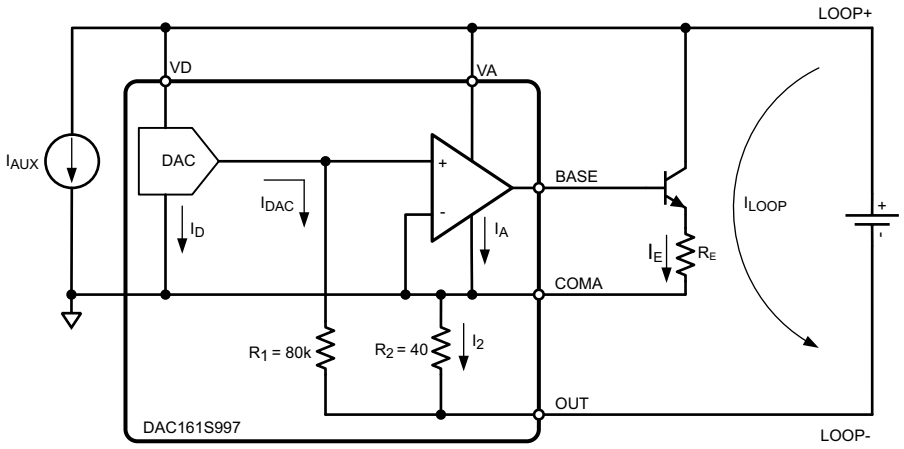


Figure 21. Loop-Powered Transmitter

3.7.1 Loop Compliance Voltage

To calculate the minimum-loop, compliance-voltage (loop-power supply voltage), add all voltage drops in the loop at the maximum-expected loop current.

From a current control loop stability point of view, $V_{CE\ (MIN)}$ must stay greater than maximum $V_{CE\ (SAT)}$:

$V_{CE\ (MIN)} > 0.2\ V$

Applying Kirchhoff's Voltage Law in the outer loop:

$$V_{CE\ (MIN)} = V_{(SUPPLY\ (MIN)} – (2 \times V_{WIRE}) - (2 \times V_F) - V_{RC\ (MAX)} - V_{ZENER} - V_{RE\ (MAX)} – V_{SENSE(MAX)} – V_{LOAD\ (MAX)} \quad (24)$$

where

- $2 \times V_{WIRE}$ is voltage drop across system wiring. If system wiring runs over a length (L) along one way, wire resistance per unit length is ρ and current in the loop is I_{LOOP}, then the voltage drop for one conductor can be given as
- $V_{WIRE\ (MAX)} = \rho \times L \times I_{LOOP\ (MAX)}$
- For example, a 24-AWG wire has resistance per unit length (ρ) of 0.026 Ω / ft or 0.0755 Ω / m.
- V_{LOAD} is the voltage drop caused by the internal resistance of the loop receiver. The internal resistance of the loop receiver may vary from 50 Ω to 250 Ω.
- $V_{LOAD\ (MAX)} = R_{LOAD} \times I_{LOOP\ (MAX)}$
- V_{SENSE} is the voltage drop across 40-Ω sense resistor internal to the DAC.
- V_F is the forward-voltage drop across the reverse polarity protection diode.
- V_F = 0.7 V at 30 mA forward current.

Rewriting Equation 24,

$$V_{SUPPLY(MIN)} > 0.2V + (2 \times \rho \times L \times I_{LOOP(MAX)}) + (2 \times 0.7V) + (100\Omega \times I_{LOOP(MAX)}) + 3.9V + (20\Omega \times I_{LOOP(MAX)}) + (40\Omega \times I_{LOOP(MAX)}) + (R_{LOAD} \times I_{LOOP(MAX)}) + (40\Omega \times I_{LOOP(MAX)}) + (R_{LOAD} \times I_{LOOP(MAX)}) \quad (25)$$

The maximum output current that can be sourced out of the OUT pin by DAC161S997, $I_{LOOP\ (MAX)}$, is approximately 24 mA.

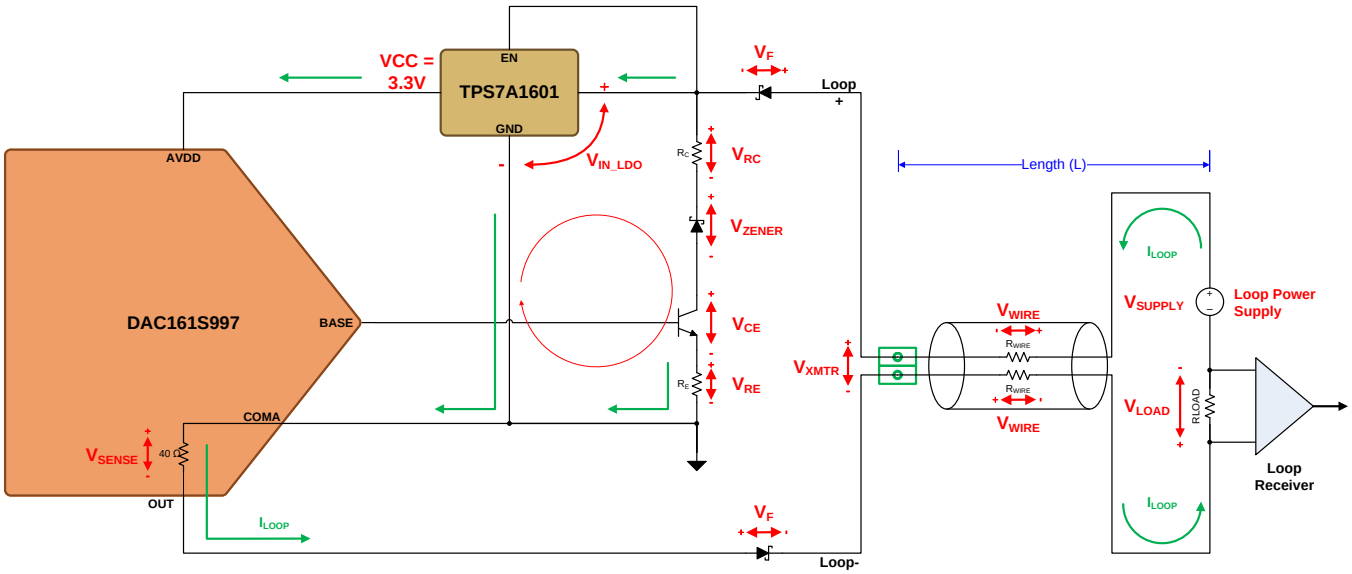


Figure 22. Series Voltage Drops in Current Loop System

LOOP CURRENT OUTPUT (OUT)				
I_{OUTMIN}	Minimum output current	Tested at DACCODE = 0x01C2 (7)	0.19	mA
I_{OUTMAX}	Maximum output current	Tested at DACCODE = 0xFFFF	23.95	mA
R_{OUT}	Output impedance		200	MΩ
	COMA to OUT voltage drop	I_{OUT} = 24 mA	960	mV

Figure 23. Specification for Loop Current Output

Next, examine what NAMUR NE43 has to say about loop current. NAMUR NE43 is an international association of process instrumentation user companies that have worked on improving the diagnostic coverage in 4- to 20-mA analog output transmitters to address associated safety issues. NAMUR NE43 provides the guideline for signaling-failure information to the safety-interlock systems over a 4- to 20-mA loop. NAMUR NE43 recommends using 3.8 mA to 20.5 mA as an extended measurement information range. NAMUR NE43 recommends using loop current below 3.6 mA or above 21 mA is in the diagnostic failure information range. Choose $I_{LOOP\ (MAX)}$ = 24 mA, depending upon DAC capability and also to comply with the NAMUR NE43 recommendation as shown in Figure 24.

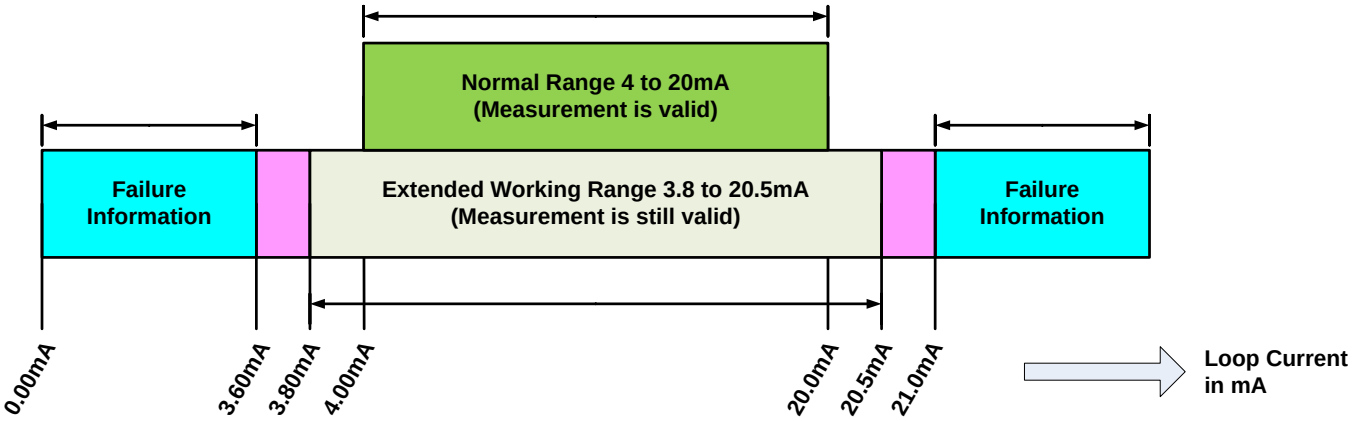


Figure 24. NAMUR NE43 Recommendation

Re-writing Equation 25,

$$V_{SUPPLY(MIN)} > 0.2V + (2 \times \rho \times L \times 24\ mA) + (2 \times 0.7V) + (100\Omega \times 24\ mA) + 3.9V + (20\Omega \times 24\ mA) + (40\Omega \times 24\ mA) + (R_{LOAD} \times 24\ mA) + (40\Omega \times 24\ mA) + (R_{LOAD} \times 24\ mA) \quad (26)$$

$$V_{SUPPLY\ (MIN)} > 2 \times 0.026\ \Omega / ft \times L \times 24\ mA) + (R_{LOAD} \times 24\ mA) + 9.34\ V \quad (27)$$

Figure 25 and Figure 26 give the loop supply voltages calculated using Equation 27 at different receiver load resistances and system wiring lengths.

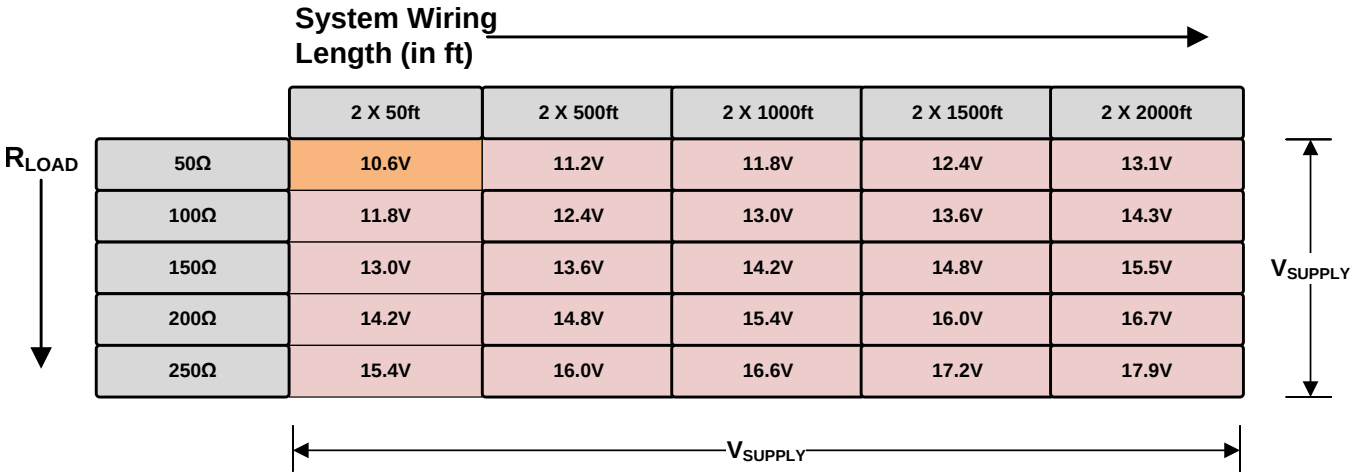


Figure 25. Loop Power Supply Voltage for Different Loads and System Wiring Length in Feet

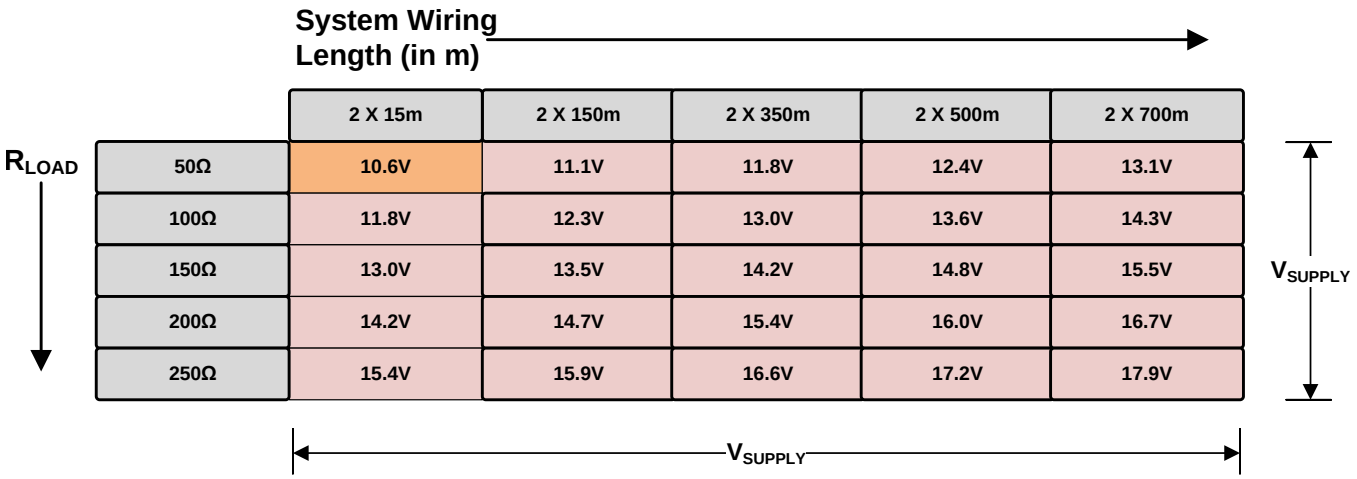


Figure 26. Loop Power Supply Voltage for Different Loads and System Wiring Length in Meters

However, the maximum loop compliance voltage must not exceed the absolute maximum voltage rating of any device used in the loop. Therefore, select the device in order to meet the maximum loop compliance voltage requirement.

3.7.2 Selection of External BJT

The DAC161S997 has been designed to use an external NPN bipolar junction transistor (BJT). Transistor Q1 conducts the majority of the signal-dependent, 4- to 20-mA loop current. Using an external transistor avoids on-chip power dissipation and thermally-induced errors. Since the external transistor is part of a current control loop, the external transistor characteristics are not critical. Virtually any transistor with sufficient voltage, current, and power rating may be used. Basic requirements are as follows:

- $V_{CEO} \geq 40$ V
- $\beta \geq 40$
- Must be able to handle power dissipation, $P_D = V_{CE\ (MAX)} \times I_{LOOP\ (MAX)}$

The NPN BJT should not be replaced with an N-channel field effect transistor (FET) for the following reasons:

- Discrete FETs typically have high threshold voltages (V_{TH}), in the order of 1.5 V to 2 V, which is beyond the BASE output maximum range
- Discrete FETs present higher load capacitance, which may degrade system stability margins. BASE output relies on the BJT's base current for biasing

3.8 Power Design

The TPS7A16xx family of ultra-low power voltage regulators offers the benefit of ultra-low quiescent current, high-input voltage, and miniaturized, high-thermal performance packaging. The TPS7A16xx family LDOs accept a maximum input voltage of 60 V, which makes these LDOs ideal for use in industrial applications where high-voltage transients are present. The TPS7A1601 has an adjustable output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors R_8 and R_{12}, as shown in Figure 27. To set LDO output voltage, V_{CC} = 3.3 V, the resistor divider components are calculated using Equation 28.

$$R_{14} = R_{18} \times \left[\frac{V_{CC}}{V_{REF}} - 1 \right] \tag{28}$$

where

- V_{REF} = LDO Internal Reference Voltage = 1.193 V (typical)
- The selected values are R_8 = 22.1 kΩ and R_{12} = 12.4 kΩ

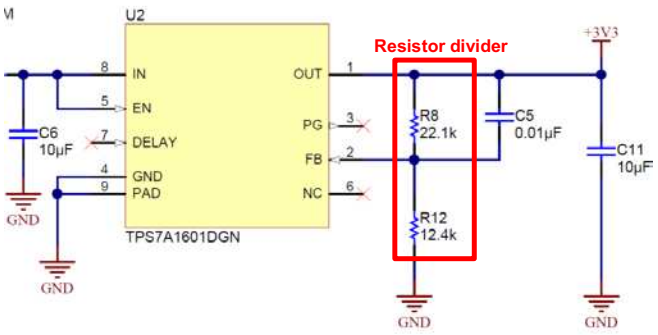


Figure 27. LDO Circuit with Feedback for Adjustable Output

The maximum power dissipation within the LDO is given by Equation 29.

$$P_D = (V_{IN\_LDO} - V_{CC}) \times I_Q \tag{29}$$

Assume a worst-case scenario where the entire maximum loop power supply voltage, $V_{SUPPLY\ (MAX)}$ = 33 V, appears across the LDO input. The maximum allowed I_Q = 3.3 mA.

$$P_D = (33\ V - 3.3) \times 3.3\ mA = 98.01\ mW \tag{30}$$

The junction-to-ambient thermal resistance, θ_{JA}, of the TPS7A1601 device is 44.5°C / W.

For safe operation: $\theta_{JA} \times P_D + T_{A\ (MAX)} < T_{J\ (MAX)}$

The maximum junction temperature before the TPS7A1601 device shuts down is 170°C. From Equation 30, the worst case junction temperature of TPS7A1601 device is approximately 90°C, assuming an ambient temperature of 85°C. Therefore, a sufficient thermal-operating margin is available with the TPS7A1601 device, even accounting for the worse-case power dissipation.

3.9 Protection

3.9.1 Protection for IEC61000-4

The design uses a local transient-voltage suppressor (TVS) diode and a bypass capacitor to reduce voltage spikes to lower, more manageable voltages to be in compliance with IEC61000-4 requirements.

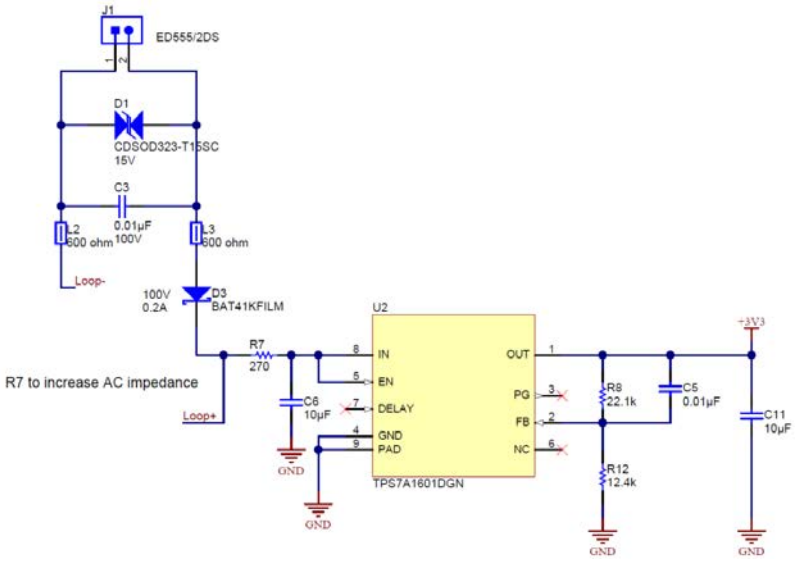


Figure 28. Protection Circuit Schematic

3.9.2 Reverse Polarity Protection

To protect the system from accidently connecting the power to the board in reverse polarity, two protection diodes are used: one in the path of Loop+ and another in Loop– as shown in Figure 29. The diodes must have a reverse-voltage rating higher than the maximum clamping-voltage of the TVS in the event of high-voltage transient.

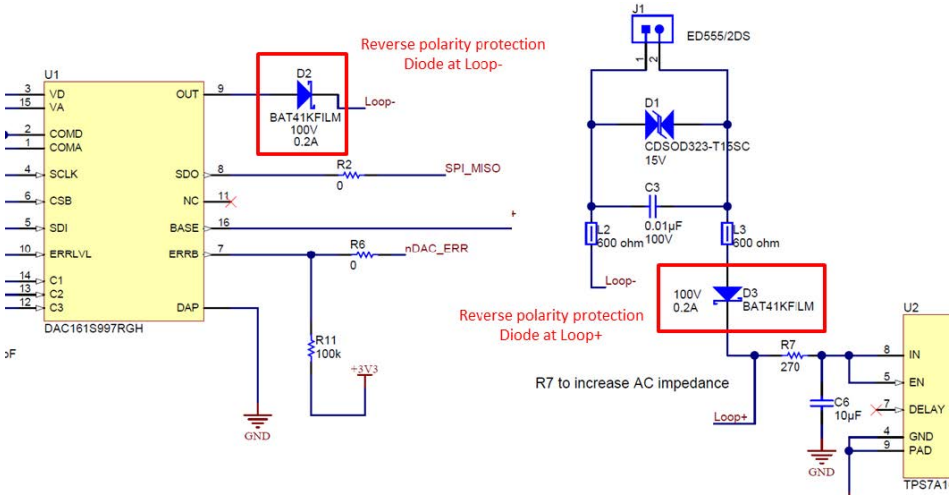


Figure 29. Reverse Polarity Protection using Schottky Diodes

4 Getting Started Hardware

This TI Design was built on the TI LaunchPad standard, and all BoosterPacks also align with this standard so that all hardware can be used across LaunchPad platforms. This section of the document will go through all facets of the hardware platform, both LaunchPads and BoosterPacks and highlight key facets of the design which will aid in getting started developing with this solution.

4.1 MSP-EXP430FR5969 LaunchPad Hardware Overview

The MSP-EXP430FR5969 is a development platform which leverages the MSP430 ultra-low-power (ULP) microcontrollers with embedded Ferroelectric Random Access Memory (FRAM) technology. It is an easy-to-use evaluation module which features on-board emulation for programming and debugging applications, as well as buttons and LEDs for quick integration of user interface. For this design, the main focus is on the power jumpers and the jumpers from the emulation side of the board to the target side of the board. Figures 30-32 display the proper jumper connections for the MSP-EXP430FR5969 LaunchPad for the three cases that may be encountered:

- Programming or debugging the device while not loop powered
- Programming or debugging the device while loop powered
- Running the application off loop power (normal operation)

Because this design is meant to be loop powered, the target device should derive all of its power from the DC carrier for the current loop. To ensure that the emulator is not powered (which will cause errors in the analog signal path), jumpers J9 (current sense jumper) and J10 (Power Select) should be modified as shown in Figure 31. Specifically, J9 should be disconnected, and J10 should be switched to the “External” selection.

Additionally, further disconnections should be made between the emulation and target sides of the LaunchPad via the jumpers on J13. These nine jumpers constitute the power, GND, UART, and SPI bi-wire JTAG connections between the two sides of the board. As a generalization for this design, all of these jumpers should be disconnected during normal operation. Only during programming and debugging should any of these jumpers remain connected. In these cases, test (TST) and reset (RST) are the only two which require population.

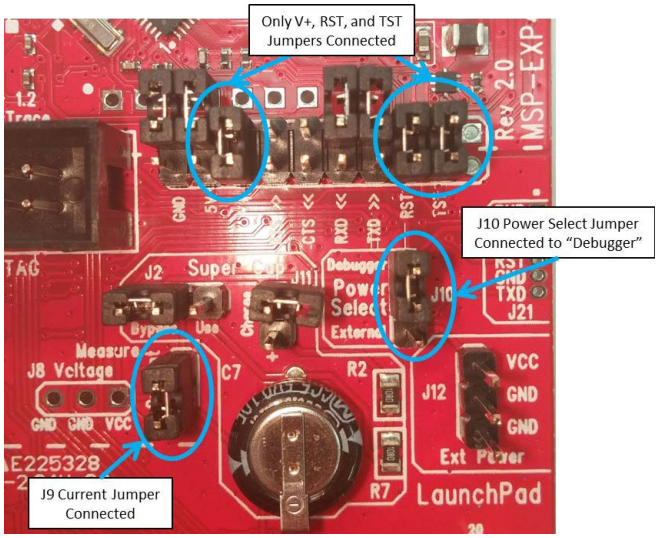


Figure 30. LaunchPad Jumper Configuration—Programming While NOT Loop Powered

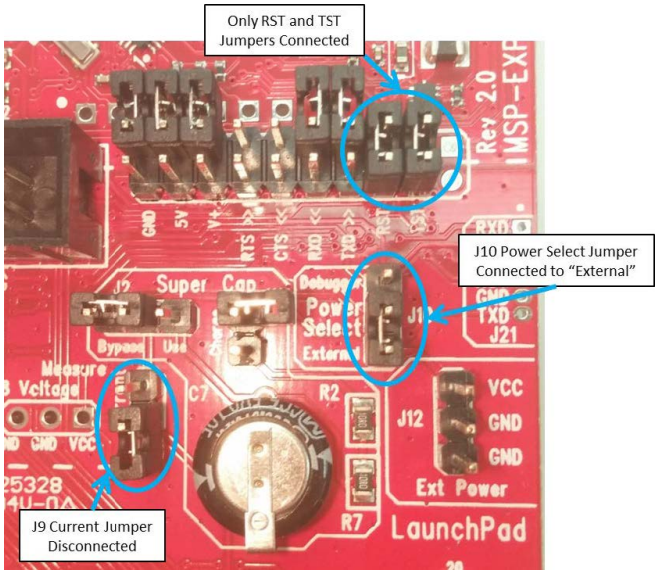


Figure 31. LaunchPad Jumper Configuration—Programming While Loop Powered

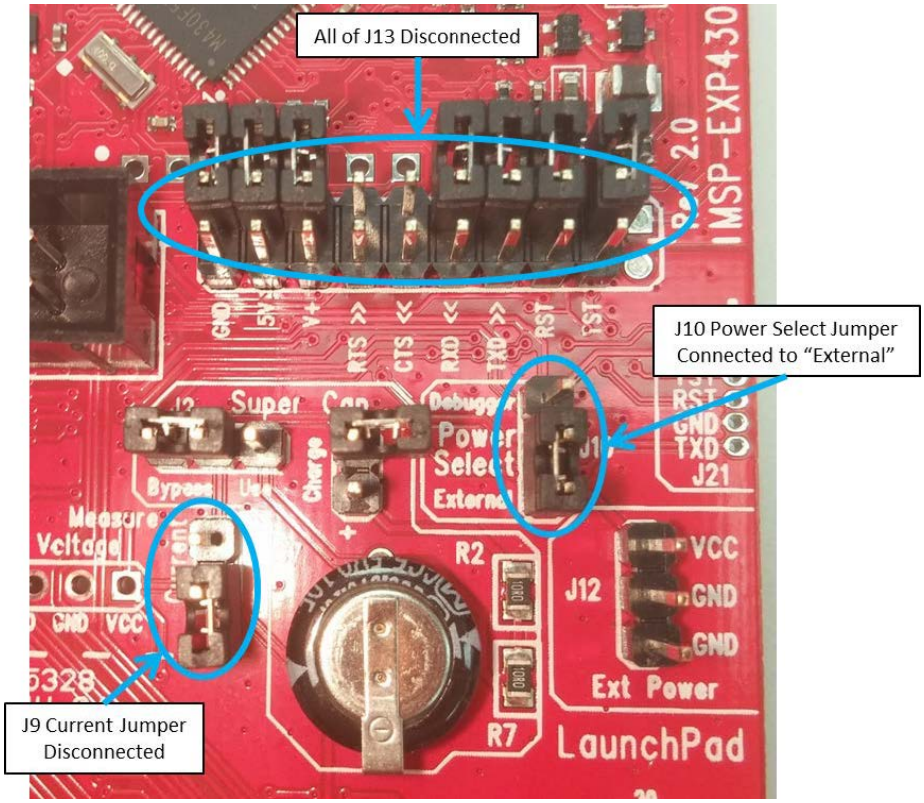


Figure 32. LaunchPad Jumper Configuration—Running Application on Loop Power (Normal Operation)

For more extensive detail on the MSP-EXP430FR5969 LaunchPad development board and jumper locations, please refer to the corresponding *MSP-EXP430FR5969 LaunchPad Development Kit User's Guide* (SLAU535a).

4.2 ADS1220 RTD BoosterPack Hardware Overview

The ADS1220 RTD BoosterPack, as stated previously, is focused on the sensor side (front-end) of the solution. To achieve this, the BoosterPack requires connections to the SPI module and two general purpose input/output pins (GPIOs; one for chip select, the other for data ready). The pins which are used, as well as 3V3, GND, and RST, are all marked in the silkscreen for the board.

NOTE: Although 5 V is specified on the silkscreen, this pin is not connected to a 5-V supply when the emulation portion of the LaunchPad is disconnected per the advice of the previous section.

For more details on these connections, consult the schematics for TIDM-HARTTRANSMITTER.

4.2.1 Connecting Your Own RTD Sensor

For quick prototyping and testing the system as a whole, a resistor of known value can be utilized as a "2-wire RTD probe" and connected as described in Figure 33. To connect your own RTD sensor probe, utilize J2, J3, and J4 (highlighted in Figure 34) as specified per the instruction given in Figure 33.

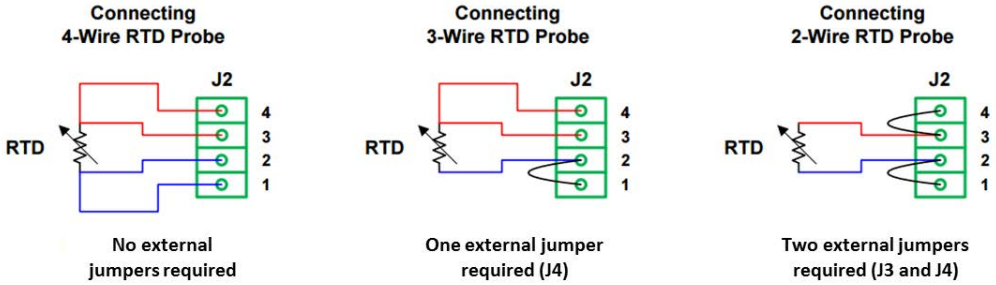


Figure 33. Connecting External 2-, 3-, and 4-wire RTD Sensor Probes

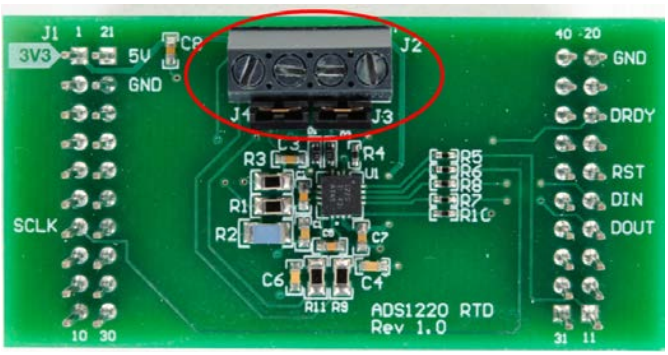


Figure 34. ADS1220 RTD BoosterPack Configurable Jumpers

4.3 DAC161S997 + HART Communication BoosterPack Hardware Overview

The DAC161S997 + HART Communication BoosterPack (DAC + HART BP) is in charge of both the analog and digital communications with respect to the current loop and the HART FSK.

The DAC161S997 aboard the DAC+HART BP shares the SPI bus with the ADS1220 from the ADS1220 RTD BoosterPack. In addition to these three pins, the DAC161S997 also requires three GPIOs for chip select, DAC_ERRLVL, and nDAC_ERR (for more details on the functionalities of these pins, consult the User's Guide for the DAC161S997).

In addition to connecting and configuring the DAC161S997, the DAC+HART BP controls the modulation and demodulation of the HART FSK physical layer. To achieve this, the PWM_OUT pin is brought out and may be measured with an oscilloscope if desired. Additionally, the main HART FSK output waveform (before being coupled into the DAC161S997) may be measured with an oscilloscope at the junction of C13 and R18 if desired. The location of these are both noted in Figure 35.

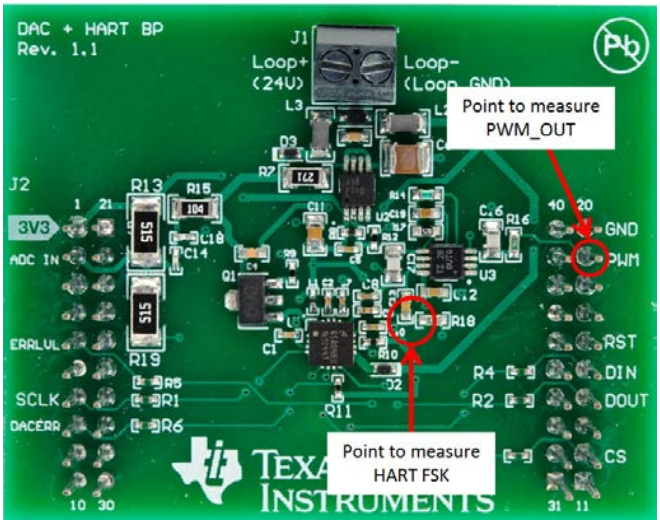


Figure 35. Measurement Points on DAC + HART BP

4.4 Connecting to a HART Master Device

For the purposes of this document, the connection procedures described in this section will align with how to connect to the Moore Industries *HIM Smart HART Loop Interface and Monitor*, Moore Industries (HIM). This HART Master device provides 24-V DC power to a HART Slave, and also allows the option for and external power source for the slave device. As the device in this design is a 2-wire loop powered device, the configuration for being powered by the HIM device will be described.

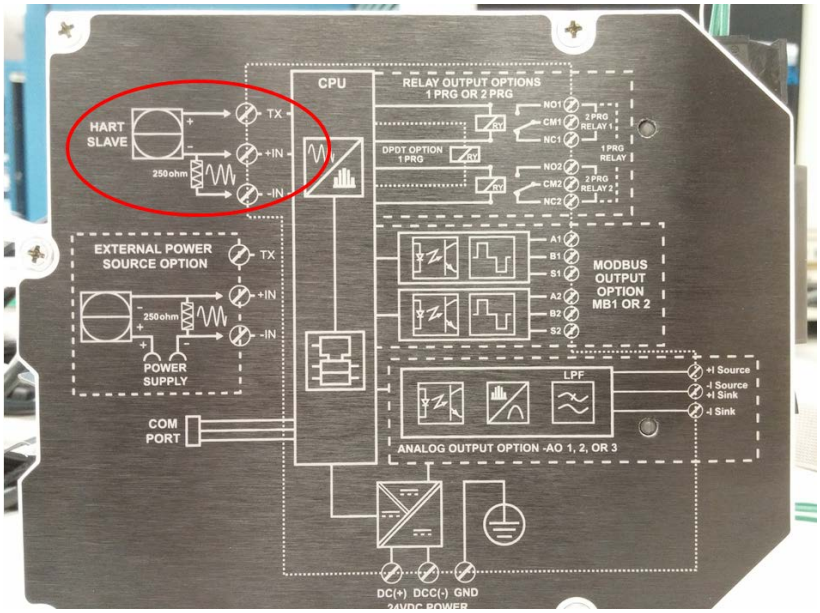


Figure 36. Moore Industries HIM Connections Inscription

According to the inscriptions on the side of the device, which are shown in Figure 36, a 250-Ω resistor is required from the Loop- connection of the DAC + HART BP to the –IN input. The Loop- connection is then also connected to the +IN input without a load resistor. Finally, the Loop+ connection of the DAC+HART BP is connected to the TX input of the HIM. From here, DC power is applied to the device (again per Figure 36). Once the DC power (ideally 24 V) has been applied to the Moore Industries HIM device, it will start up, provide power to the HART Slave device (if one is connected) and begin to query/communicate with the HART slave device. Connections to other HART master devices may differ, and caution should be shown when connecting this design to a HART master to ensure that all connections are made properly before applying power to the device.

CAUTION

Improper care in making these connections properly may result in damage to the device.

5 Getting Started Firmware

The software packaged with this design is intended to be sufficient for a full demonstration of the capabilities of the solution, but is NOT intended to be implemented in an end equipment system. This demonstration level firmware provides two main layers, the lower level HART SoftModem and Protocol Stack driver layer, and the main application layer. While the driver layer of the software is packaged as a locked binary library, the application layer is open for modification and creation of a full sensor application.

5.1 HART SoftModem and Protocol Stack Driver Layer

These aspects of the firmware are delivered as binary libraries to protect the intellectual property of the third party software vendor. To obtain more information on this software, please refer *HART SoftModem and Protocol Stack* (Smart Embedded Systems).

5.2 Application Layer

The application layer software is based off of the same firmware found packaged with TI designs which share the same analog path as *Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter* (TIDU385). As such, the software code is designed to implement a temperature transmitter application highlighting ADS1220 receiving data from an RTD temperature detector and the DAC161S997 outputting this on a 4- to 20-mA current loop, all while maintaining HART FSK communications.

The basic flow of the created application layer is depicted in Figure 37.

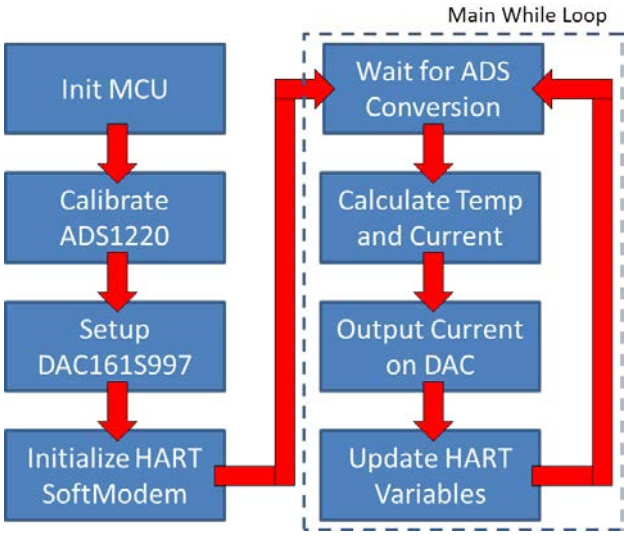


Figure 37. Main Application Layer Flow Chart

Table 4 describes the files that are included in the software package and describes their functionality to the overall demo application.

Table 4. Demo Software File Descriptions

FILE NAME	DESCRIPTION
ads1220.c	Contains all function calls to control and communicate with ADS1220
ads1220.h	Header file for ads1220.c
hart-extvars.h	Contains all HART variables' prototypes
main.c	Main application file
RTD_math.c	Contains all functions for calculating RTD resistance and interpolating to find the corresponding temperature value
RTD_math.h	Header file for RTD_math.c
temp-trans.h	Contains macro definitions for specific port pins
ti-dac161.c	Contains all function calls to control and communicate with DAC161S997
ti-dac161.h	Header file for ti-dac161.c
hartmodem-5969pcm.lib	Library file for HART SoftModem
HARTStack.lib	Library file for HART Protocol Stack

6 Test Setup

The test setup displayed in Figure 38 is the one set up for testing the HART FSK Physical Layer and HART communications in general. The entire contents of this test setup, and the components not pictured in Figure 38 are listed in Table 5. A detailed diagram for setting up the transmitter for testing is shown in Figure 39.

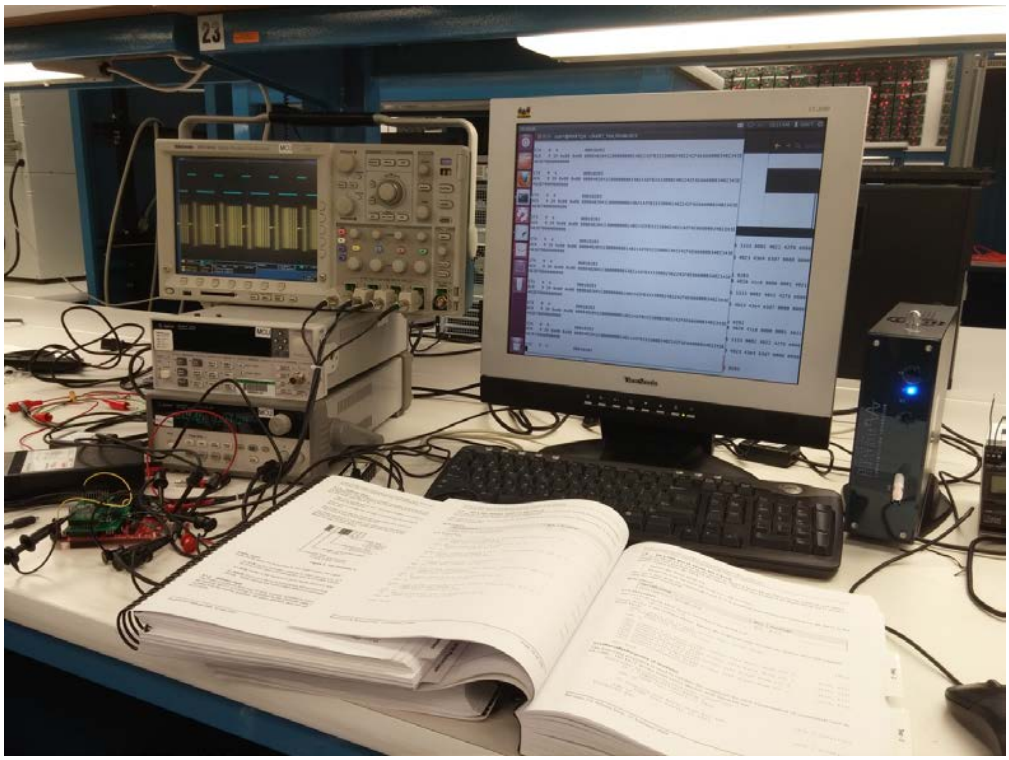


Figure 38. HART FSK Physical Layer Test Setup

Table 5. Complete Test Setup Contents

EQUIPMENT	USAGE
HART Test System (HCF_KIT-192)	Host for multiple HART master modems; run routines to test HART FSK Physical, Data Link, and Application Layers
HART FSK Physical Layer Test Kit (HCF_KIT-116)	RS-232 to HART modem with tunable amplification; interface for HART FSK Physical, Data Link, and Application Layers
ProComSol HM-RS232-ISO	RS-232 to HART modem; interface for HART FSK Physical, Data Link, and Application Layers
Tektronix DPO 4034 Oscilloscope	HART FSK Physical Layer screenshots, debugging Data Link and Application Layers
Agilent E3640A DC Power Supply	Providing +20V DC power to system for current loop operations
HART Digital Filter (HCF_TOOL-31)	Analog filter with passband for HART digital communications only
HART Analog Filter (HCF_TOOL-32)	Analog filter with passband for HART analog communications only
Bipolar Power Supply	Provides DC power and interface for signal generator in parallel for device impedance and noise immunity testing
Signal Generator	Used to generate tones to assess device impedance and noise immunity

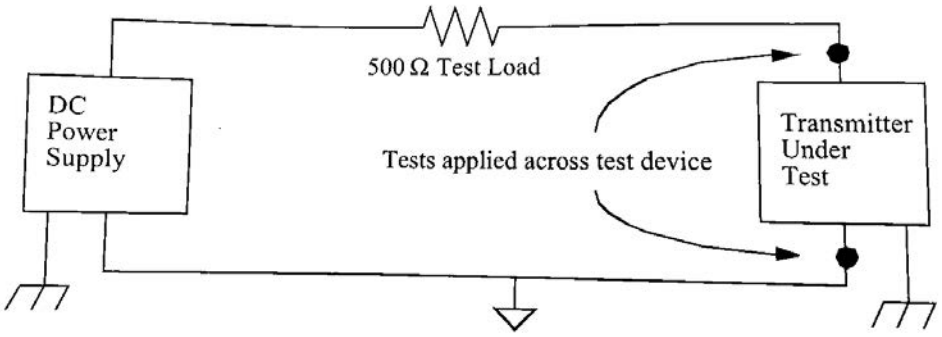


Figure 39. 2-Wire Transmitter Connection for HART FSK Testing

As can be seen in Figure 39, to connect the design board to the HART Test System (HCF_KIT-192), a DC Power Supply and 500Ω Test Load are required. Also required for FSK HART testing is either the HART FSK Physical Layer Test Kit (HCF_KIT-116) or a similar RS-232 to HART modem (see ProComSol HM-RS232-ISO). This test setup is used for all HART Data Link Layer and Application Layer testing. Some HART FSK Physical Layer testing is done in this configuration, but many subtle variations of this test setup are utilized for the different Physical Layer tests. These variations will be noted in the proceeding sections.

7 Test Data

The test results for this design are two fold; testing done for the ADC and DAC accuracy for the analog signal loop and testing done on the digital HART FSK Physical Layer. Each of these are pivotal to the overall performance of the system as a whole.

NOTE: All test data for the digital HART FSK Physical Layer is immediately taken from FieldComm HART pre-certification equipment and test procedures.

7.1 Analog Signal Loop Test Results

For details on testing the analog signal loop of this design, please refer to the documentation for previous designs that utilize the same analog signal chain: *Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter* (TIDU385).

7.2 Digital HART FSK Physical Layer Test Results

According to the *FSK Physical Layer Test Specification HCF_TEST-2* (HART Communication Foundation), a HART transmitter as described by this design should:

- Draw DC current from the loop
- Be DC isolated from ground
- Vary amount of current drawn as a means of analog signaling

Included on top of these requirements, a HART certified transmitter device must meet specifications set out in nine separate tests. The following subsections will display test results from select HART FSK Physical Layer tests and discuss how they satisfy specifications.

7.2.1 Waveshape

The first and most basic requirement of the HART FSK Physical Layer is the Waveshape of the transmitter output. There are three parameters measured for compliance of the transmitted HART waveform for a transmitter device:

1. Signal Amplitude – amplitude must be within 400 mV to 600 mV with a 500-Ω test load
2. Signal Waveshape – characteristics of the waveshape of the transmitted signal must align with ideally sinusoidal characteristics
3. Transmit Frequency – modulation frequencies must be within 1% tolerance of ideal value

The wave shape is assessed for both tones that must be generated by a HART product, 1200 Hz and 2200 Hz.

7.2.1.1 1200-Hz Tone Results

Figure 40 shows the 1200-Hz Waveshape as captured on the oscilloscope. As can be seen from this screenshot, the peak-to-peak voltage of the wave is within the 400–600-mVpp window as specified by the *FSK Physical Layer Test Specification HCF_TEST-2* (HART Communication Foundation). Also of note is that the half-wave period is also within the 396–438-µs window.

Figure 40. 1200Hz FSK Waveshape—Single Wave

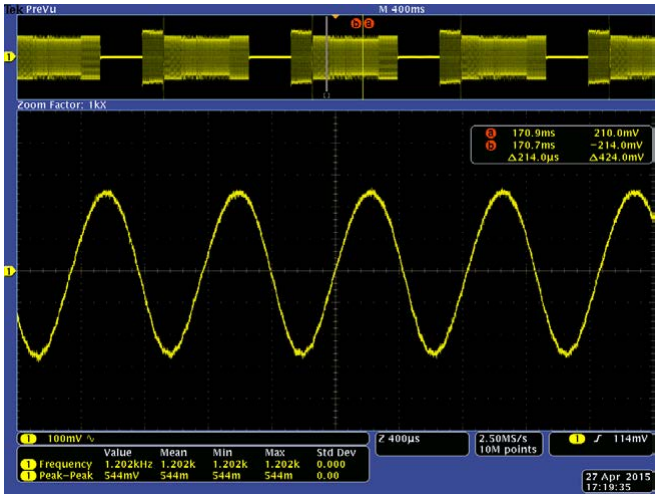


Figure 41. 1200Hz FSK Waveshape—Multiple Waves

7.2.1.2 2200-Hz Tone Results

Figure 42 displays the 2200-Hz Waveshape as captured on the oscilloscope. As can be seen from this screenshot, the peak-to-peak voltage of the wave is within the 400–600-mVpp window as specified by the *FSK Physical Layer Test Specification HCF_TEST-2* (HART Communication Foundation) Also of note is that the half-wave period is also within the 216–238-µs window.

Figure 42. 2200Hz FSK Waveshape—Single Wave

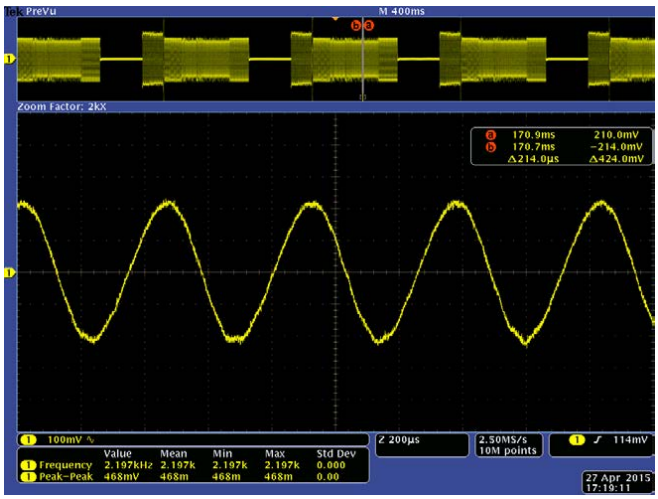


Figure 43. 2200Hz FSK Waveshape—Multiple Waves

7.2.2 Carrier Start / Stop / Decay

Another very important test for the HART FSK Physical Layer is the Carrier Start/Stop/Decay time. This timing is tested to ensure that the transmitted signal level has an appropriate rise or fall time at the start and finish of each transmission. This testing requires three paramters to be measured:

1. Carrier start time: time from the assertion of RTS until the carrier reaches a threshold of >120-mVpp amplitude – must be <4.2 ms
2. Carrier stop time: time from the disassertion of RTS until the carrier drops below the minimum receive threshold of 80mV – must be <2.5 ms
3. Carrier decay time: time from the disassertion of RTS until the carrier drops to an amplitude within the range of allowable noise (<6.16 mVpp) – must be <5 ms

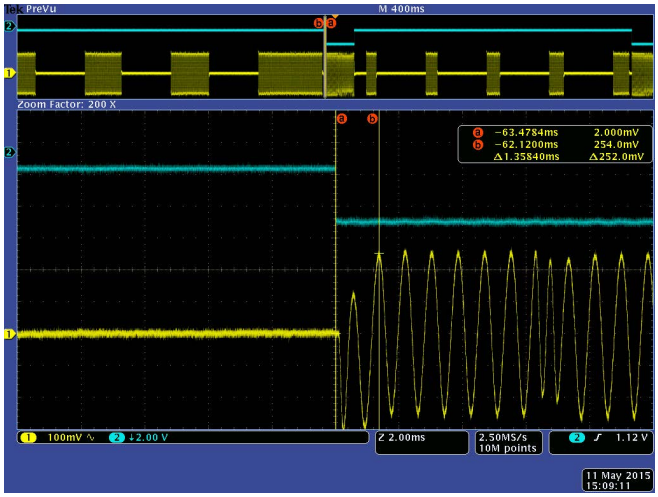


Figure 44. Carrier Start Timing

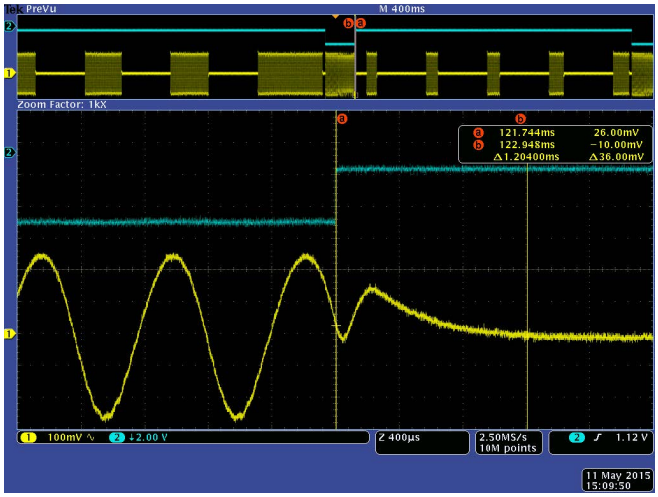


Figure 45. Carrier Stop / Decay Timing

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDM-HRTTRANSMITTER.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-HRTTRANSMITTER.

8.3 Layer Plots

To download the layer plots, see the design files at TIDM-HRTTRANSMITTER.

8.4 Altium Project

To download the Altium project files, see the design files at TIDM-HRTTRANSMITTER.

8.5 Layout Guidelines

To download the layout guidelines, see the design files at TIDM-HRTTRANSMITTER.

8.6 Gerber Files

To download the Gerber files, see the design files at TIDM-HRTTRANSMITTER.

8.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-HRTTRANSMITTER.

8.8 Software Files

To download the software files, see the design files at TIDM-HRTTRANSMITTER.

9 References

1. *Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter* (TIDU385)
2. *How HART Works* (HART Communication Foundation)
3. *HART SoftModem and Protocol Stack* (Smart Embedded Systems)
4. *Namur NE43* (Namur NE43)
5. *MSP-EXP430FR5969 LaunchPad Development Kit User's Guide* (SLAU535a)
6. *Moore Industries HIM Smart HART Loop Interface and Monitor*, Moore Industries (HIM)
7. *FSK Physical Layer Test Specification HCF_TEST-2* (HART Communication Foundation)

10 About the Author

TYLER WITT is a Systems Applications Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment, and supporting customers in the industrial segment. Tyler brings to this role his experience with MSP430™ microcontrollers and interfacing with high-precision data converters.

Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed device name from TIDM-HARTTRANSMITTER to TIDM-HRTTRANSMITTER throughout design guide.....	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265