

RHK3845MKDICE

Radiation Hardened High Voltage Synchronous Step-Down Regulator Kit with Power NMOS FETs

DESCRIPTION

The RHK3845MKDICE is a radiation hardened dice kit that includes one RH3845MK high voltage synchronous step-down controller and two RH411MK power NMOS FETs. In its final hybrid configuration, the RHK3845MK is a wide input voltage range, step-down, synchronous switching regulator. Input voltage range is 7.5V to 60V. With an external V_{CC} supply, minimum input can be reduced to 4.0V. The final hybrid supports output voltages up to 36V, and a switching frequency range of 100kHz to 500kHz. The bulk input and output capacitors, inductor, diodes and other passive elements are needed to finish the design. Note that Burst Mode[®] operation which is available in the LT3845 is not available in the RH3845 version.

DIE CROSS REFERENCE

LTC® Finished Part Number	Order Part Number
RHK3845MK RHK3845MK	RHK3845MK DICE RHK3845MK DWF*

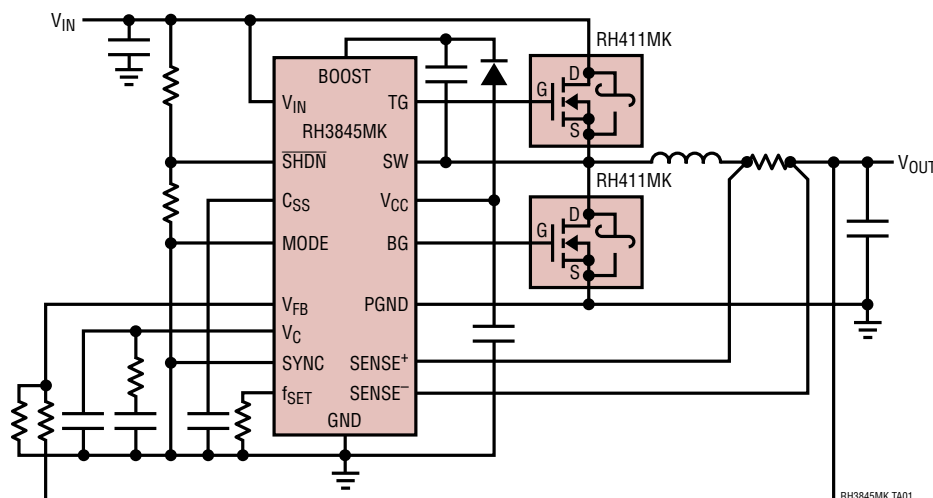
Please refer to LTC standard product data sheet for other applicable product information.

Each kit contains one RH3845MK die and two RH411MK dice.

*DWF = DICE in wafer form.

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TYPICAL APPLICATION



DICE/DWF SPECIFICATION

RH3845MKDICE High Voltage Synchronous Step-Down Controller

DESCRIPTION

The RH3845MK is a high voltage, synchronous, current mode controller for medium to high power, high efficiency supplies. It offers a wide 7.5V to 60V input range. With an external V_{CC} supply, minimum input is 4V. An onboard regulator simplifies the biasing requirements by providing IC power directly from V_{IN} .

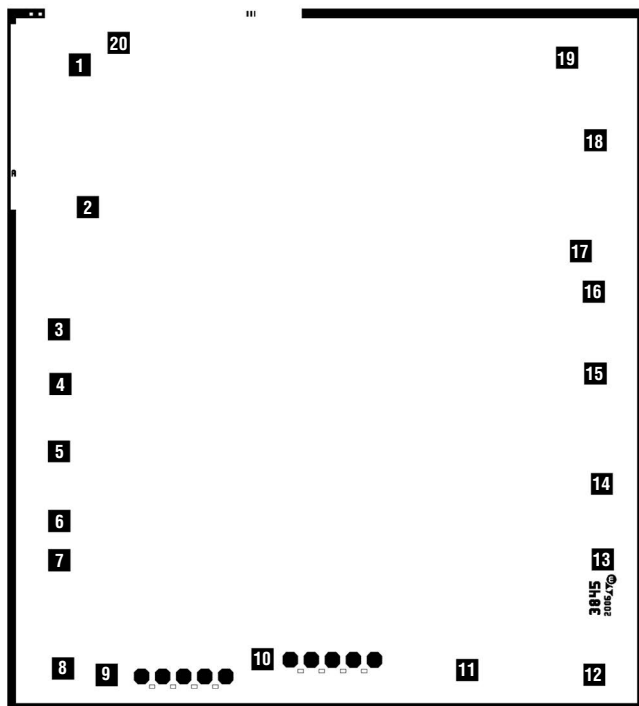
Additional features include an adjustable fixed operating frequency synchronizable to an external clock for noise sensitive applications, gate drivers capable of driving large N-channel MOSFETs, a precision undervoltage lockout, low shutdown current, short-circuit protection, and a programmable soft-start. Note that Burst Mode operation which is available in the LT3845 is not available in the RH3845 version.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}	65V
BOOST	80V
BOOST to SW	24V
V_{CC} , MODE	24V
SENSE ⁺ , SENSE ⁻	40V
SENSE ⁺ TO SENSE ⁻	±1V
SYNC, V_{FB} , AND C_{SS}	5V
$\overline{SHDN}$ Pin Current	1mA
Operating Junction Temperature Range ...	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C

DICE PINOUT



113mils × 124mils,
Backside metal: Alloyed Gold Layer
Backside potential: GND

See page 1 for ordering information

PAD FUNCTION

1. V_{IN}	11. GND
2. $\overline{SHDN}$	12. SENSEN
3. C_{SS}	13. SENSEP
4. MODE	14. PGND
5. V_{FB}	15. BG
6. VC	16. V_{CC}
7. SYNC	17. SW
8. FSET	18. TG
9. GND	19. BOOST
10. GND	20. GND

RH3845MKDICE

TABLE 1: DICE/DWF ELECTRICAL TEST LIMITS Specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 20\text{V}$, $V_{CC} = \text{BOOST} = 10\text{V}$, $\text{SHDN} = 2\text{V}$, $R_{SET} = 49.9\text{k}$, $\text{SENSE}^- = \text{SENSE}^+ = 10\text{V}$, $\text{SGND} = \text{PGND} = \text{SW} = 0\text{V}$.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IN} Minimum Start Voltage (Note 2)			7.5	V
V_{IN} UVLO Threshold (Falling)		3.6	4.0	V
V_{IN} Supply Current	$V_{CC} > 9\text{V}$		200	μA
V_{IN} Shutdown Current	$V_{\text{SHDN}} = 0.3\text{V}$		100	μA
BOOST Supply Current (Note 3)			2	mA
V_{CC} Supply Current			4.5	mA
SHDN Enable Threshold (Rising)		1.30	1.40	V
Reference Voltage		1.214	1.250	V
V_{FB} Input Bias Current			50	nA
V_{FB} Error Amp Transconductance		350		μS
Error Amp Sink/Source Current		35		μA
MODE Pin Current (Note 4)			2	μA
Peak Current Limit Sense Voltage		90	120	mV
Soft-Start Charge Current		8	14	μA
Sense Pins Common-Mode Range		0	36	V
Sense Pins Input Current	$V_{\text{SENSE(CM)}} > 4\text{V}$		400	μA
Reverse Protect Sense Voltage	$V_{\text{MODE}} = 7.5\text{V}$		120	mV
Reverse Current Sense Voltage Offset	$V_{\text{MODE}} = V_{FB}$		20	mV
Switching Frequency	$R_T = 49.9\text{k}$	270	360	kHz
Programmable Frequency Range		100	500	kHz

DICE/DWF SPECIFICATION

RH3845MKDICE

TABLE 2: ELECTRICAL CHARACTERISTICS Specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 20\text{V}$, $V_{CC} = \text{BOOST} = 10\text{V}$, $\text{SHDN} = 2\text{V}$, $R_{SET} = 49.9\text{k}$, $\text{SENSE}^- = \text{SENSE}^+ = 10\text{V}$, $\text{SGND} = \text{PGND} = \text{SW} = 0\text{V}$. (Pre-Irradiation)

PARAMETER	CONDITIONS	SUB-GROUP	$T_A = 25^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			UNITS
			MIN	TYP	MAX		MIN	TYP	MAX	
V_{IN} Minimum Start Voltage (Note 2)		1			7.5	2, 3			7.5	V
V_{IN} UVLO Threshold (Falling)		1	3.6	3.8	4.0	2, 3	3.6	3.8	4.0	V
V_{IN} Supply Current	$V_{CC} > 9\text{V}$	1		130	200	2, 3			800	μA
V_{IN} Shutdown Current	$V_{\text{SHDN}} = 0.3\text{V}$	1		65	100	2, 3			200	μA
BOOST Supply Current (Note 3)		1		1.4	2	2, 3			3.5	mA
V_{CC} Supply Current		1		3.8	4.5	2, 3			5.5	mA
V_{CC} Current Limit		1	-40	-150		2, 3	-40			mA
SHDN Enable Threshold (Rising)		1	1.30	1.35	1.4	2, 3	1.30		1.5	V
SHDN Hysteresis		1		140		2, 3	100		200	mV
Reference Voltage		1	1.214	1.232	1.250	2, 3	1.214		1.250	V
V_{FB} Input Bias Current		1		20	50	2, 3		20		nA
V_{FB} Error Amp Transconductance		1	350	450		2, 3	340		540	μS
Error Amp Sink/Source Current		1	35	50		2, 3	20			μA
Peak Current Limit Sense Voltage		1	90	105	120	2, 3	85		125	mV
Soft-Start Charge Current		1	8	12	14	2, 3	8		16	μA
Sense Pins Common-Mode Range		1	0		36	2, 3	0		36	V
Sense Pins Input Current	$V_{\text{SENSE(CM)}} > 4\text{V}$	1		320	400	2, 3			500	μA
Reverse Protect Sense Voltage	$V_{\text{MODE}} = 7.5\text{V}$	1		108	120	2, 3			140	mV
Reverse Current Sense Voltage Offset	$V_{\text{MODE}} = V_{FB}$	1		15	20	2, 3			25	mV
Switching Frequency	$R_T = 49.9\text{k}$	1	270	300	360	2, 3	240		390	kHz
Programmable Frequency Range		1	100		500	2, 3	100		500	kHz
External Sync Frequency Range		1	100		600	2, 3	100		600	kHz
Non-Overlap Time TG to BG		1		250		2, 3				ns
Non-Overlap Time BG to TG		1		250		2, 3				ns
TG Minimum On-Time		1		400		2, 3				ns
TG Minimum Off-Time		1		300		2, 3				ns
TG, BG Drive On Voltage	$V_{CC} = 10\text{V}$	1	8	8.75		2, 3	8			V
TG, BG Drive Off Voltage		1			0.1	2, 3			0.1	V
TG, BG Drive Rise Time	$C_{TG} = C_{BG} = 3300\text{pF}$	1		45		2, 3				ns
TG, BG Drive Fall Time	$C_{TG} = C_{BG} = 3300\text{pF}$	1		45		2, 3				ns

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TABLE 3: ELECTRICAL CHARACTERISTICS Specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 20\text{V}$, $V_{CC} = \text{BOOST} = 10\text{V}$, $\text{SHDN} = 2\text{V}$, $R_{SET} = 49.9\text{k}$, $\text{SENSE}^- = \text{SENSE}^+ = 10\text{V}$, $\text{SGND} = \text{PGND} = \text{SW} = 0\text{V}$. (Post-Irradiation)

PARAMETER	CONDITIONS	10KRADS (Si) MIN MAX	20KRADS (Si) MIN MAX	50KRADS (Si) MIN MAX	100KRADS (Si) MIN MAX	200KRADS (Si) MIN MAX	UNITS
V_{IN} Minimum Start Voltage (Note 2)		7.5	7.5	7.5	7.5	7.5	V
V_{IN} UVLO Threshold (Falling)		4	4	4	4	4	V
V_{IN} Supply Current	$V_{CC} > 9\text{V}$	200	200	200	200	200	μA
V_{IN} Shutdown Current	$V_{\text{SHDN}} = 0.3\text{V}$	100	100	100	100	100	μA
BOOST Supply Current (Note 3)		2	2	2	2	2	mA
V_{CC} Supply Current		4.5	4.5	4.5	4.5	4.5	mA
V_{CC} Current Limit		-40	-40	-40	-40	-40	mA
SHDN Enable Threshold (Rising)		1.30 1.5	1.30 1.5	1.30 1.5	1.30 1.5	1.30 1.5	V
SHDN Hysteresis		100 180	100 180	100 180	100 180	80 180	mV
Reference Voltage		1.214 1.250	1.210 1.246	1.208 1.244	1.204 1.240	1.187 1.223	V
V_{FB} Input Bias Current		50	100	120	250	350	nA
V_{FB} Error Amp Transconductance		350	330	300	280	250	μS
Error Amp Sink/Source Current		35	35	35	35	30	μA
Peak Current Limit Sense Voltage		90 120	85 120	85 120	80 120	75 120	mV
Soft-Start Charge Current		8 16	8 16	6 16	5 16	4 16	μA
Sense Pins Common-Mode Range		36	36	36	36	36	V
Sense Pins Input Current	$V_{\text{SENSE(CM)}} > 4\text{V}$	400	400	400	400	400	μA
Reverse Protect Sense Voltage	$V_{\text{MODE}} = 7.5\text{V}$	120	120	120	120	120	mV
Reverse Current Sense Voltage Offset	$V_{\text{MODE}} = V_{FB}$	20	20	20	20	20	mV
Switching Frequency	$R_T = 49.9\text{k}$	270 370	270 370	270 370	270 370	270 370	kHz
Programmable Frequency Range		100 500	100 500	100 500	100 500	100 500	kHz
Non-Overlap Time TG to BG		350	350	350	350	350	ns
Non-Overlap Time BG to TG		350	350	350	350	350	ns
TG Minimum On-Time		500	500	500	500	500	ns
TG Minimum Off-Time		350	350	350	360	360	ns
TG, BG Drive On Voltage	$V_{CC} = 10\text{V}$	8	8	8	8	8	V
TG, BG Drive Off Voltage		0.1	0.1	0.1	0.1	0.1	V
TG, BG Drive Rise Time	$C_{TG} = C_{BG} = 3300\text{pF}$	60	60	60	60	60	ns
TG, BG Drive Fall Time	$C_{TG} = C_{BG} = 3300\text{pF}$	60	60	60	60	60	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability.

Note 2: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 3: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 4: Connect the MODE pin to V_{FB} for pulse-skipping mode or V_{CC} for forced continuous mode. Burst Mode operation is not available in the RH3845 version of this part.

TABLE 4: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*, 2, 3
Group A Test Requirements (Method 5005)	1, 2, 3
Group B and D for Class S, End Point Electrical Parameters (Method 5005)	1, 2, 3

*PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

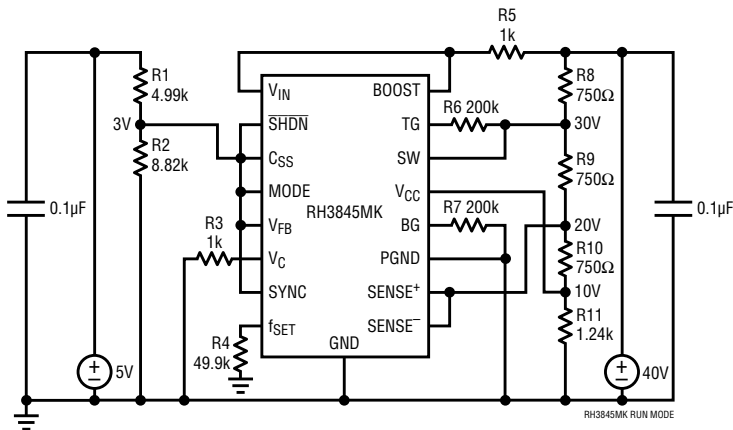
The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

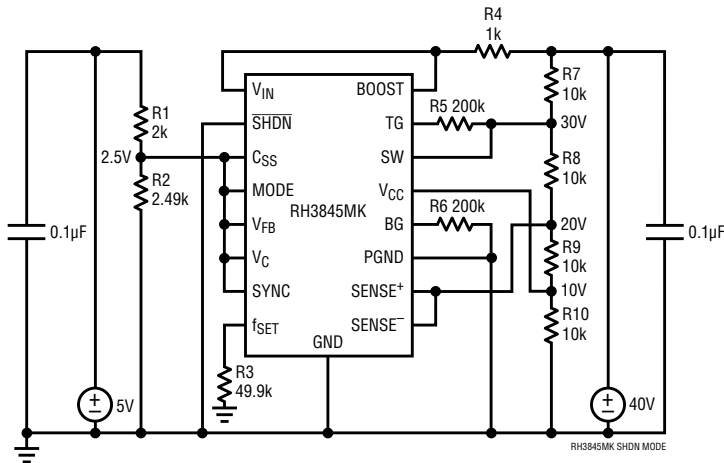
DICE/DWF SPECIFICATION

RH3845MKDICE

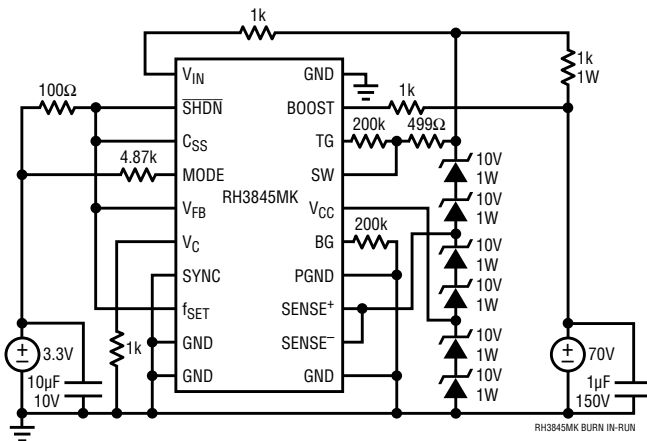
TOTAL DOSE BIAS CIRCUIT — RUN MODE



TOTAL DOSE BIAS CIRCUIT — SHUTDOWN MODE

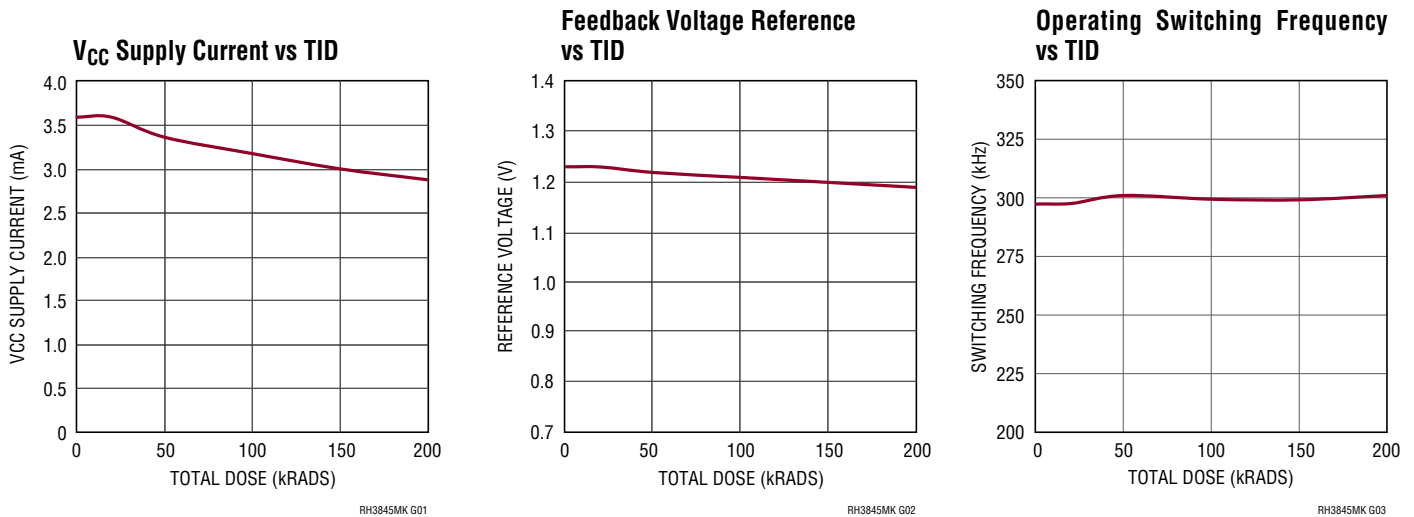


BURN-IN CIRCUIT — RUN MODE



RH3845MKDICE

TYPICAL PERFORMANCE CHARACTERISTICS



Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand.

This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

DESCRIPTION

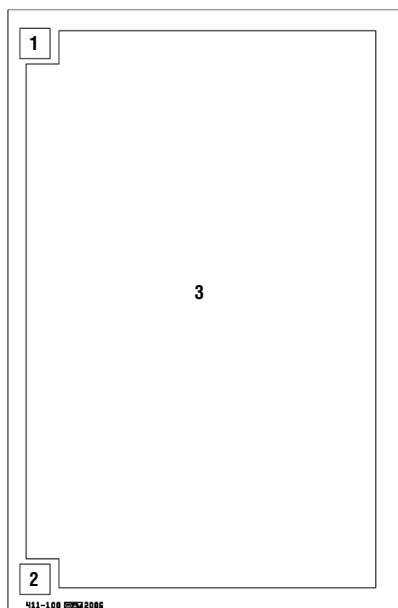
The RH411MK is a high performance power N-MOSFET for use only in combination with an LTC synchronous current mode controller. This device has been characterized for Total Ionizing Dose (TID) up to 200KRad(Si). The low 28mΩ $R_{DS(ON)}$, low 23nC gate charge and 80V FET enhance switching regulator efficiency. The integrated source-drain high current Schottky diode fulfills the need for a “Catch” diode across the bottom switch of a Buck regulator and reduces power dissipation during the regulator switch non-overlap time.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{GS}±15V
 Operating Junction Temperature..... 150°C

The RH411MKDICE are available for ordering only as part of the RHK3845MKDICE (kit) under specific terms and conditions. Contact LTC sales or marketing for additional details.



PAD FUNCTION

- | | |
|------------|--------|
| 1. | Gate |
| 2. | Gate |
| 3. | Source |
| Substrate. | Drain |

157mils × 102mils²,
 Backside metal: Alloyed Gold Layer
 Backside potential: NMOS Drain

RH411MKDICE

TABLE 1 DICE/DWF ELECTRICAL TEST LIMITS $T_A = 25^\circ\text{C}$ (Notes 2, 3, 4)

PARAMETER	TEST CONDITION	MIN	MAX	UNITS
Drain-to-Source Breakdown Voltage	$V_{GS} = 0V$; $I_D = 3mA$	100		V
Static Drain-to-Source On State Resistance	$V_{GS} = 8V$, $I_D = 0.2A$		45	$m\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 9.8mA$	3.95	4.60	V
Zero Gate Voltage Drain Current	$V_{DS} = 60V$, $V_{GS} = 0V$		1	μA
Gate-to-Source Leakage	$V_{GS} = \pm 15V$, $V_{DS} = 0V$	-20	20	nA
Total Gate Charge	$V_{GS} = 8V$, $V_{DS} = 30V$, $I_D = 200mA$		30	nC
Schottky Diode Forward Voltage	$V_{GS} = 0V$, $I_D = -0.18A$		0.6	V

TABLE 2 ELECTRICAL CHARACTERISTICS (Pre-Irradiation) (Notes 2, 4,5)

PARAMETER	TEST CONDITION	$T_A = 25^\circ\text{C}$		SUB-GROUP	$-55^\circ\text{C} < T_A < 150^\circ\text{C}$		SUB-GROUP	UNITS
		MIN	MAX		MIN	MAX		
Drain-to-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 3mA$	100		1	85		2, 3	V
Static Drain-to-Source On State Resistance	$V_{GS} = 8V$, $I_D = 5A$		45	1		95	2, 3	$m\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 9.8mA$	3.95	4.65	1	2.25	5.8	2, 3	V
Zero Gate Voltage Drain Current	$V_{DS} = 60V$, $V_{GS} = 0V$		1	1		200	2, 3	μA
Gate-to-Source Leakage	$V_{GS} = \pm 15V$, $V_{DS} = 0V$	-20	20	1	-1000	1000	2, 3	nA
Total Gate Charge	$V_{GS} = 8V$, $V_{DS} = 30V$, $I_D = 200mA$		30	1		50	2, 3	nC
Schottky Diode Forward Voltage	$V_{GS} = 0V$, $I_D = -0.2A$		0.6	1		0.75	2, 3	V
	$V_{GS} = 0V$, $I_D = -5A$		0.75	1		0.85	2, 3	V

TABLE 3 ELECTRICAL CHARACTERISTICS (Post-Irradiation, $T_A = 25^\circ\text{C}$) (Notes 2, 4,5)

PARAMETER	TEST CONDITION	50KRad(Si)		100KRad(Si)		150KRad(Si)		200KRad(Si)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Drain-to-Source Breakdown Voltage	$V_{GS} = 0V$; $I_D = 3mA$	80		80		80		80		V
Static Drain-to-Source On State Resistance	$V_{GS} = 8V$; $I_D = 5A$		50		50		50		50	$m\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}$; $I_D = 9.8mA$	3.0	4.65	2.25	4.65	1.75	4.65	1.25	4.65	V
Zero Gate Voltage Drain Current	$V_{DS} = 60V$; $V_{GS} = 0V$		10		10		10		10	μA
Gate-to-Source Leakage	$V_{GS} = \pm 15V$; $V_{DS} = 0V$	-100	100	-100	100	-100	100	-100	100	nA
Total Gate Charge	$V_{GS} = 8V$, $V_{DS} = 30V$, $I_D = 200mA$		40		40		40		40	nC
Schottky Diode Forward Voltage	$V_{GS} = 0V$, $I_D = -0.2A$		0.65		0.65		0.65		0.65	V
	$V_{GS} = 0V$, $I_D = -5A$		0.8		0.8		0.8		0.8	V

Note 1: Stress beyond those listed under Absolute Maximum Ratings may cause damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The RH411MK is tested under pulse current conditions such that $T_J \approx T_A$.

Note 3: Dice are probe tested at 25°C to the limits shown in Table 1. Dice are tested under low current conditions which assure full high current specifications when assembled in packaging systems approved by Linear Technology.

Note 4: Dice that are not qualified by Linear Technology with a can sample are guaranteed to meet specifications in Table 1 only. Dice qualified by Linear Technology with a can sample meet specifications in all tables.

Note 5: Can sample are tested in a 4-Lead TO-3 package.

DICE/DWF SPECIFICATION

RH411MKDICE

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Dice data sheet is subject to change. Please consult factory for current revision in production.

This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

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TABLE 5. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
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Group A Test Requirements (Method 5005)	1, 2, 3
Group B and D for Class S, End Point Electrical Parameters (Method 5005)	1, 2, 3

*PDA applies to subgroup 1. See PDA Test Notes.

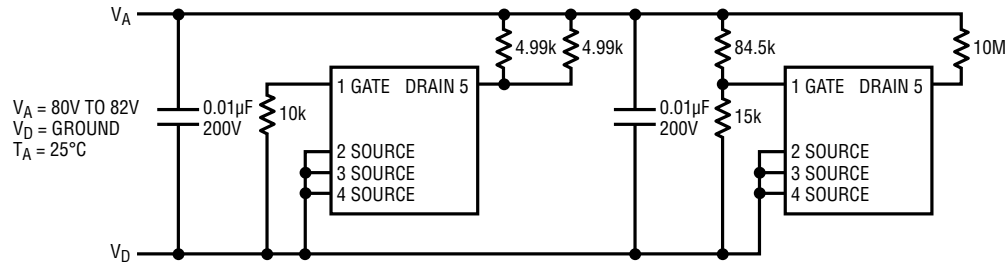
PDA Test Notes

The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

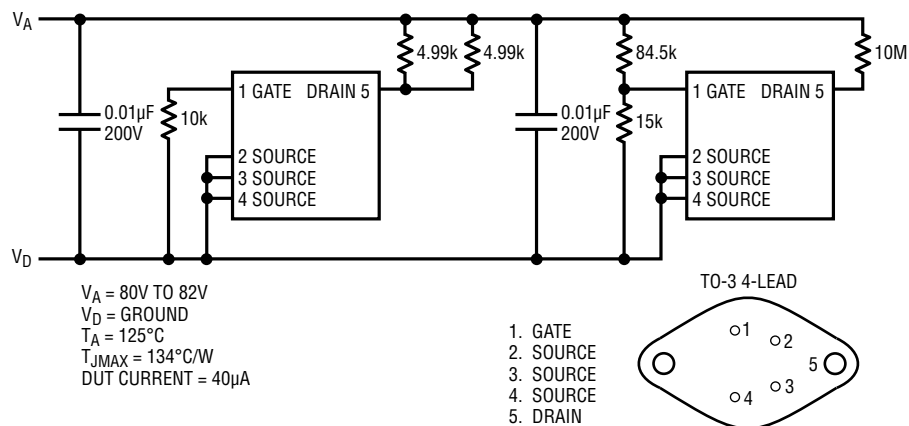
Linear Technology Corporation reserves the right to test to tighter limits than those given.

RH411MKDICE

TOTAL DOSE BIAS CIRCUIT



BURN-IN CIRCUIT

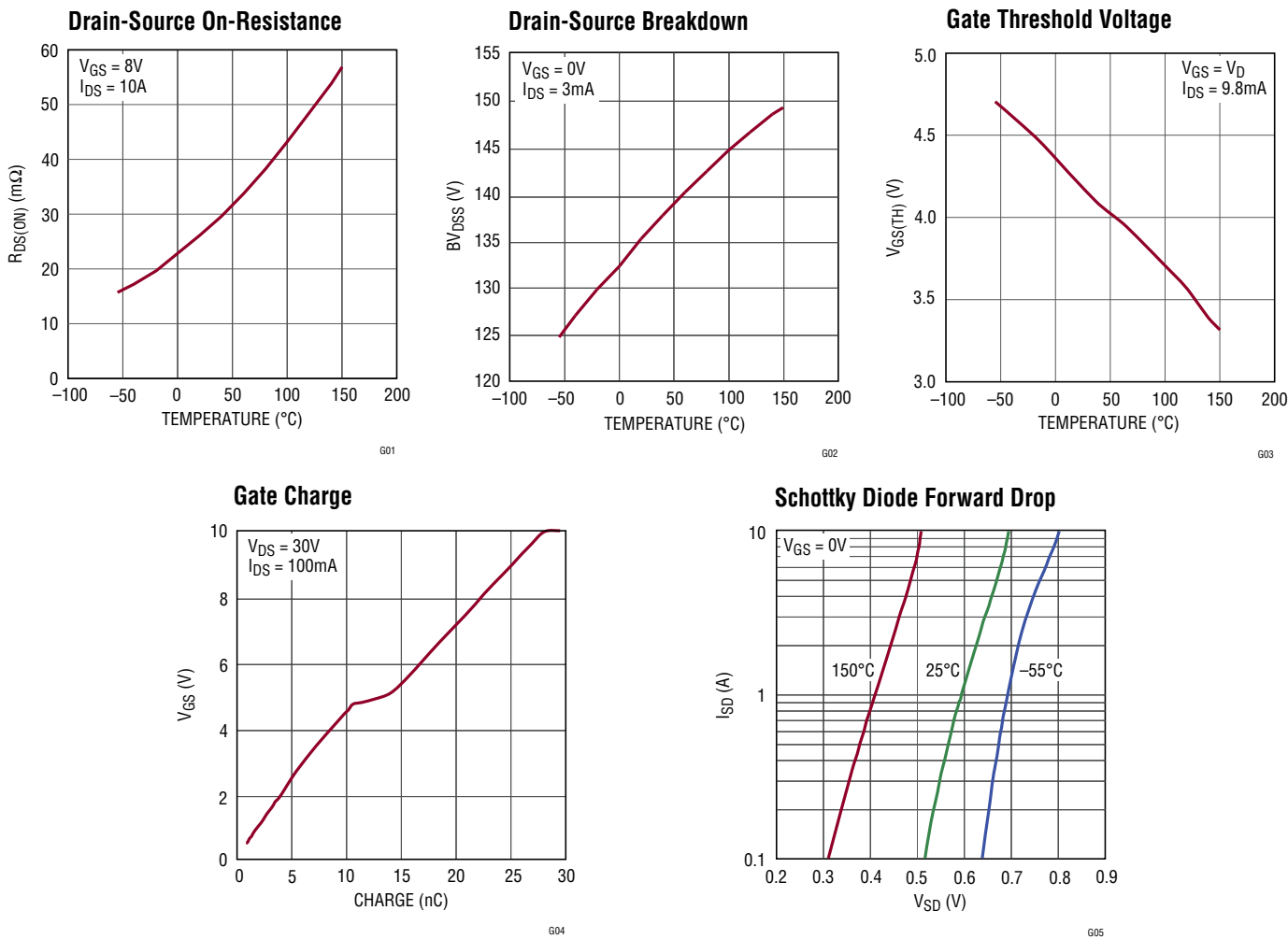


DICE/DWF SPECIFICATION

RH411MKDICE

TYPICAL PERFORMANCE CHARACTERISTICS PREIRRADIATION

(4-Lead TO-3 Package)

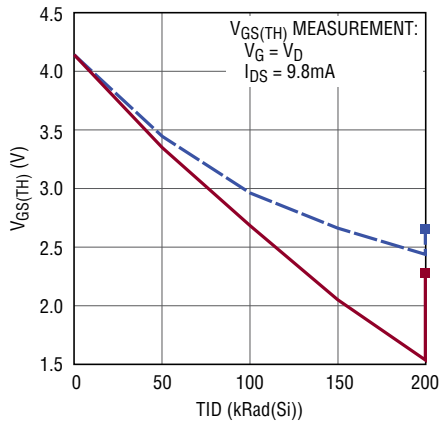


RH411MKDICE

TYPICAL PERFORMANCE CHARACTERISTICS POST-IRRADIATION

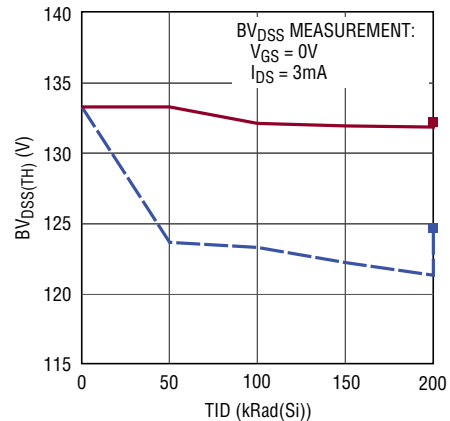
(4-Lead TO-3 Package)

Gate Threshold Voltage vs TID



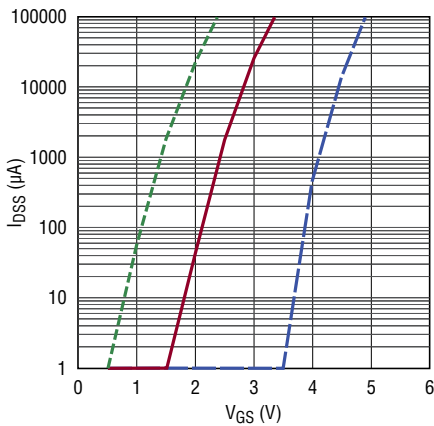
— BIASED $V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
 - - BIASED $V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$
 ■ POST 3 WEEK 25°C BIASED ANNEAL, $V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
 ■ POST 3 WEEK 25°C BIASED ANNEAL, $V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$

Drain-Source Breakdown vs TID



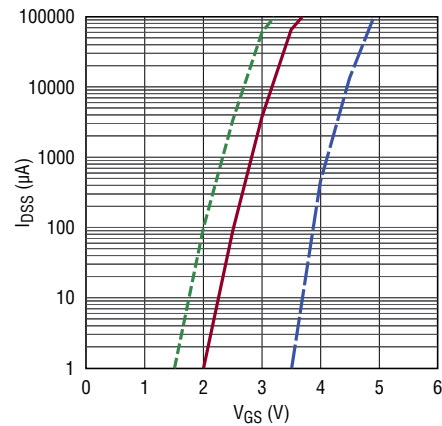
— BIASED $V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
 - - BIASED $V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$
 ■ POST 3 WEEK 25°C BIASED ANNEAL, $V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
 ■ POST 3 WEEK 25°C BIASED ANNEAL, $V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$

I_{DSS} vs TID, Gate Biased



I_{DSS} MEASUREMENT:
 $V_{DS} = 0.1\text{V}$
 — PRE IRRADIATION
 — POST 100 kRad(Si), $V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$
 - - POST 200 kRad(Si), $V_{DS} = 0\text{V}$, $V_{GS} = 12\text{V}$

I_{DSS} vs TID, Drain Biased



I_{DSS} MEASUREMENT:
 $V_{DS} = 0.1\text{V}$
 — PRE IRRADIATION
 — POST 100 kRad(Si), $V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
 - - POST 200 kRad(Si), $V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$

DICE/DWF SPECIFICATION

RH411MKDICE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/15	Removed V_{CC} Current Limit. Corrected Reverse Current Sense Voltage Offset from 10mV to 20mV. Clarified Description text.	3, 5, 8

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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