Reference Design RD-356

1. Fairchild Motion SPM® 7 Series

This reference design supports design of Fairchild's Motion SPM® 7 Series. It should be used in conjunction with each datasheet as well as Fairchild's application notes and technical support team. Please visit Fairchild's website at http://www.fairchildsemi.com.

Application	Device Name	Max. Supply Voltage	Max. Power Rating	Topology
`Home Appliance (Fan Motor)	FSB70625	200 V_{DC}	81 W	3-Phase Inverter
	FSB70325	200 V_{DC}	49 W	
	FSB70550	400 V_{DC}	110W	
	FSB70450	400 V_{DC}	110 W	
	FSB70250	400 V_{DC}	81 W	

1.1. Key Features

- 3-Phase FRFET® Inverter with High-Voltage Integrated Circuit (HVIC)
- Maximum $R_{DS(ON)}$: FSB70625=0.8 Ω, FSB70325=1.4 Ω, FSB70550=1.85 Ω, FSB70450=2.2 Ω, FSB70250=3.4 Ω
- High-Performance PQFN Package
- Open-Source Pins Separate from Low-Side MOSFETs for 3-Phase Current-Sensing
- Active-HIGH Interface Works with 3.3 V / 5 V Logic
- Schmitt-Trigger Input
- Optimized for Low Electromagnetic Interference (EMI)
- HVIC Temperature-Sensing for Temperature Monitoring
- HVIC for Gate Driving with Under-Voltage Protection (UVP)
- Interlock Function
- Isolation Rating: 1500 V_{RMS} / Min.
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

The internal circuit diagram is shown in Figure 1. The V_{TS} pin is from the HVIC and provides the temperature-sensing signal.

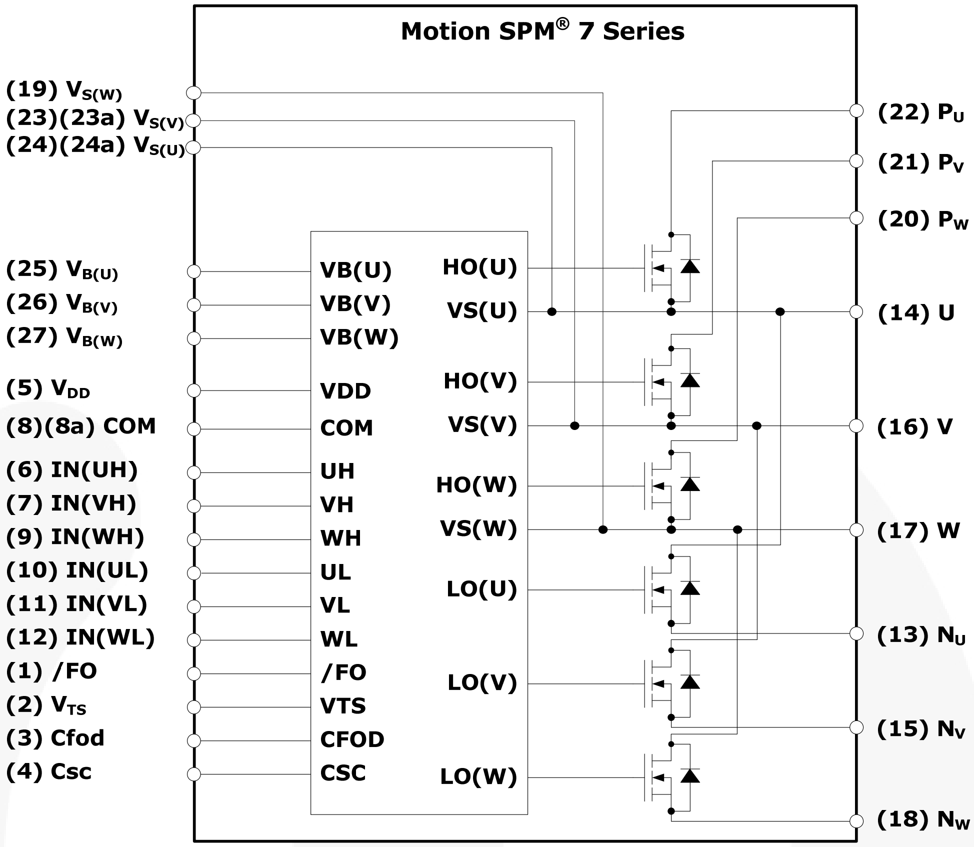

Figure 1. Internal Circuit Diagram

2. Pin Description

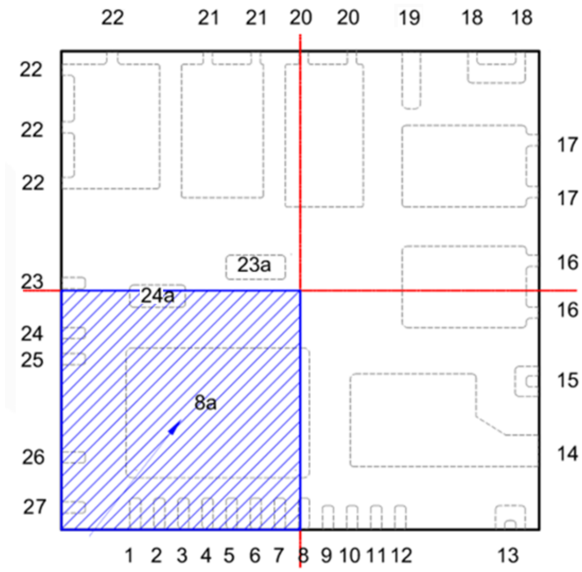

Figure 2. Pin Numbers and Locations in PQFN Package (Top-Through View)

Table 1. Pin Descriptions

Pin #	Name	Pin Description
1	/FO	Fault Output
2	V_{TS}	Voltage Output of HVIC Temperature
3	Cfod	Capacitor for Duration Time of Fault Output
4	Csc	Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input
5	V_{DD}	Supply Bias Voltage for IC and MOSFETs Driving
6	IN_UH	Signal Input for High-Side U Phase
7	IN_VH	Signal Input for High-Side V Phase
8 (8a)	COM	Common Supply Ground
9	IN_WH	Signal Input for High-Side W Phase
10	IN_UL	Signal Input for Low-Side U Phase
11	IN_VL	Signal Input for Low-Side V Phase
12	IN_WL	Signal Input for Low-Side W Phase
13	Nu	Negative DC-Link Input for U Phase
14	U	Output for U Phase
15	N_V	Negative DC-Link Input for V Phase
16	V	Output for V Phase
17	W	Output for W Phase
18	N_W	Negative DC-Link Input for W Phase
19	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase MOSFET Driving
20	P_W	Positive DC-Link Input for W Phase
21	P_V	Positive DC-Link Input for V Phase
22	P_U	Positive DC-Link Input for U Phase

Pin #	Name	Pin Description
23(23a)	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase MOSFET Driving
24(24a)	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase MOSFET Driving
25	$V_{B(U)}$	High-Side Bias Voltage for U phase MOSFET Driving
26	$V_{B(V)}$	High-Side Bias Voltage for V phase MOSFET Driving
27	$V_{B(W)}$	High-Side Bias Voltage for W phase MOSFET Driving

3. Application Block Diagram

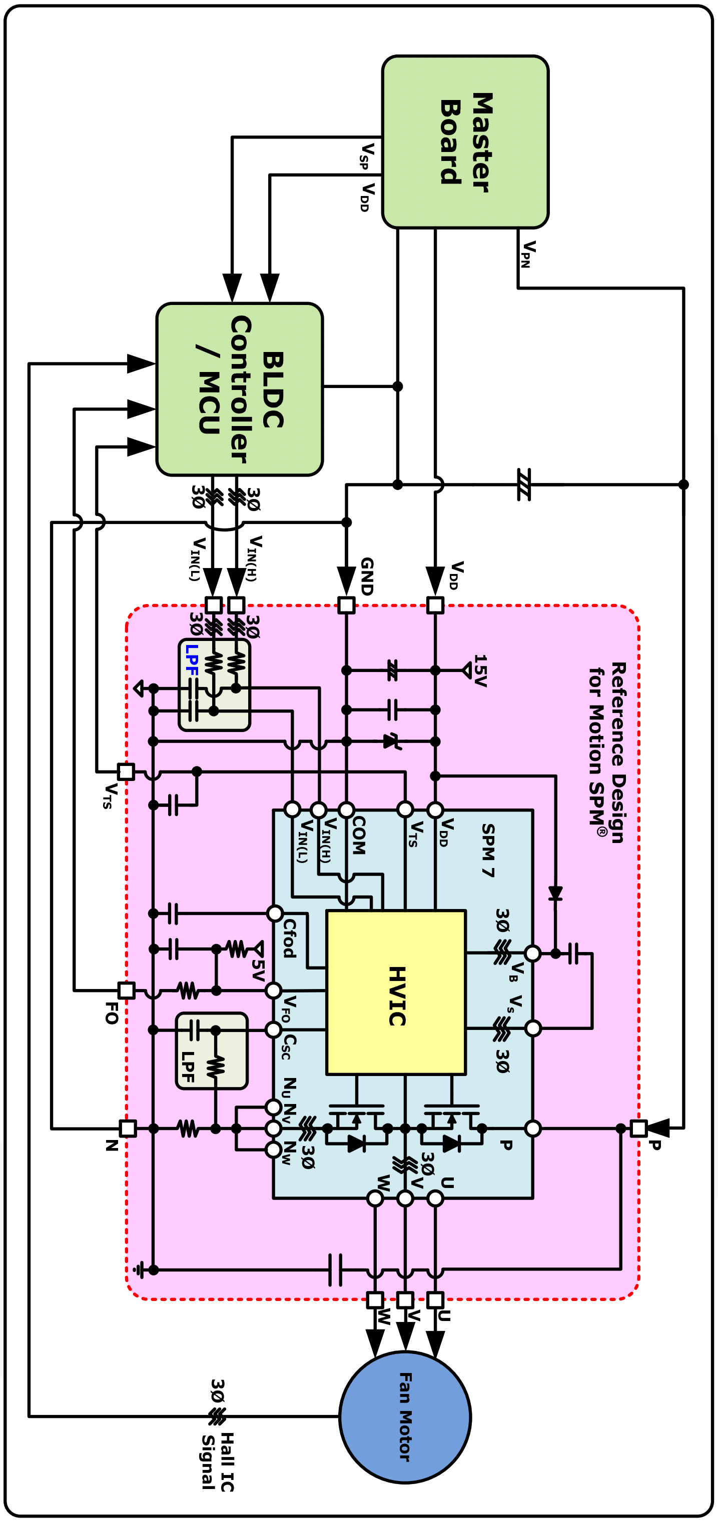

Figure 3. Block Diagram of Outdoor Fan Motor for Air-Conditioner

4. Schematic

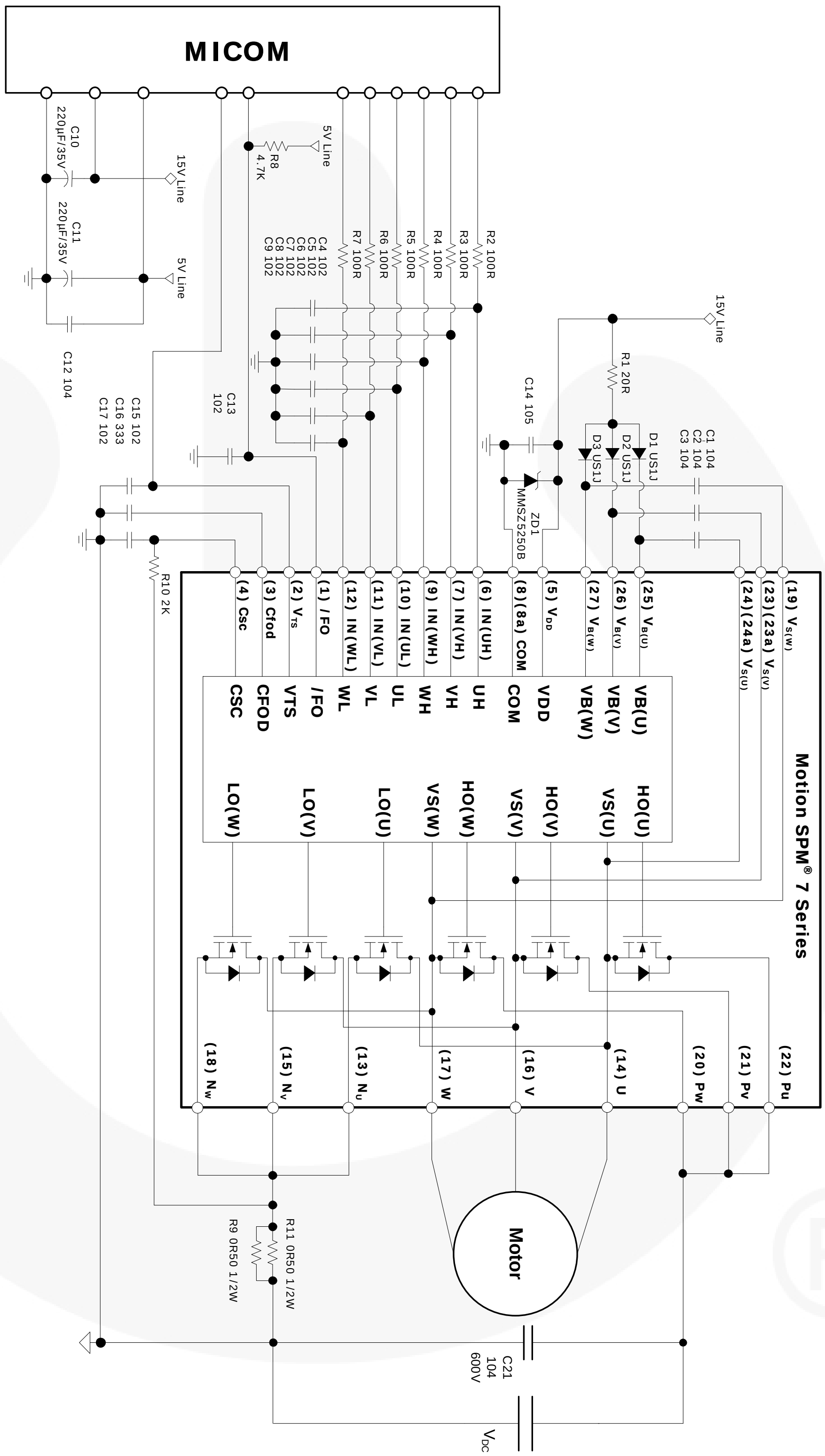

Figure 4. Schematic for 3-Phase Inverter Part (Direct Coupling)

5. Key Parameter Design

5.1. Selection of Bootstrap Capacitance(C_{BS})

The current flow path of the bootstrap circuit is shown in Figure 5. When V_S is pulled down to ground (either through the low-side or the load), bootstrap capacitor C_{BS} is charged through bootstrap diode D_{BS} and resistor R_{BS} from the V_{DD} supply.

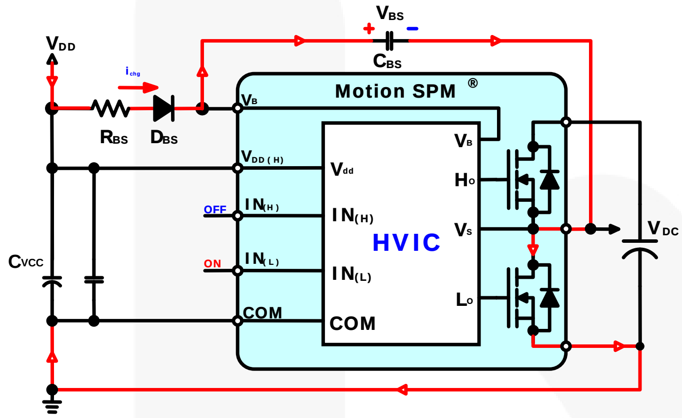

Figure 5. Bootstrap Circuit

The bootstrap capacitor of the Motion SPM® 7 Series can be calculated by:

$$C_{BS} = \frac{Q_{BS}}{\Delta V_{BS}} \tag{1}$$

where:

Q_{BS} = Total gate charge from C_{BS}; and

ΔV_{BS} = Allowable drop voltage of the C_{BS} (voltage ripple).

Total gate charge, Q_{BS}, required by the bootstrap capacitor, can be calculated by:

$$Q_{BS} = Q_g + Q_{LS} + (I_{LK,D} + I_{LK,C} + I_{QBS}) \times t_{ON} \tag{2}$$

where:

Q_g = Gate charge to turn on the high-side MOSFET;

Q_{LS}= Level-shift charge required per cycle;

I_{LK} = Total leakage current;

$I_{LK,D}$ = Bootstrap diode leakage current;

$I_{LK,C}$ = Bootstrap capacitor leakage current, which can be ignored if it is not an electrolytic capacitor;

I_{QBS}= Quiescent current of gate driver IC; and

t_{ON}= Maximum on pulse width of high-side MOSFET.

The total leakage current can be calculated by summing all of the individual components' leakage currents. In case of FSB70325, minimum C_{BS} is calculated as:

$$C_{BS\_min} = \frac{Q_{BS}}{\Delta V_{BS}} = \frac{Q_g + Q_{LS} + (I_{LK,D} + I_{LK,C} + I_{QBS}) \times t_{ON}}{\Delta V_{BS}} \tag{3}$$

$$= \frac{50\,nC + (100\,\mu A + 70\,\mu A) \times 200\,\mu s}{0.1V} = 0.84\,\mu F$$

→ More than two times (2X) → 2.2 µF

where:

V_{DD}=15 V

Bootstrap diode = US1J

$Q_g + Q_{LS}$ = Approximate maximum 50 nC (designed value);

$I_{LK,D}$ = 100 µA (maximum. value from datasheet);

$I_{LK,C}$ = 0 (ceramic capacitor);

I_{QBS}=70 µA (maximum value from datasheet);

t_{ON}= 200 µs (depends on system);

ΔV_{BS} = 0.1 V (depends on system);

Recommended C_{BS} is normally 2~3 times C_{BS_min}.

5.2. Initial Charging Sequence for Bootstrap Capacitor

Adequate on-time duration of the low-side MOSFET to fully charge the bootstrap capacitor is required for initial bootstrap charging. In case of the Motion SPM® 7 Series, the initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} = C_{BS} \times R_{BS} = \frac{1}{\delta} \times In \frac{V_{CC}}{V_{DD} - V_{BS(\min)} - V_F - V_{LS}} \tag{4}$$

where:

V_F = Forward voltage drop across the bootstrap diode;

$V_{BS(min)}$ = Minimum value of the bootstrap capacitor;

V_{LS} = Voltage drop across the low-side IGBT or load; and

δ = Duty ratio of PWM.

To charge three bootstrap capacitors at the same time; theoretically, the maximum initial charging current could exceed OCP level. Therefore, initial charging time for bootstrap capacitors should be separated as shown in Figure 6.

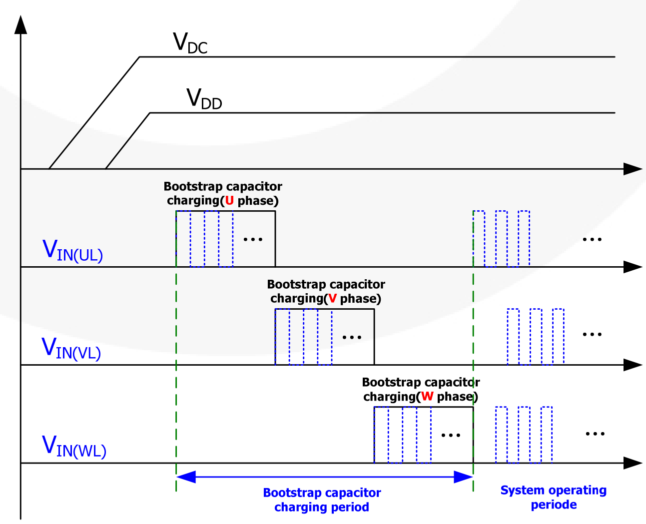

Figure 6. Bootstrap Recommended Initial Bootstrap Capacitors Charging Sequence

5.3. Selection of Shunt Resistor (One Shunt)

The value of shunt resistor is calculated by the following equations.

Maximum short-circuit (SC) current trip level (depends on user selection):

$$I_{SC(max)}=1.5 \times I_{D(max)} \tag{5}$$

SC trip reference voltage (depends on datasheet):

$$V_{SC} = \text{Min.}0.45\text{ V, Typ.}0.5\text{ V, Max.}0.55\text{ V} \tag{6}$$

Shunt resistance:

$$I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)} \tag{7}$$

If the deviation of the shunt resistor is limited below ±5%:

$$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95,\ R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05 \tag{8}$$

Actual SC trip current level becomes:

$$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)},\ I_{SC(min)}= V_{SC(min)} / R_{SHUNT(max)} \tag{9}$$

Inverter output power:

$$P_{OUT} = \sqrt{3} / \sqrt{2} \times MI \times V_{DC\ Link} \times I_{RMS} \times PF \tag{10}$$

where:

MI = modulation index;

V_{DC_Link}= DC link voltage;

I_{RMS} = Maximum load current of inverter; and

PF = power factor;

Average DC current:

$$I_{DC\ AVG}= V_{DC\_Link}/ (P_{out} \times Eff) \tag{11}$$

where:

Eff = inverter efficiency.

The power rating of shunt resistor is calculated by the following equation:

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio \tag{12}$$

where:

R_{SHUNT} = Shunt resistor typical value at T_C=25°C

Derating Ratio = Derating ratio of shunt resistor at T_{SHUNT}=100°C (from datasheet of shunt resistor); and

Margin = Safety margin (determined by customer).

Shunt Resistor Calculation Examples

Calculation Conditions:

- DUT: FSB70450, Tolerance of R_{SHUNT}: ±5%
- SC Trip Reference Voltage:
  - $V_{SC(min)}$=0.45 V, $V_{SC(typ)}$=0.50 V, $V_{SC(max)}$=0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 0.4 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{D(max)}$): 0.6 A
- Modulation Index(MI): 0.9
- V_{DC} Link ($V_{DC\ LINK}$): 300 V
- Power Factor (PF): 0.8
- Inverter Efficiency (Eff): 0.98
- Shunt Resistor Value at T_C=25°C (R_{SHUNT}): 0.25Ω
- Derating Ratio of Shunt Resistor at T_{SHUNT}=100°C: 70%
- Safety Margin: 20%

Calculation Results:

- $I_{SC(max)}$: 1.5 x $I_{D(max)}$ = 1.5 x 0.6 A= 0.9 A
- $R_{SHUNT(min)}$: $V_{SC(max)}$ / $I_{SC(max)}$ = 0.55 V / 0.9 A = 0.61 Ω
- $R_{SHUNT(typ)}$: $R_{SHUNT(min)}$ / 0.95 = 0.61 Ω / 0.95 = 0.64 Ω
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ x 1.05 = 0.64 Ω x 1.05 = 0.67 Ω
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.45 V / 0.67 Ω = 0.67 A
- $I_{SC(typ)}$: $V_{SC(typ)}$ / $R_{SHUNT(typ)}$ = 0.5 V / 0.64 Ω = 0.78 A
- $P_{OUT} = \sqrt{3}/\sqrt{2} \times MI \times V_{DC\ Link} \times I_{RMS} \times PF$ = 105.8 W
- $I_{DC\ AVG}$= (P_{OUT}/Eff) / $V_{DC\ Link}$ = 0.36 A
- $P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times \text{Margin})$ / Derating Ratio = $(0.36^2 \times 0.67 \times 1.2)$ / 0.7=0.15 W (therefore, recommended power rating of shunt resistor is 0.2 W)

5.4. Design of Over-Temperature Protection (OTP) Circuit

The Motion SPM® 7 Series provides sensing output of the temperature for the OTP circuit. The V_{TS} PIN is directly connected to the built-in temperature sensor in HVIC, as shown in the Figure 7.

Note:

1. V_{TS} is only for sensing temperature related to the module and cannot shutdown MOSFETs automatically.

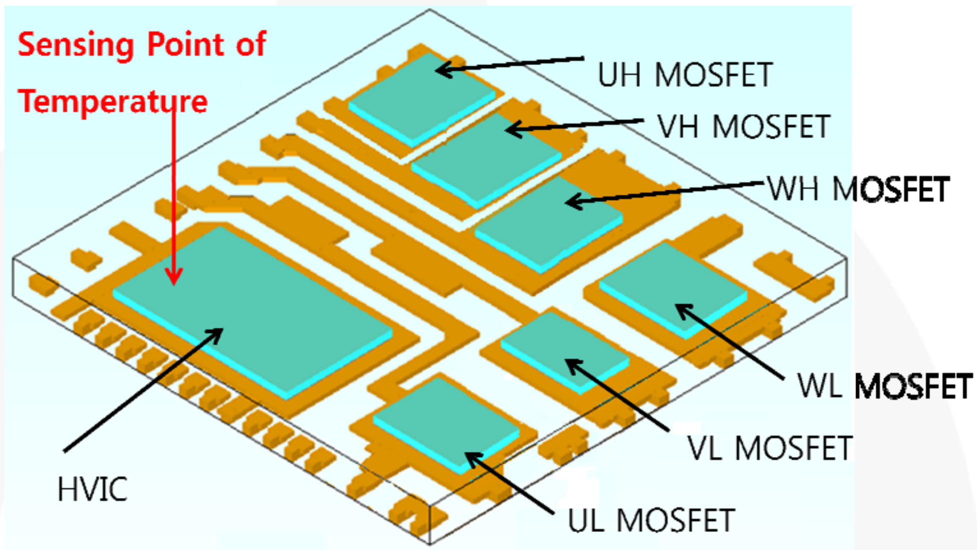

Figure 7. Position of the Built-in Temperature Sensor

Figure 8 is V-T curve of Temperature Sensing (TS) function in Motion SPM® 7 Series.

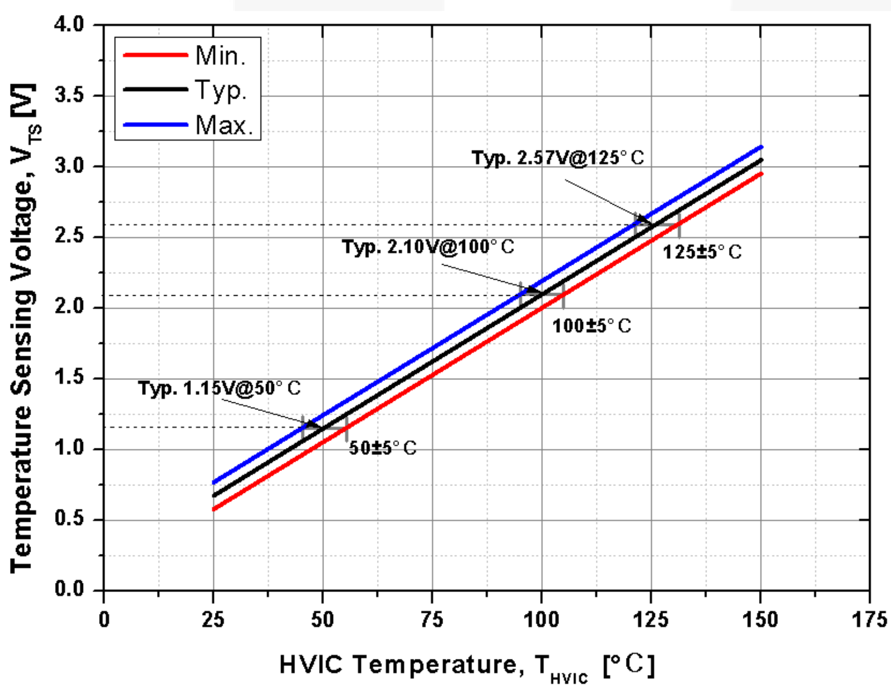

Figure 8. V-T Curve of Temperature Sensing (TS) Function

Figure 9 is a typical application circuit for the TS function. In this reference design, the set level is 100°C (V_{TS}=2.1 V), the reset level is 80°C (V_{TS}=1.72 V), and the hysteresis temperature is 20°C (Figure 10). If using an Analog-to-Digital Converter (ADC) port, a capacitor is needed between the VTS and GND pins (Figure 11).

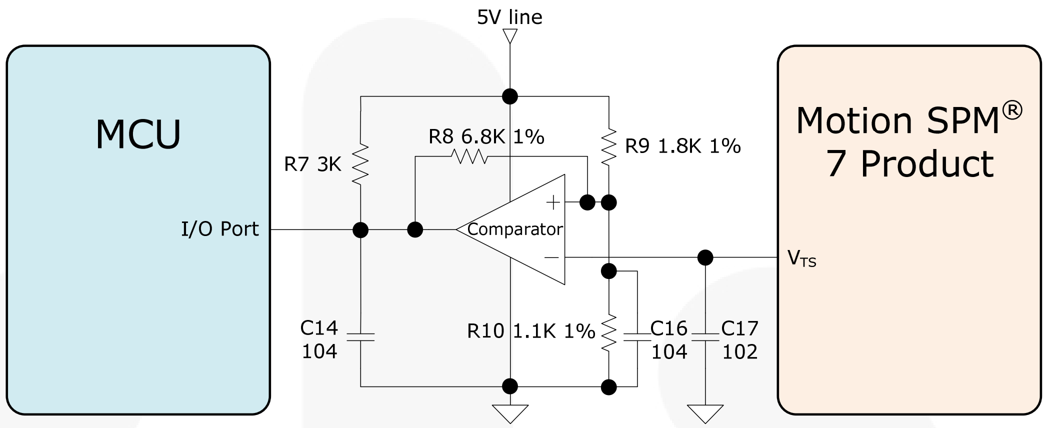

Figure 9. Temperature Sensing Circuit using I/O Port in MCU Example

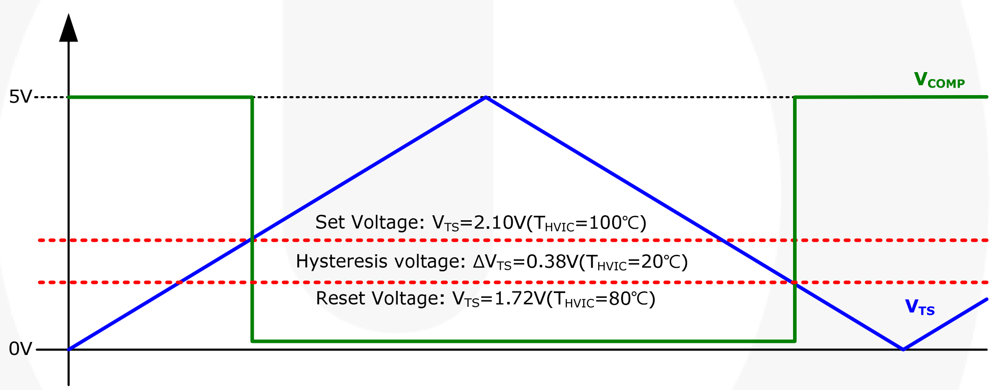

Figure 10. Timing Chart of Temperature Sensing Circuit

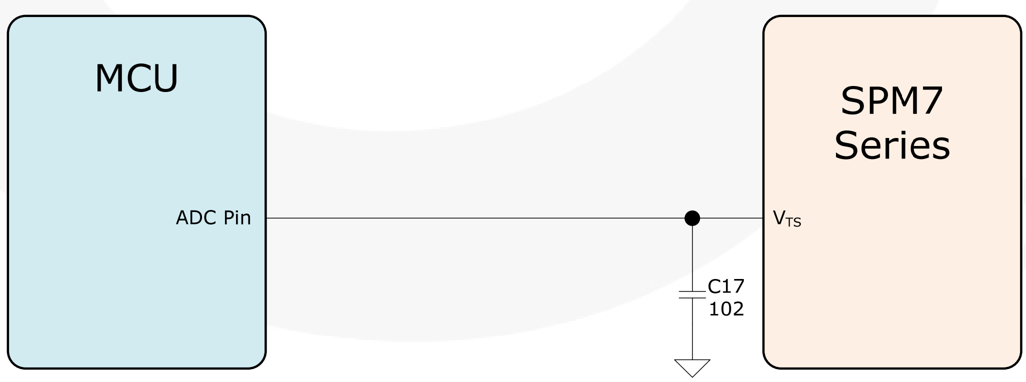

Figure 11. Temperature Sensing Circuit using ADC Port in MCU Example

5.5. Interlock Function

The Motion SPM® 7 Series has an interlock function to prevent shoot-through when high- and low-side input, HIN and LIN, are placed in HIGH status at the same time.

The behavior of the interlock function, based on the one-leg diagram in Figure 12 Is shown in Table 2 and Figure 13.

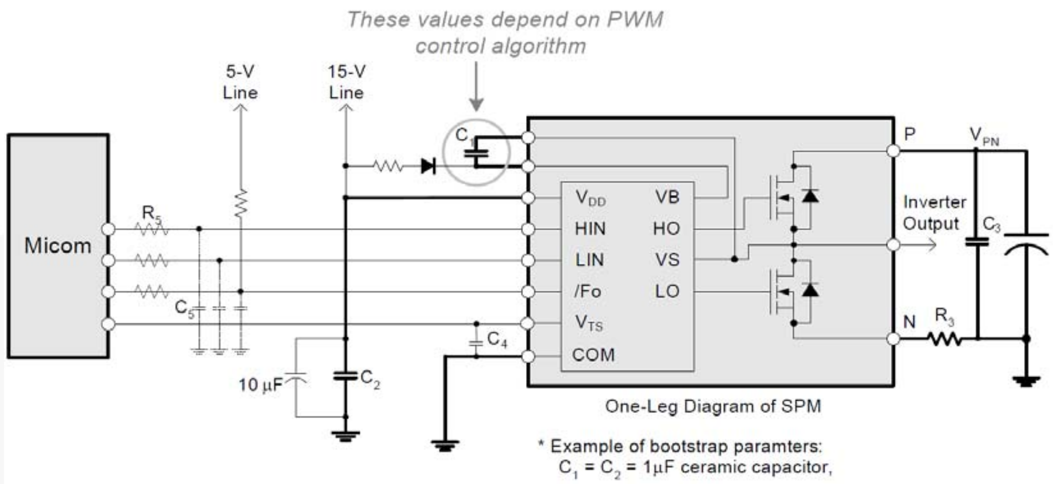

Figure 12. One-Leg Diagram of Motion SPM® 7 Series

Table 2. Logic Table for Inverter Output

HIN	LIN	Output	Status
0	0	Z	Both MOSFETs OFF
0	1	0	Low-Side MOSFET ON
1	0	V_{DC}	High-Side MOSFET ON
1	1	Forbidden	Interlock *(refer to Figure 13)*
Open	Open	Z	Same as (0,0)

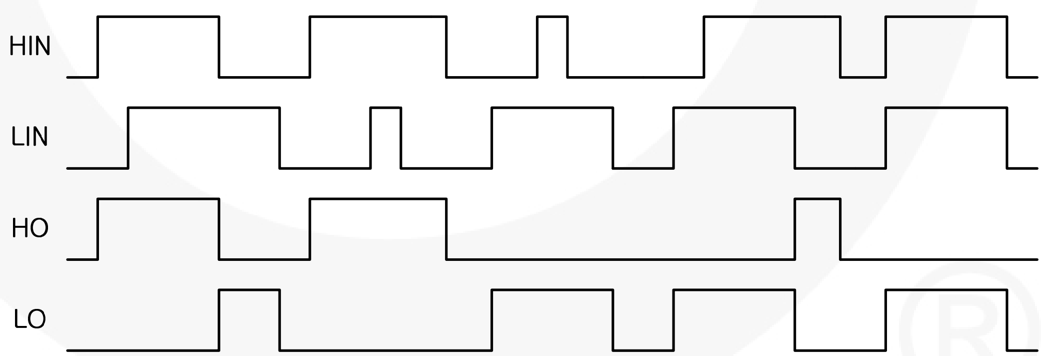

Figure 13. Timing Chart for the Input and Output of HVIC

5.6. Selection of C_{FOD}

The external capacitor connected between the C_{FOD} and COM pins determines the fault output duration (t_{FOD}).

t_{FOD} can be calculated by the following approximate equation:

$$t_{FOD} = C_{FOD} \,/\, (24 \times 10^{-6}) \ \ [s] \qquad (13)$$

5.7. Printed Circuit Board (PCB) Layout Guidance

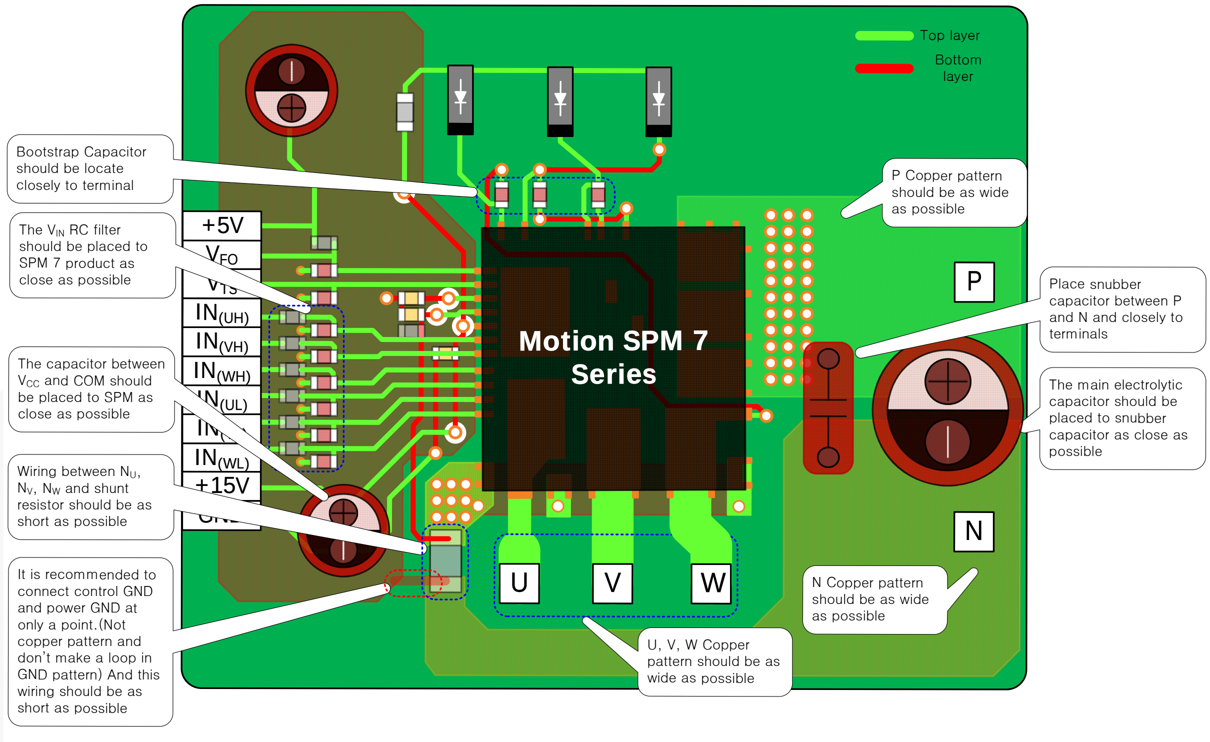

Figure 14. PCB Layout Guidance

Related Resources

AN-9077: Motion SPM® 7 Series Assembly Guide

AN-9078: Motion SPM® 7 Series Assembly Guide

FSB70325 − Motion SPM® 7 Series

FSB70625 − Motion SPM® 7 Series

FSB70250 − Motion SPM® 7 Series

FSB70450 − Motion SPM® 7 Series

FSB70550 − Motion SPM® 7 Series

SPM® Module Design Guide

Motion Control Design Tool