PHOTO OF THE PROTOTYPE

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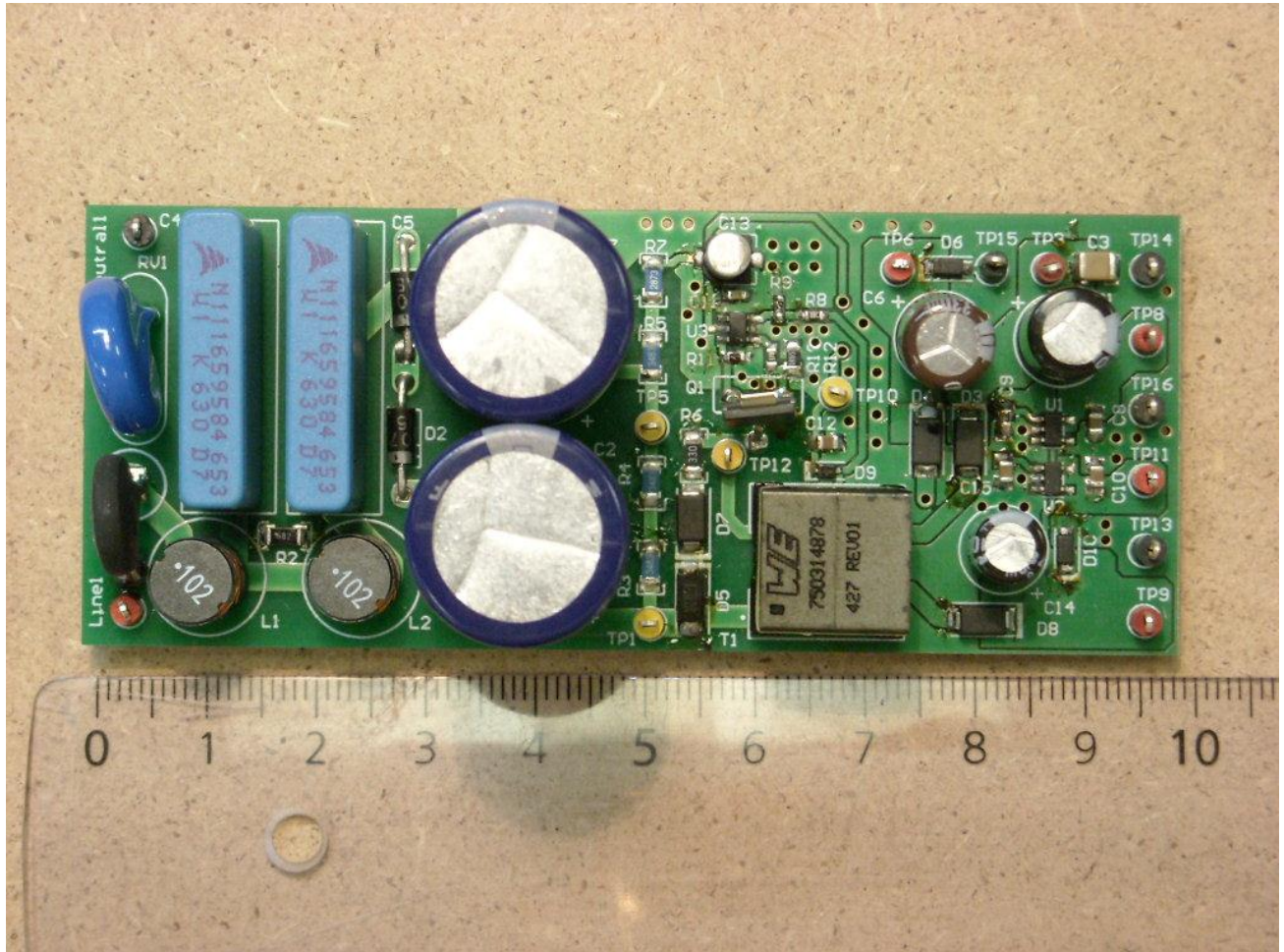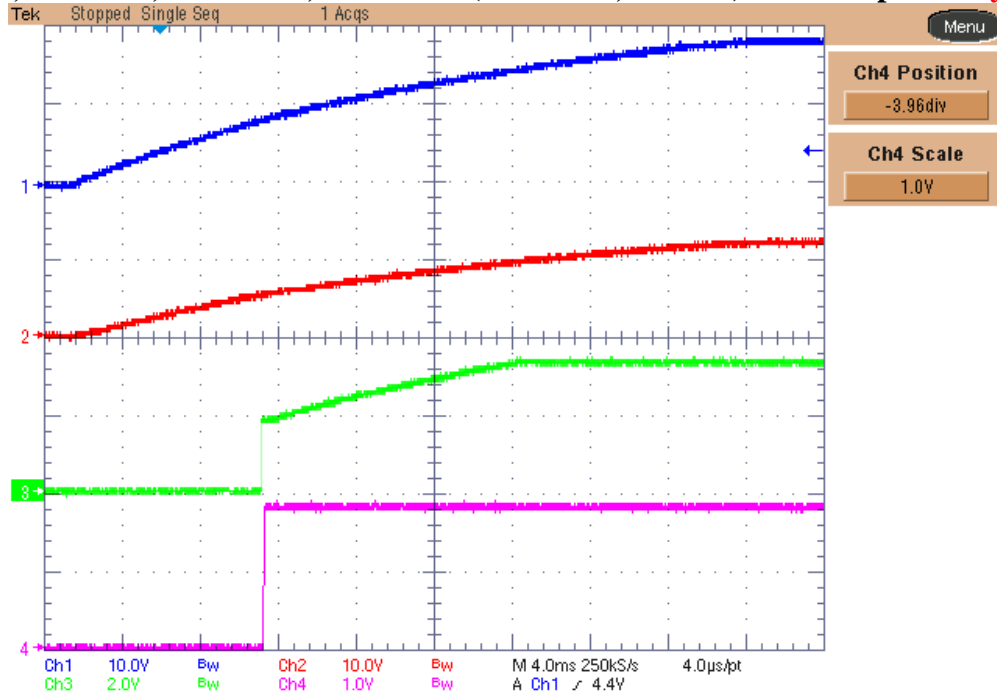
1   Output Voltage at Startup

The output voltage ramp-up behavior for all outputs is shown in the pictures below. The input voltage has been set to 325Vdc. In the upper picture all outputs have been fully loaded, while for the bottom one no load has been applied.

Ch1: 18V, Ch2:12V, Ch3: 3.3V, Ch4: 1.8V (4msec/div, 20MHz) → all outputs fully loaded


Ch1: 18V, Ch2:12V, Ch3: 3.3V, Ch4: 1.8V (4msec/div, 20MHz) → all outputs unloaded

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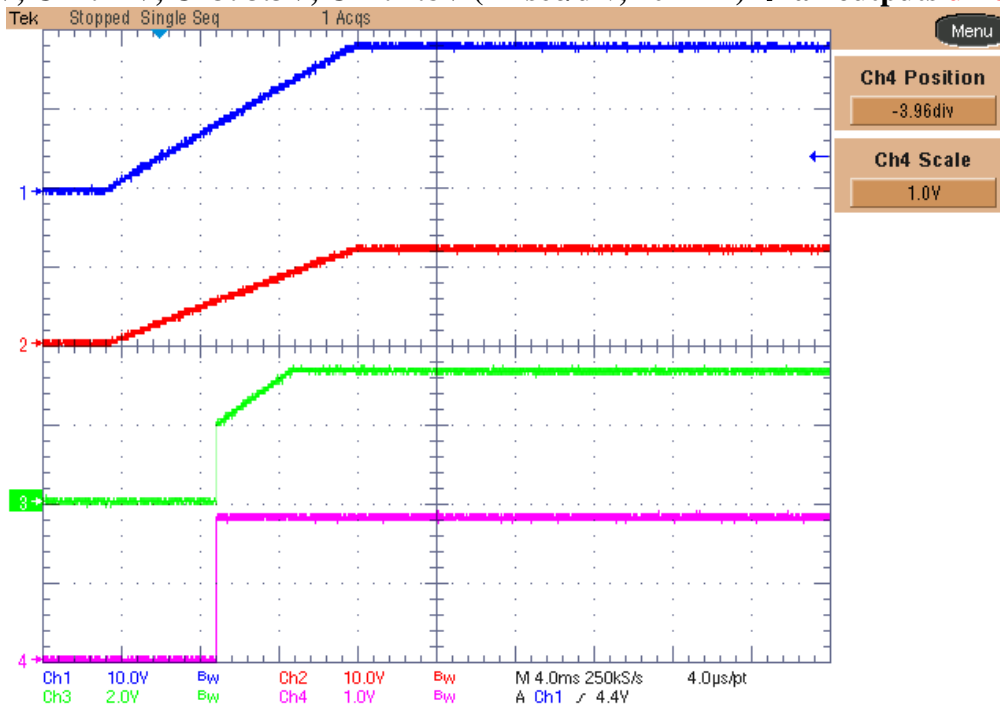
2 Efficiency

The efficiency data are shown in the tables and graphs below. All outputs have been loaded proportionally. The input voltage has been set to 200Vdc, 325Vdc and 375V (equivalent to the rectified 141Vac, 230Vac and 265Vac).
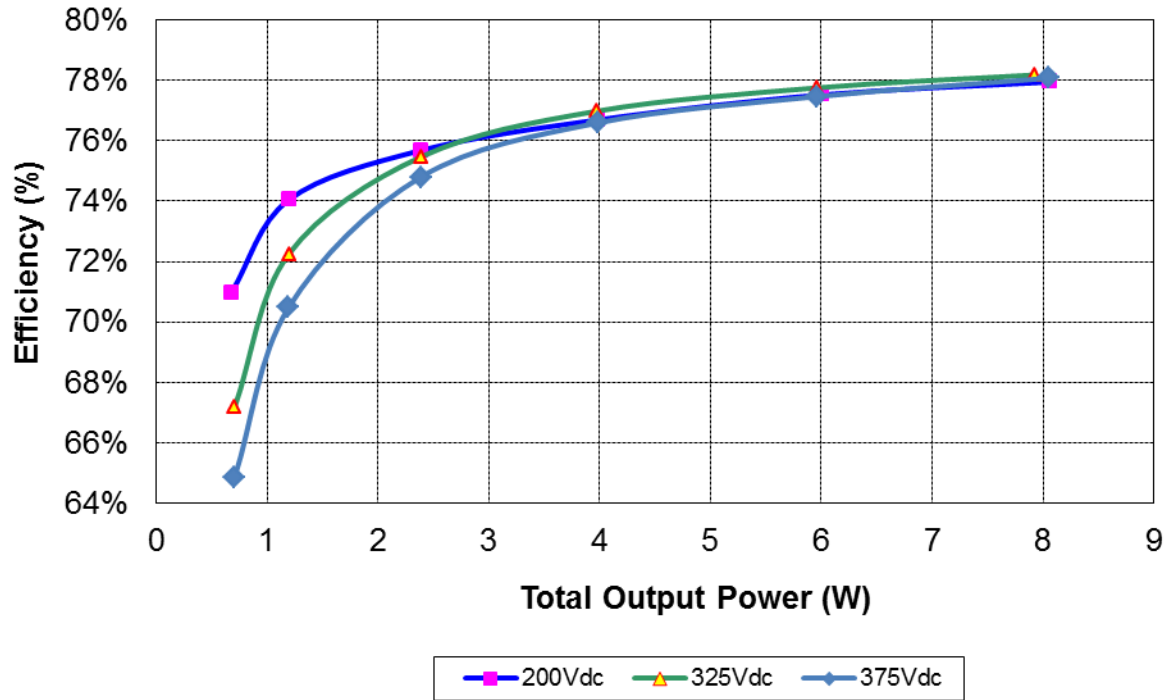
Vin (Vdc)	Iin (mA)	Pin (W)	V18 (V)	I18 (mA)	V12 (V)	I12 (mA)	V3.3 (V)	I3.3 (mA)	V1.8 (V)	I1.8 (mA)	Pout (W)	Ploss (W)	Eff (%)
200	0.198	0.040	18.31	0	12.56	0	3.303	0	1.802	0	0.000	0.040	0.0%
200	4.76	0.952	18.32	18.1	11.98	24.3	3.303	12.3	1.802	6.8	0.676	0.276	71.0%
200	8.08	1.616	18.35	30.3	11.97	45.7	3.303	21.8	1.802	12.0	1.197	0.419	74.1%
200	15.78	3.156	18.36	60.4	11.96	91.1	3.304	44.4	1.803	24.1	2.389	0.767	75.7%
200	25.98	5.196	18.37	101.9	11.97	150.0	3.304	74.2	1.803	40.3	3.985	1.211	76.7%
200	38.74	7.748	18.36	153.3	11.96	227.4	3.305	110.3	1.803	60.0	6.007	1.741	77.5%
200	51.70	10.340	18.37	208.0	11.95	302.3	3.305	146.2	1.804	79.6	8.060	2.280	78.0%

Vin (Vdc)	Iin (mA)	Pin (W)	V18 (V)	I18 (mA)	V12 (V)	I12 (mA)	V3.3 (V)	I3.3 (mA)	V1.8 (V)	I1.8 (mA)	Pout (W)	Ploss (W)	Eff (%)
325	0.265	0.086	18.34	0	12.55	0	3.303	0	1.802	0	0.000	0.086	0.0%
325	3.24	1.052	18.33	18.1	11.96	26.9	3.304	12.3	1.803	6.8	0.706	0.345	67.2%
325	5.09	1.654	18.33	30.3	11.95	45.7	3.304	21.8	1.803	12.0	1.195	0.459	72.2%
325	9.75	3.169	18.36	60.6	11.96	91.1	3.304	44.2	1.803	24.1	2.392	0.777	75.5%
325	15.89	5.164	18.37	101.4	11.97	150.0	3.304	74.2	1.803	40.2	3.976	1.188	77.0%
325	23.60	7.670	18.39	150.6	11.97	227.4	3.305	110.3	1.803	60.0	5.964	1.706	77.8%
325	31.18	10.134	18.39	200.0	11.97	302.3	3.305	146.2	1.803	79.6	7.923	2.210	78.2%

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| Vin (Vdc)	Iin (mA)	Pin (W)	V18 (V)	I18 (mA)	V12 (V)	I12 (mA)	V3.3 (V)	I3.3 (mA)	V1.8 (V)	I1.8 (mA)	Pout (W)	Ploss (W)	Eff (%)
375	0.298	0.112	18.34	0	12.61	0	3.304	0	1.803	0	0.000	0.112	0.0%
375	2.91	1.089	18.33	18.1	11.96	26.9	3.304	12.3	1.803	6.8	0.706	0.383	64.8%
375	4.52	1.695	18.33	30.3	11.95	45.7	3.303	21.7	1.803	11.9	1.195	0.500	70.5%
375	8.51	3.191	18.35	60.4	11.96	91.1	3.304	44.2	1.803	24.0	2.387	0.804	74.8%
375	13.88	5.205	18.37	102.0	11.97	150.0	3.304	74.2	1.803	40.3	3.987	1.218	76.6%
375	20.53	7.699	18.39	150.6	11.97	227.4	3.305	110.3	1.803	60.0	5.964	1.735	77.5%
375	27.50	10.313	18.38	207.1	11.97	302.3	3.305	146.2	1.803	79.6	8.052	2.261	78.1%

3   Output Voltage Regulation vs. Load

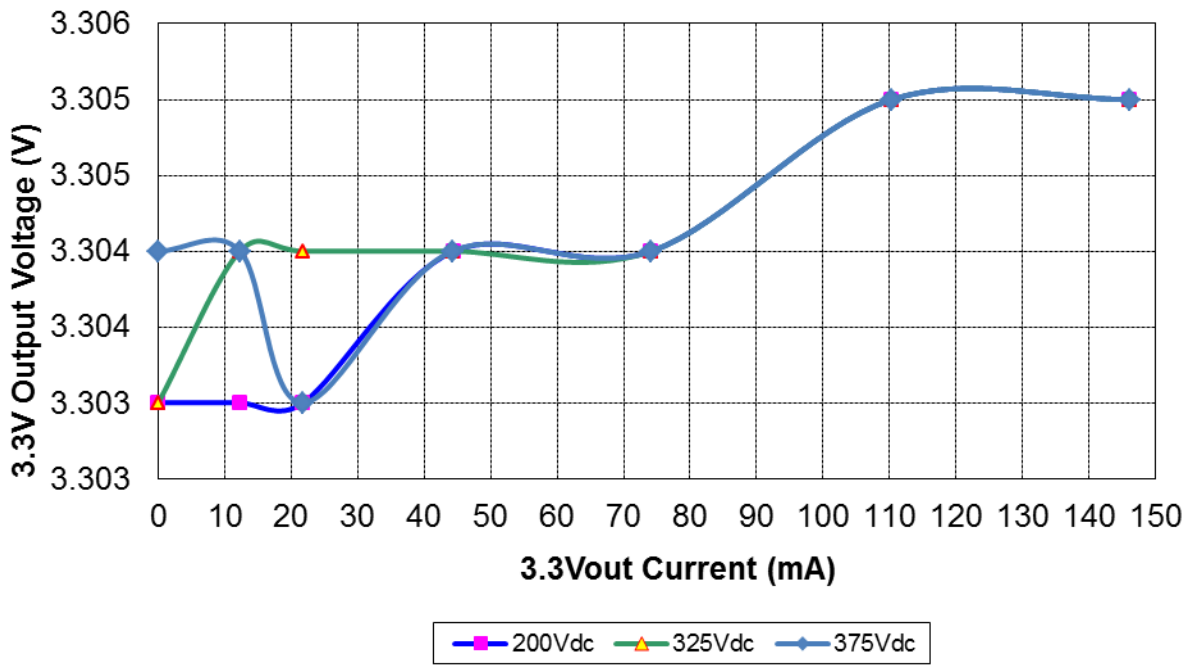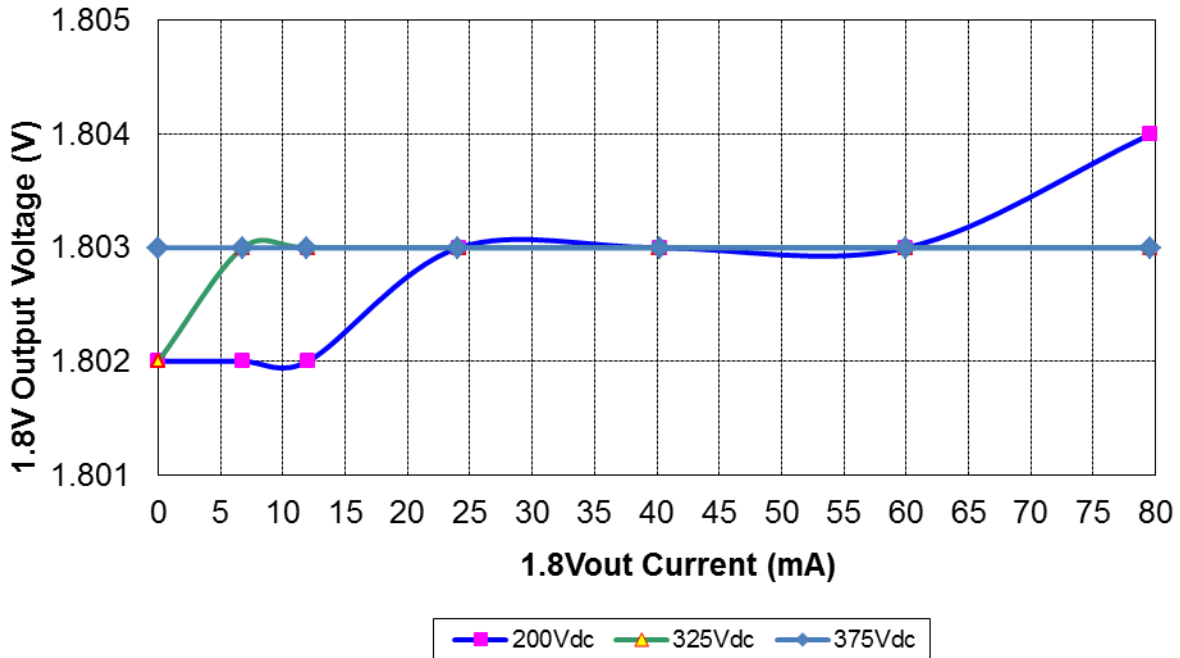All output voltages variation versus their own loads has been plotted in the graphs below.

18Vout:

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12Vout:

3.3Vout:

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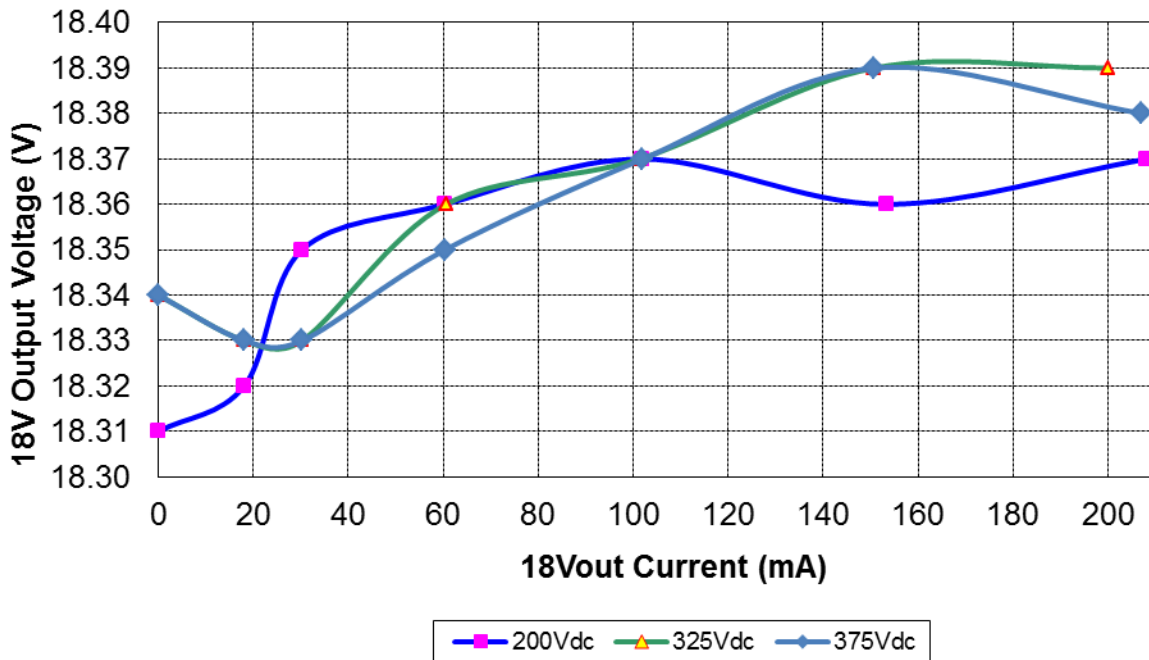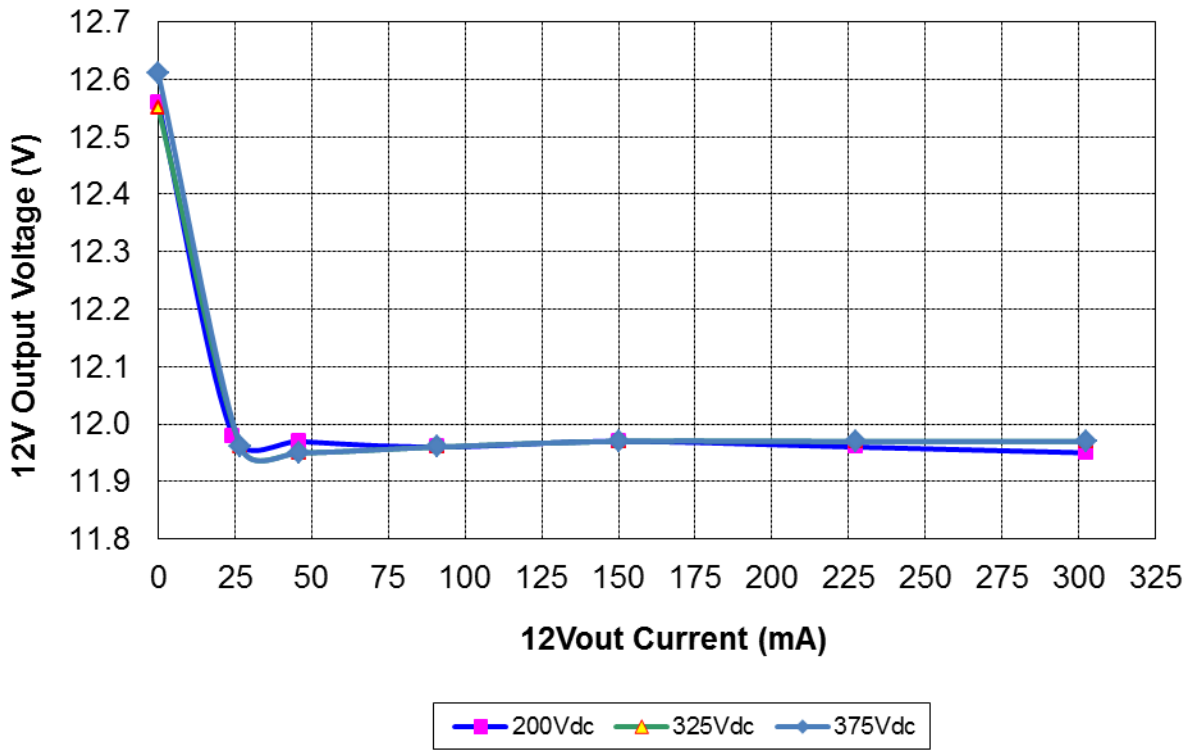
1.8Vout:

4   Cross regulation

4.1   Minimum current on 18Vout to get 3.3V @ 150mA and 1.8V @ 40mA under regulation: No minimum current required on 18Vout.

4.2   With 3.3V loaded @ 150mA, 1.8V loaded @ 40mA, 18Vout unloaded and 12V unloaded: the voltage on the 18V output goes to 21.77V; it reduces to 20.6V if loaded @ 18mA. The 12V output goes to 13.94V.

5   Switching Node Waveforms

The image below shows the voltage on switch node collector of Q1 at 325Vdc input voltage and full load conditions.
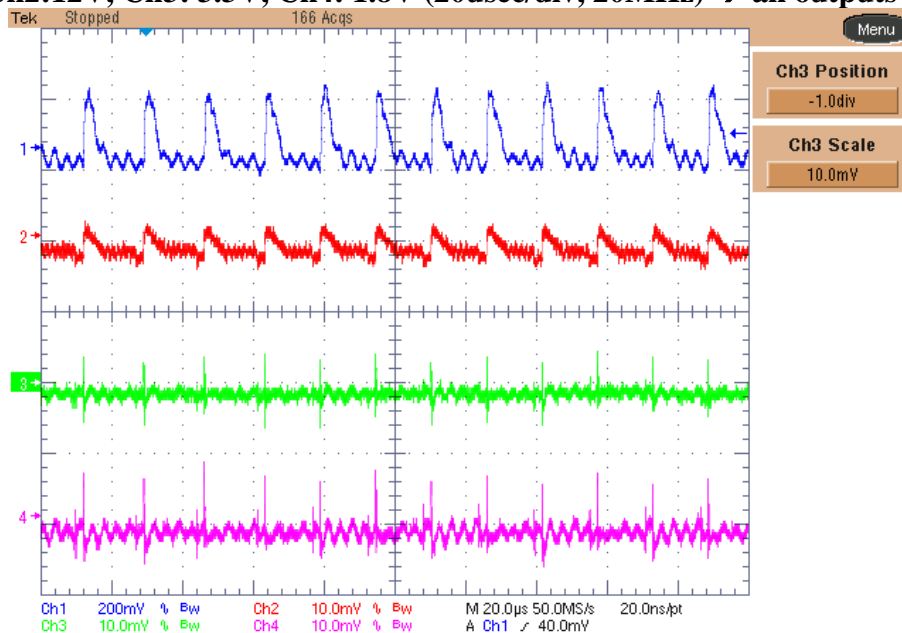**Ch3: Collector of Q1 (100V/div, 4usec/div, No BWL)**
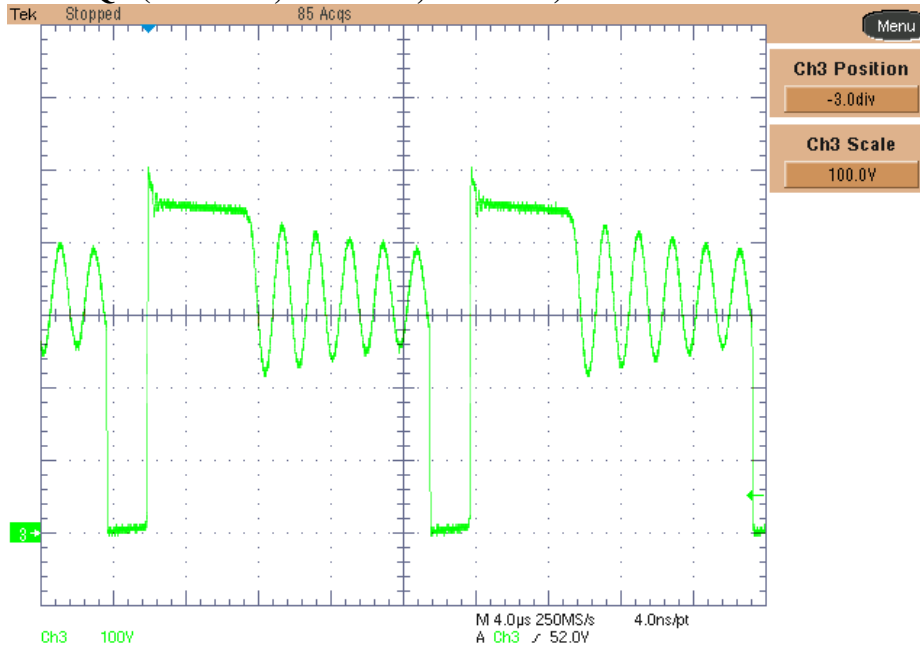
6   Output Ripple Voltages

The output ripple voltages on all outputs @ 325Vdc input voltage are shown below.
**Ch1: 18V, Ch2:12V, Ch3: 3.3V, Ch4: 1.8V (20usec/div, 20MHz) → all outputs fully loaded**

7 Transient Response on 12Vout

The 12V output voltage variation versus transient load is shown below. The input voltage has been set to 325Vdc and the load switched between 0A and 600mA for the upper picture and 50mA to 600mA for the bottom one..

Ch1: 12Vout (500mV/div, 1msec/div, AC, 20MHz), Ch4: 12Iout (200mA/div, DC, 20MHz)
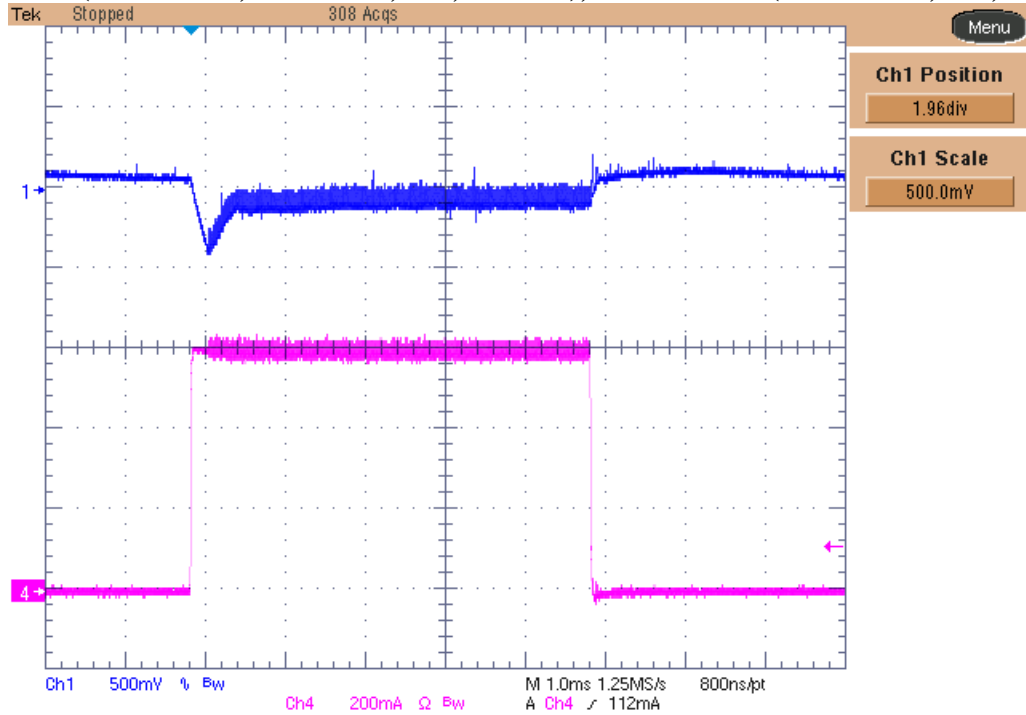
Ch1: 12Vout (200mV/div, 2msec/div, AC, 20MHz), Ch4: 12Iout (200mA/div, DC, 20MHz)

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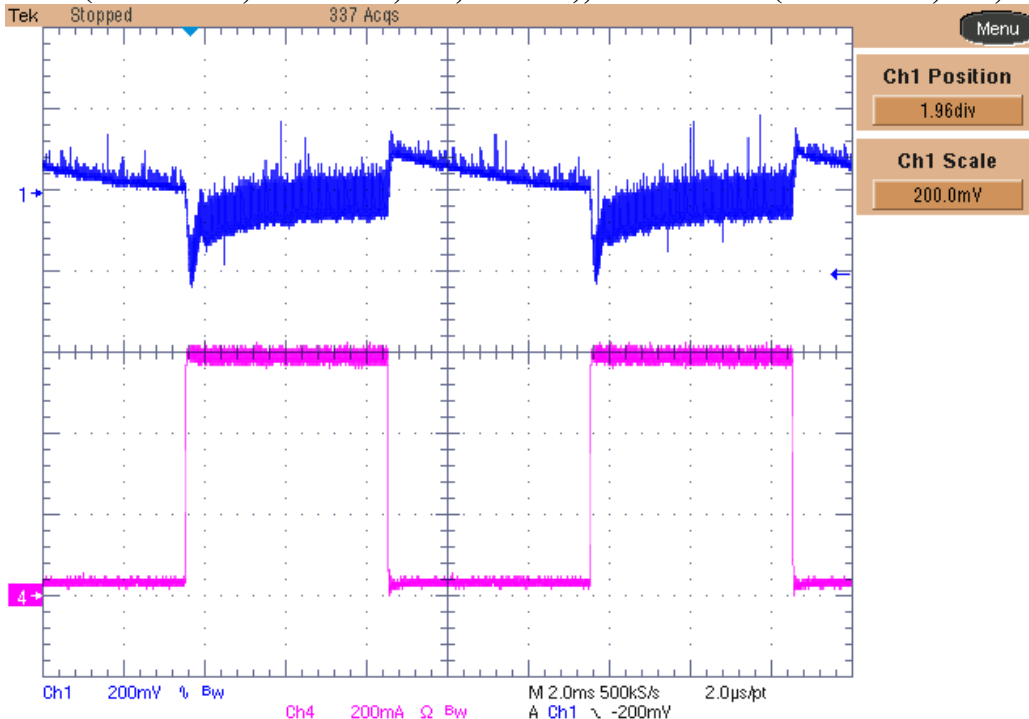
8   Holdup

The holdup time of the converter has been measured by applying 212Vdc on the input, equivalent to 150Vac, and then disconnecting it. The load was set to 1W distributed into the 3.3V and 1.8V outputs. The picture below shows the screenshot at the scope.
Since the result shows 454msec, the electrolytic capacitors on the rectified AC voltage must be increased in order to meet the 500msec required by specs.

Ch3: Input DC voltage (100V/div, 100msec/div)
Ch1: 3.3Vout (2V/div, 20MHz BWL)
Ch2: 1.8Vout (1V/div, 20MHz BWL)
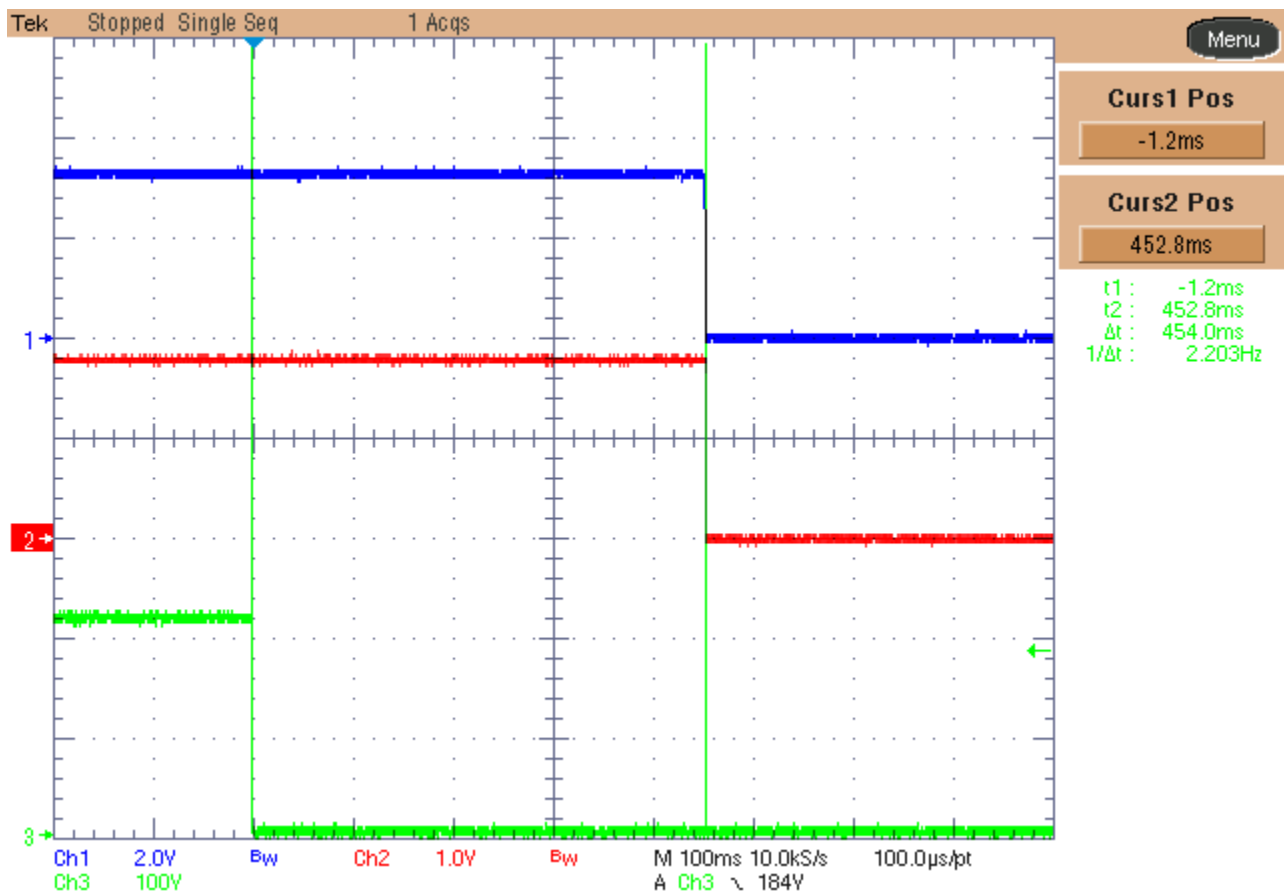
9   Thermal Analysis

The thermal analysis of the converter shows the temperatures for each component, in the graphs below. The converter has been placed horizontally on the bench without any forced convection. The input voltage was 325Vdc for the upper picture and 625Vdc for the bottom one. All outputs were loaded so that the total load was 5W. The ambient temperature was 24C.

Vin = 325Vdc
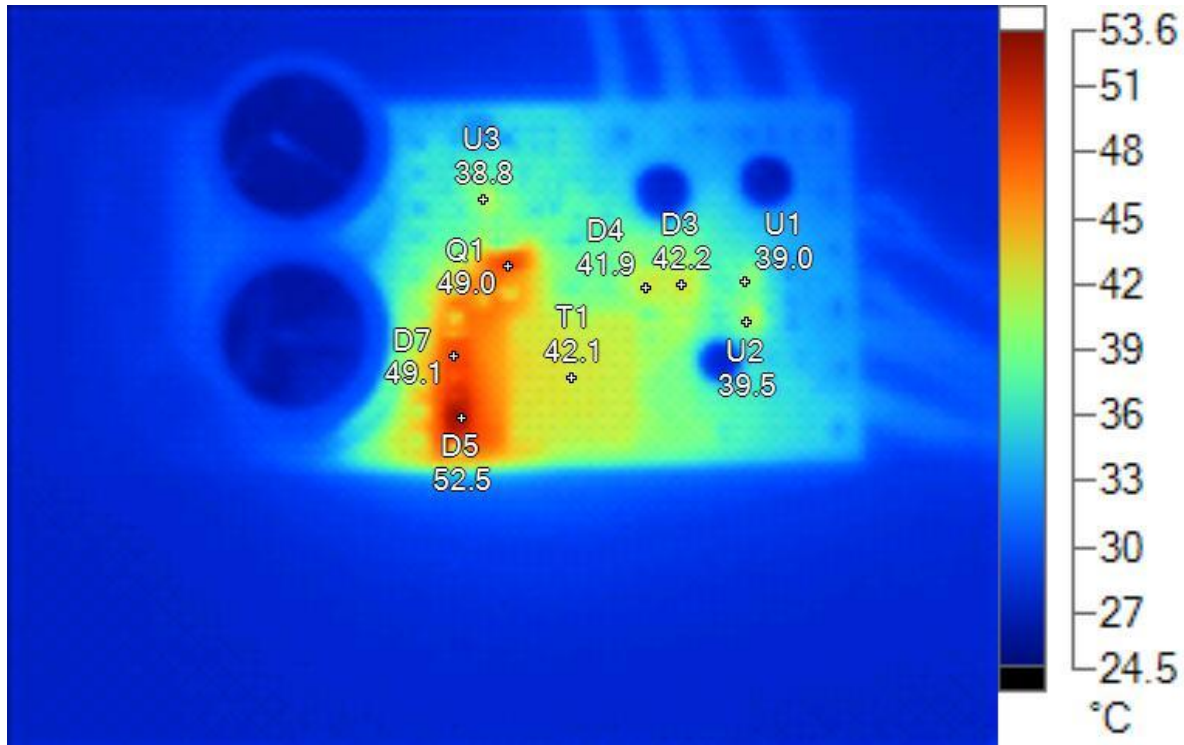
Image Info

Background temperature	24.0°C
Average Temperature	30.3°C
Image Range	25.5°C to 52.6°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	7/24/2014 6:45:04 PM

Main Image Markers

Name	Temperature
D5	52.5°C
Q1	49.0°C
D3	42.2°C
D4	41.9°C
T1	42.1°C
U2	39.5°C
U1	39.0°C
D7	49.1°C
U3	38.8°C

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Vin = 625Vdc
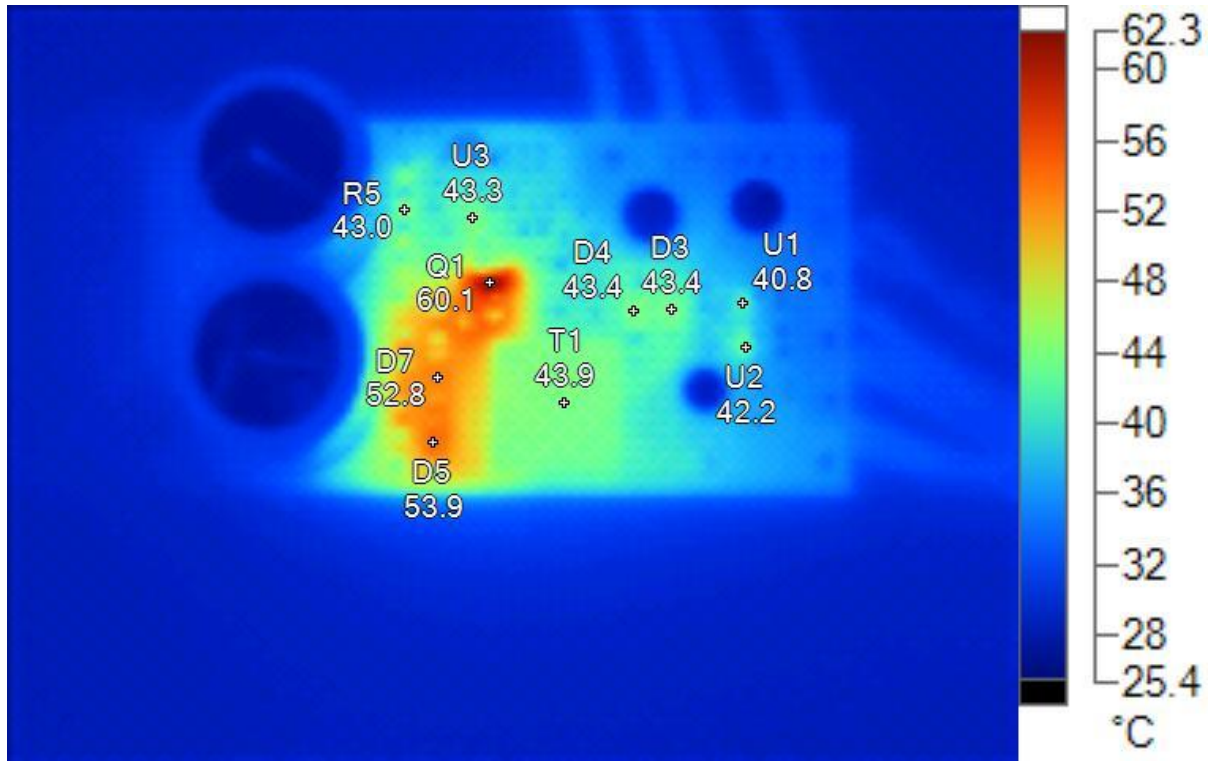
Image Info

Background temperature	24.0°C
Average Temperature	31.6°C
Image Range	26.4°C to 61.1°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	7/24/2014 6:47:07 PM

Main Image Markers

Name	Temperature
D5	53.9°C
D7	52.8°C
Q1	60.1°C
T1	43.9°C
D4	43.4°C
D3	43.4°C
U2	42.2°C
U1	40.8°C
R5	43.0°C
U3	43.3°C

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