Test Data
For PMP9403
4/11/2014

Table of Contents

1. Design Specifications

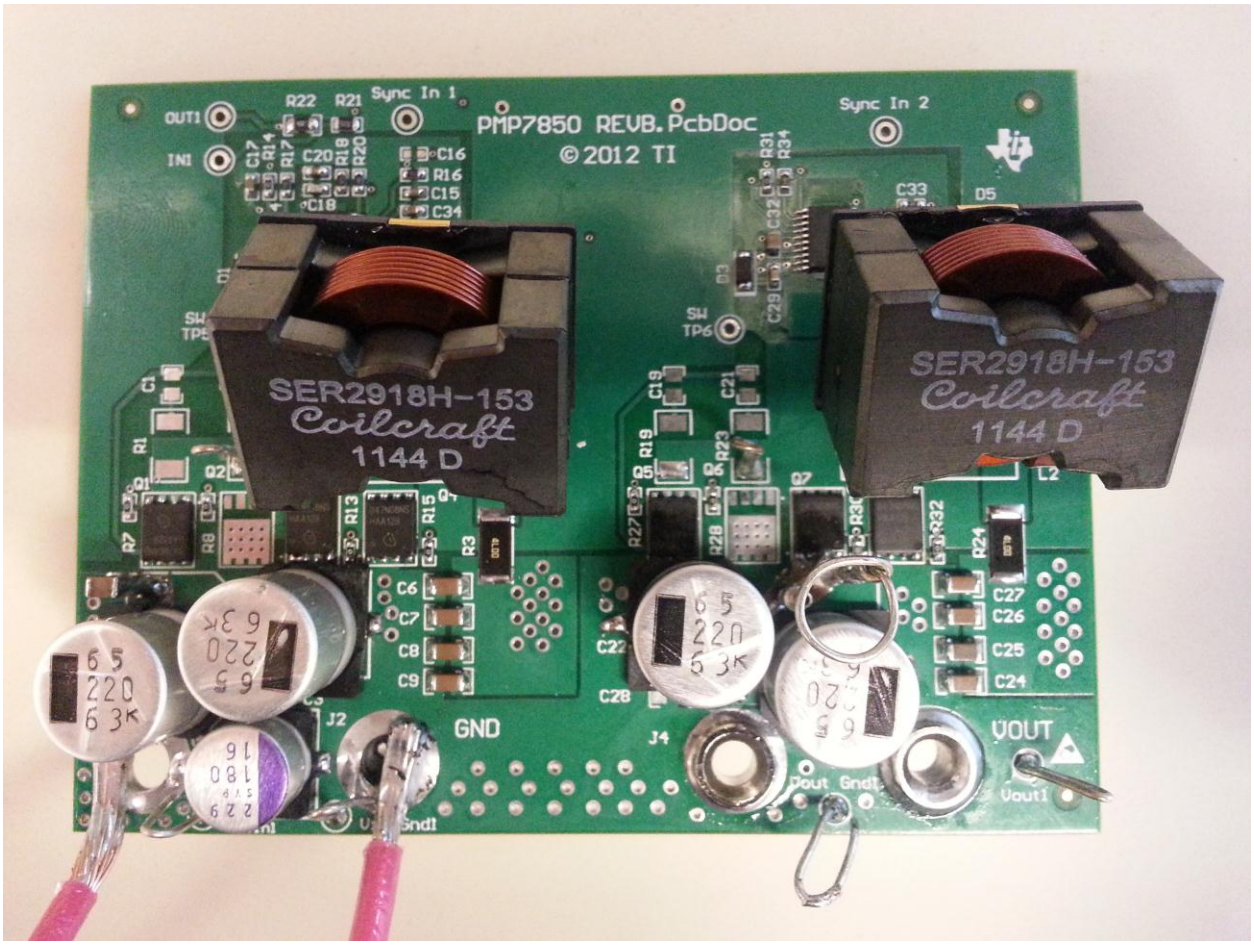
Vin Minimum	**9VDC**
Vin Maximum	**15VDC**
Vout	**48VDC**
Iout	**4A Max.**
Approximate Switching Frequency	**≈ 180KHz per Phase (≈ 360KHz Effective)**

2. Circuit Description

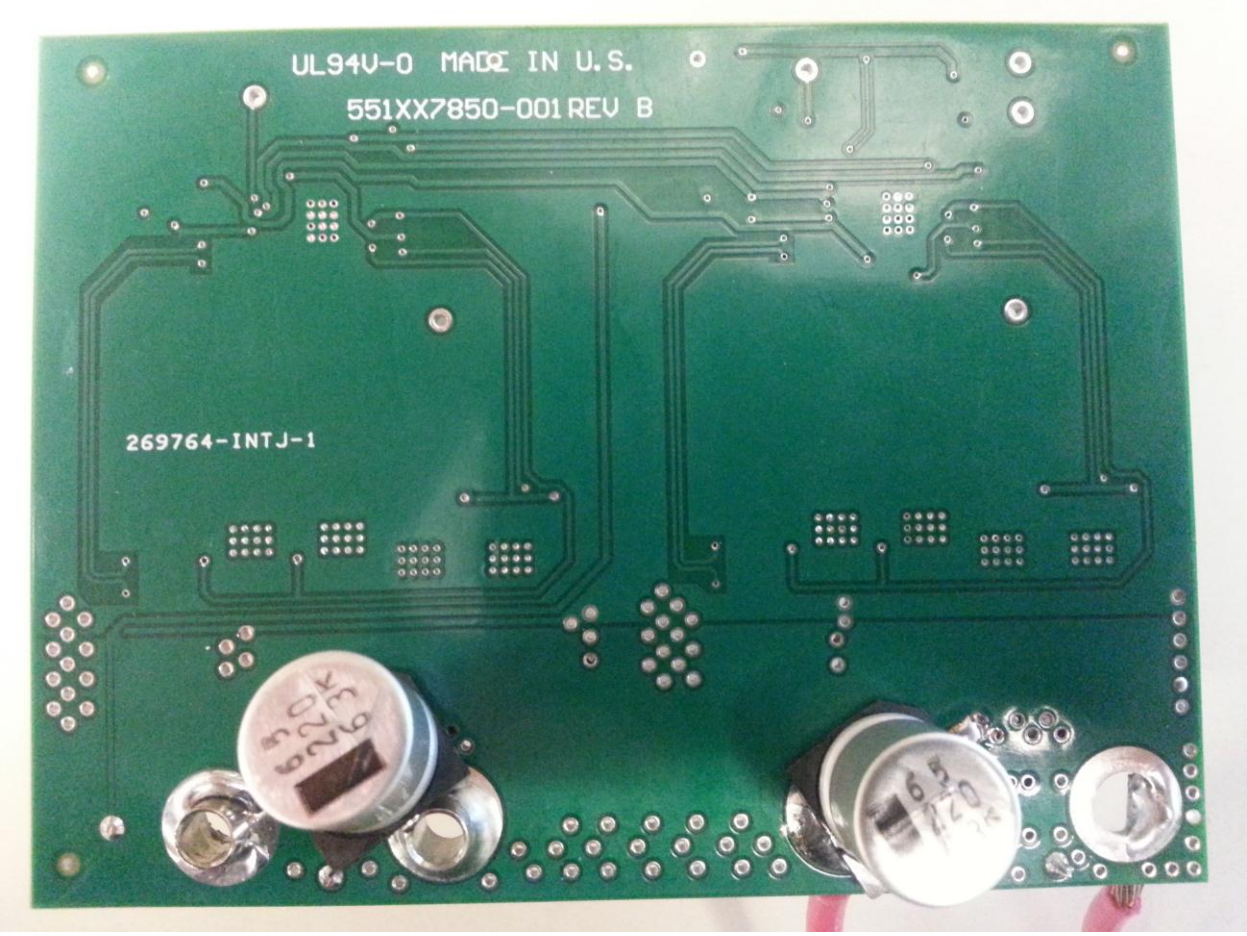
PMP9403 is a Dual-Phase Synchronous Boost Converter using the LM5122 controller IC. The design accepts an input voltage of 9Vin to 15Vin and provides an output of 48Vout capable of supplying a maximum of 4A of current to the load. This design was built on the PMP7850 REVB PCB. All tests in this report were performed at 9Vin, 12Vin, and 15Vin.

3. PMP9403 Board Photos

Board Dimensions: 4” x 3”

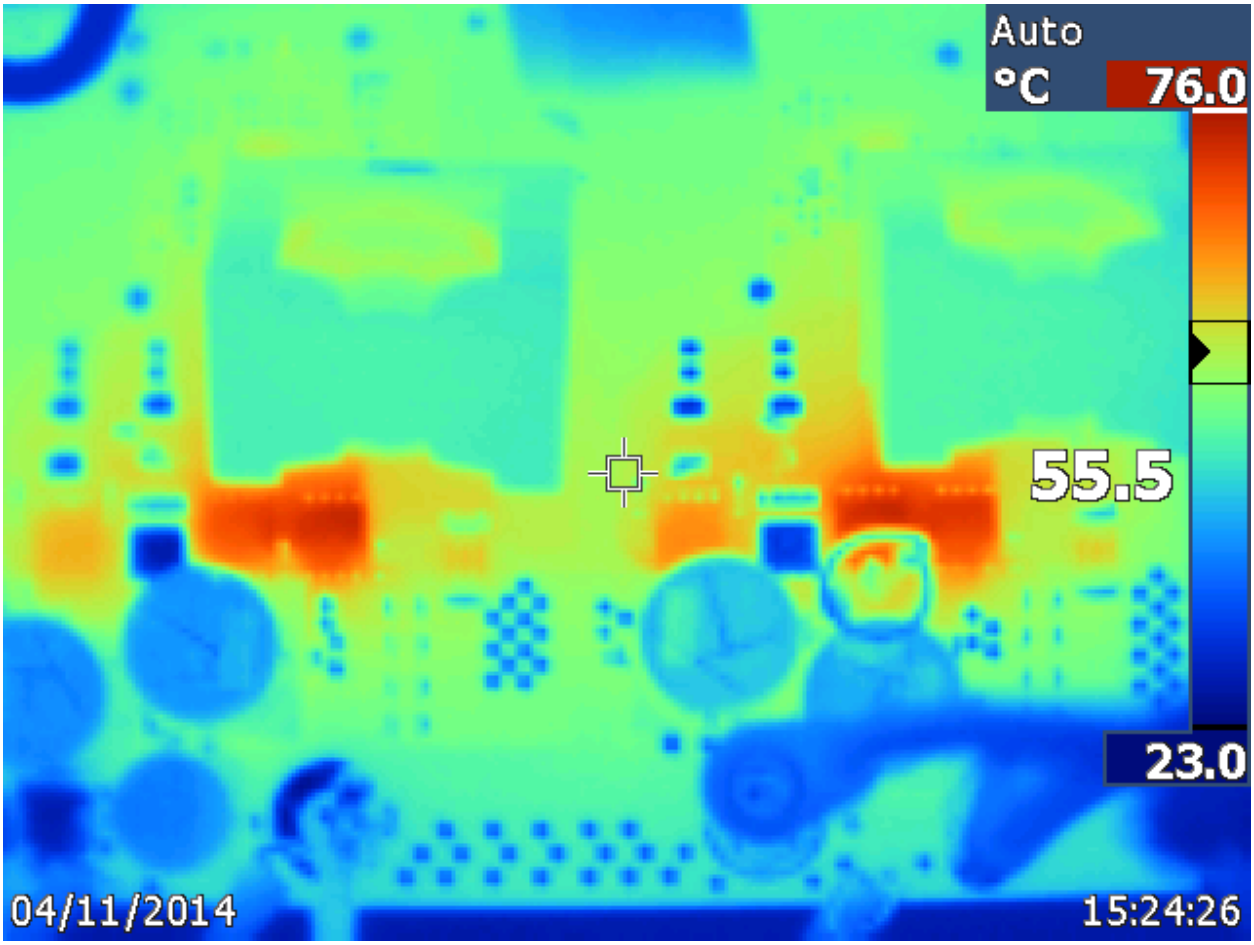


Board Photo (Top)

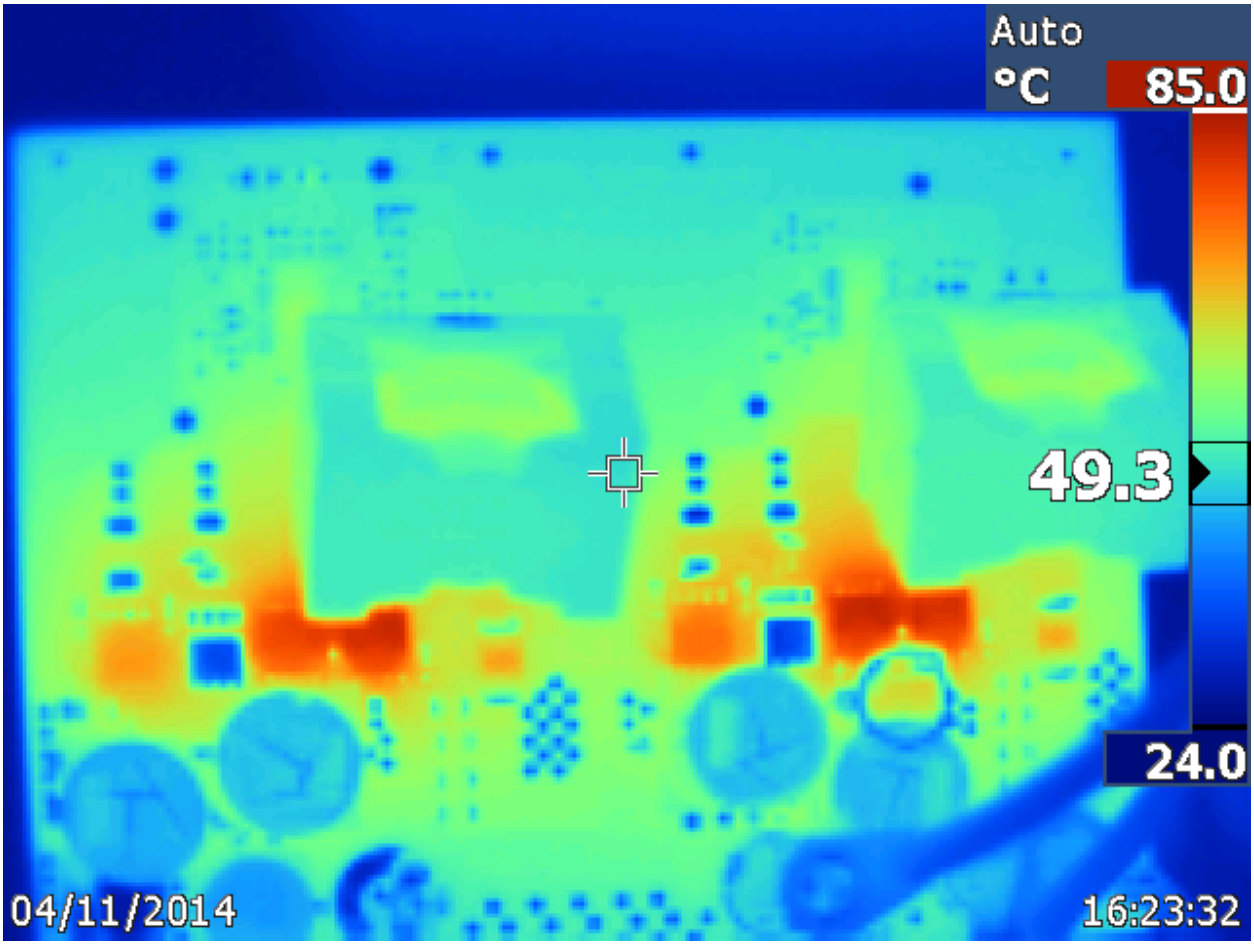


Board Photo (Bottom)

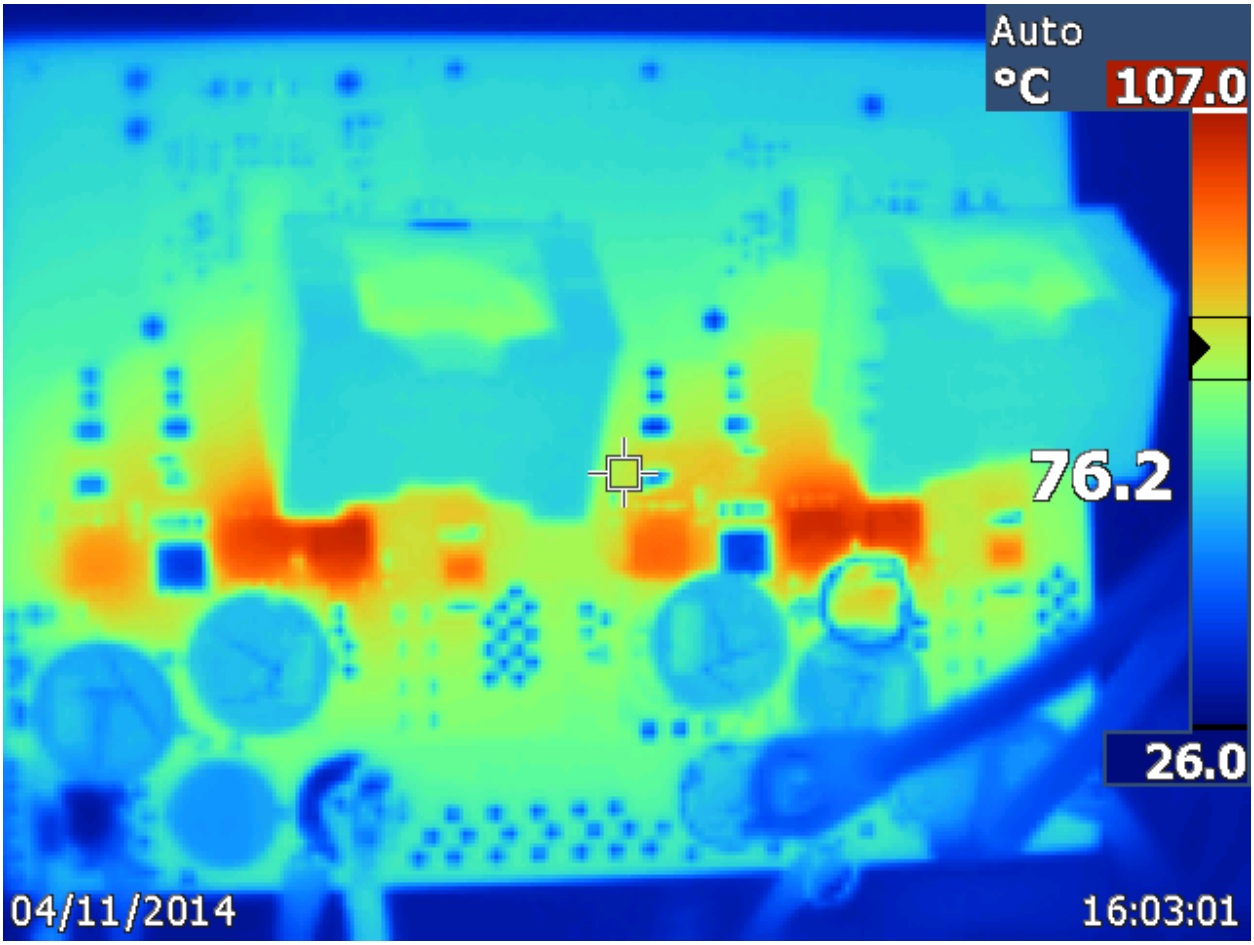
4. Thermal Data



IR thermal image taken at steady state with 15Vin and 4A load (no airflow)



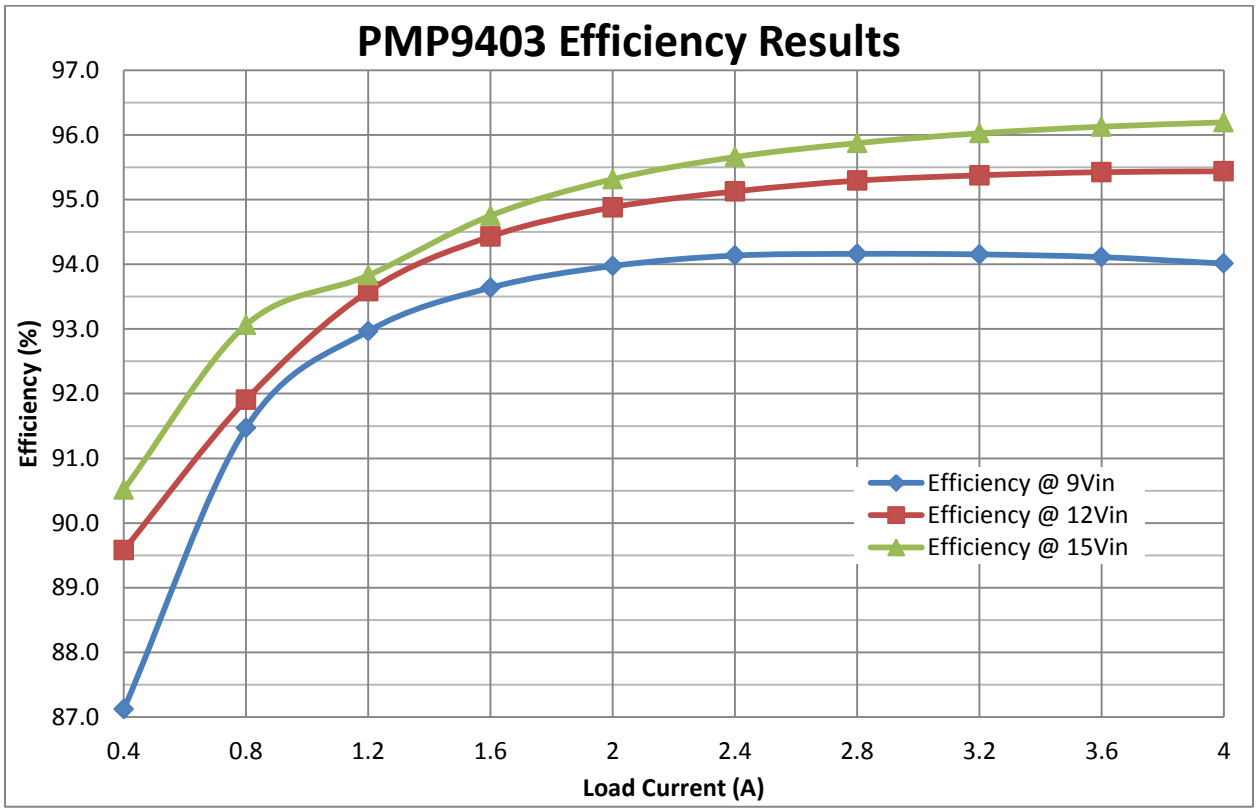
IR thermal image taken at steady state with 12Vin and 4A load (no airflow)



IR thermal image taken at steady state with 9Vin and 4A load (no airflow)

5. Efficiency

5.1 Efficiency Chart



5.2 Efficiency Data

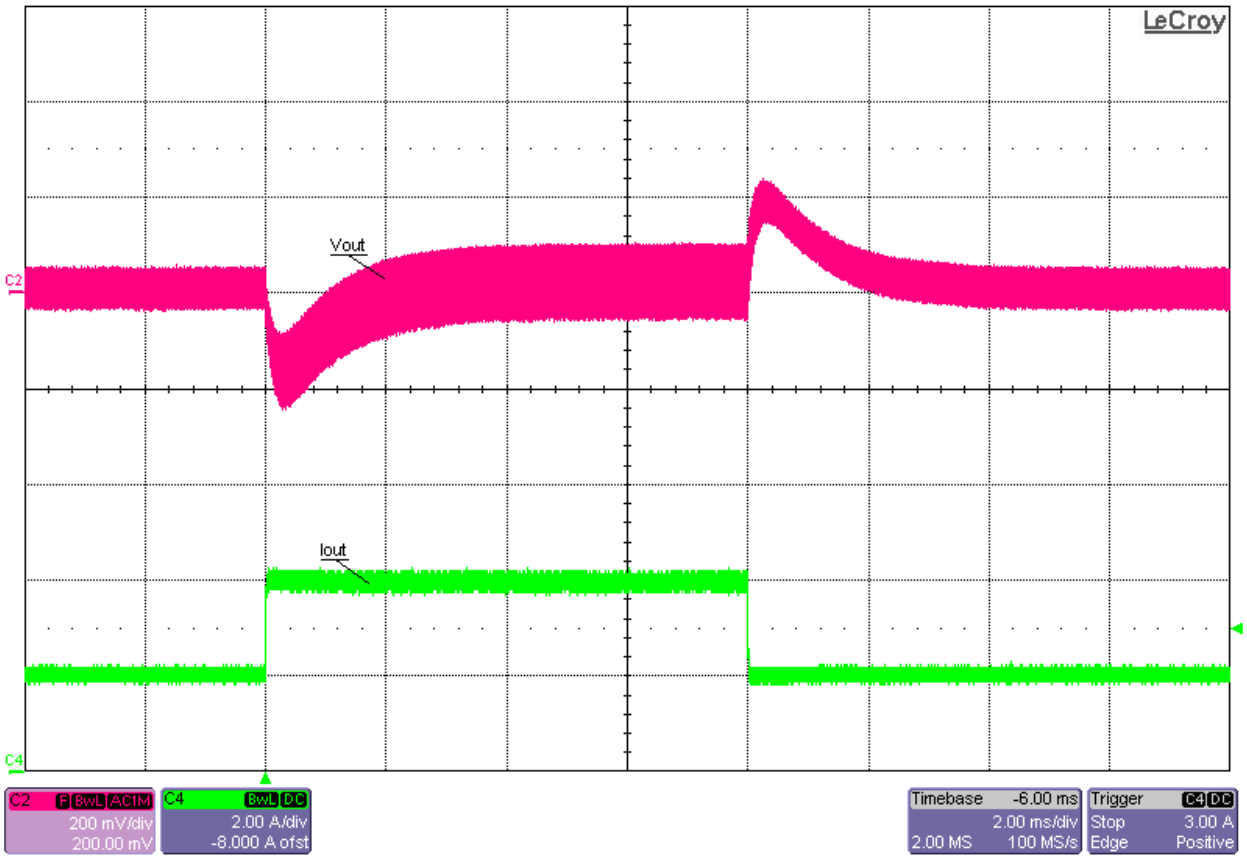
Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Efficiency (%)
9	2.469	48.397	0.4	22.22	19.36	87.1
9	4.703	48.396	0.8	42.33	38.72	91.5
9	6.941	48.396	1.2	62.47	58.08	93.0
9	9.188	48.395	1.6	82.69	77.43	93.6
9	11.444	48.395	2	103.00	96.79	94.0
9	13.709	48.394	2.4	123.38	116.15	94.1
9	15.989	48.393	2.8	143.90	135.50	94.2
9	18.274	48.391	3.2	164.47	154.85	94.2
9	20.567	48.39	3.6	185.10	174.20	94.1
9	22.875	48.387	4	205.88	193.55	94.0

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Efficiency (%)
12	1.801	48.401	0.4	21.61	19.36	89.6
12	3.511	48.401	0.8	42.13	38.72	91.9
12	5.172	48.401	1.2	62.06	58.08	93.6
12	6.834	48.401	1.6	82.01	77.44	94.4
12	8.502	48.401	2	102.02	96.80	94.9
12	10.176	48.401	2.4	122.11	116.16	95.1
12	11.851	48.4	2.8	142.21	135.52	95.3
12	13.532	48.399	3.2	162.38	154.88	95.4
12	15.215	48.397	3.6	182.58	174.23	95.4
12	16.903	48.396	4	202.84	193.58	95.4

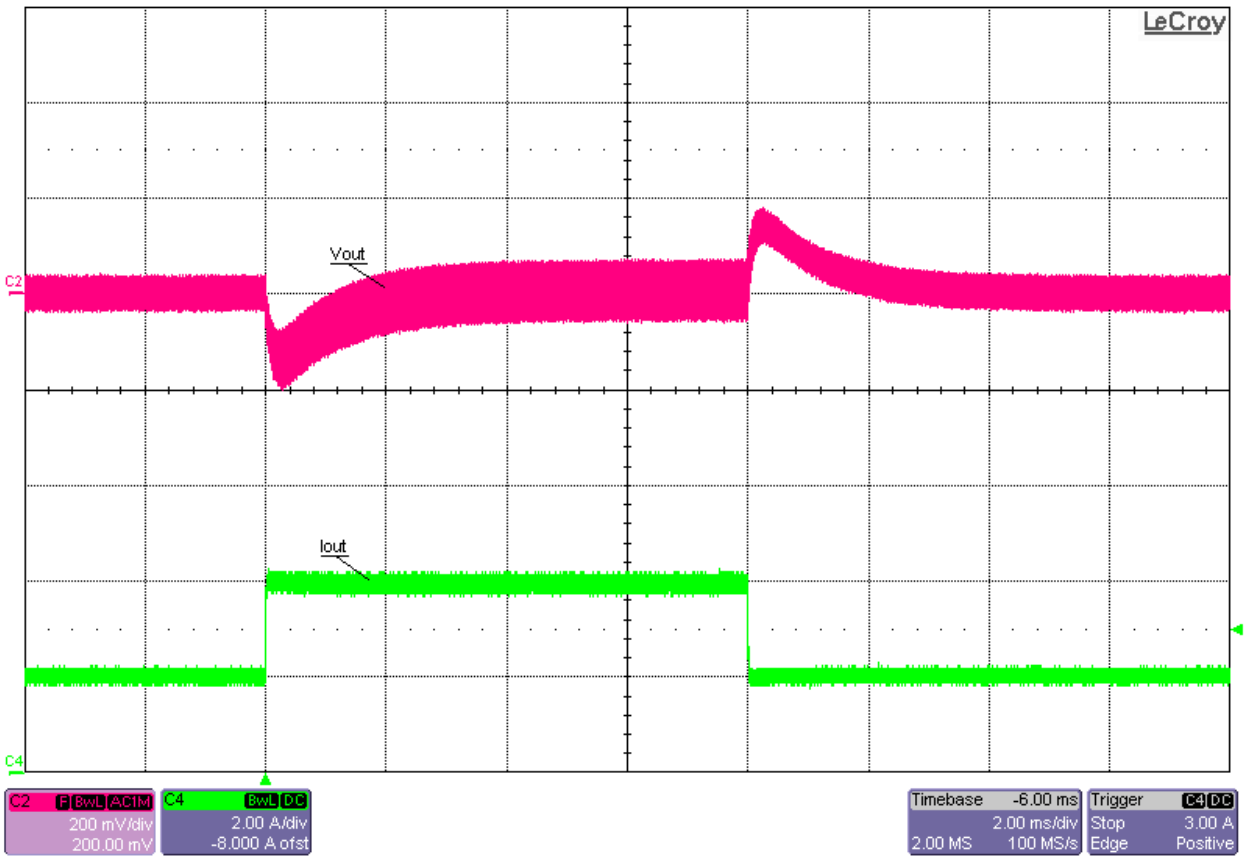
Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Efficiency (%)
15	1.426	48.404	0.4	21.39	19.36	90.5
15	2.774	48.404	0.8	41.61	38.72	93.1
15	4.127	48.404	1.2	61.91	58.08	93.8
15	5.449	48.404	1.6	81.74	77.45	94.8
15	6.771	48.404	2	101.57	96.81	95.3
15	8.096	48.404	2.4	121.44	116.17	95.7
15	9.424	48.403	2.8	141.36	135.53	95.9
15	10.753	48.402	3.2	161.30	154.89	96.0
15	12.084	48.401	3.6	181.26	174.24	96.1
15	13.417	48.4	4	201.26	193.60	96.2

6 Waveforms

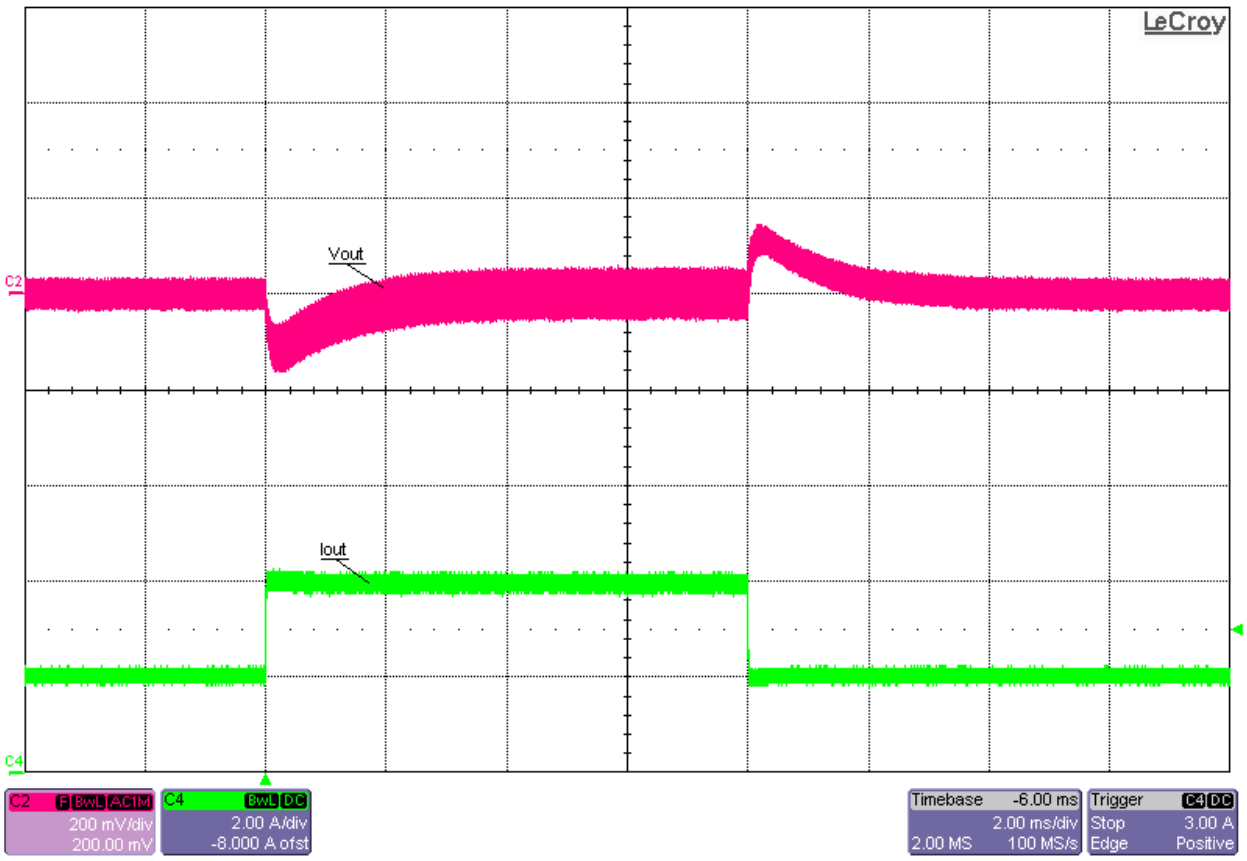
6.1 Load Transient Response



Load Transient Response at 9Vin and 50%-to-100% (2A-to-4A) Load Step

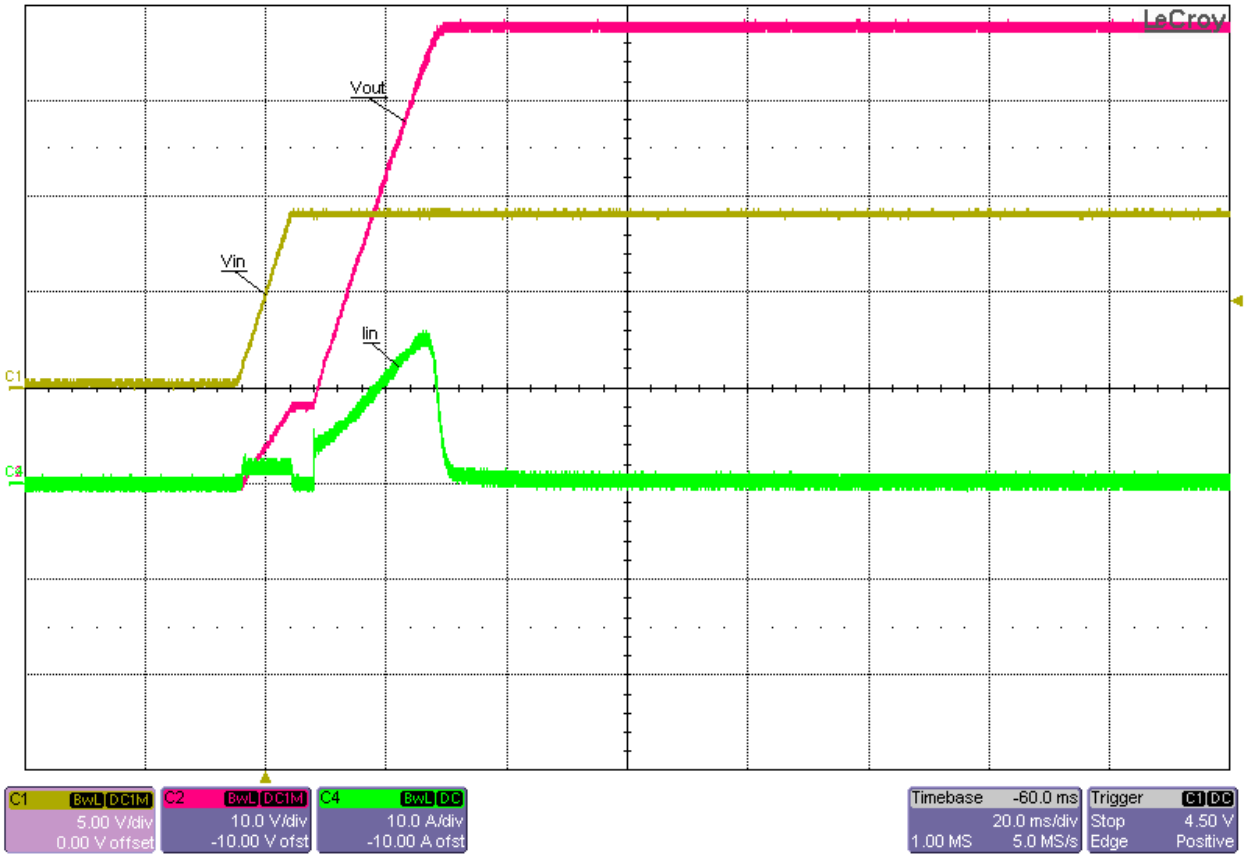


Load Transient Response at 12Vin and 50%-to-100% (2A-to-4A) Load Step

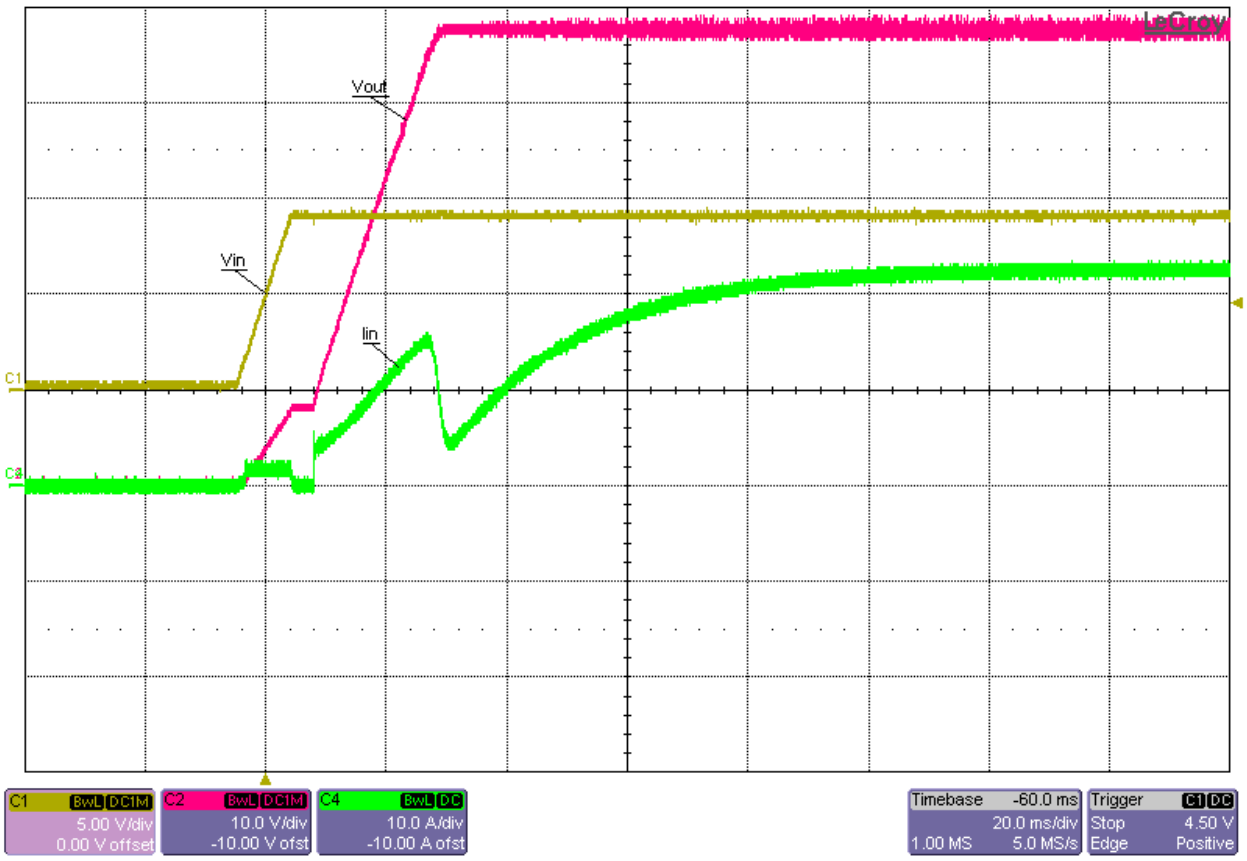


Load Transient Response at 15Vin and 50%-to-100% (2A-to-4A) Load Step

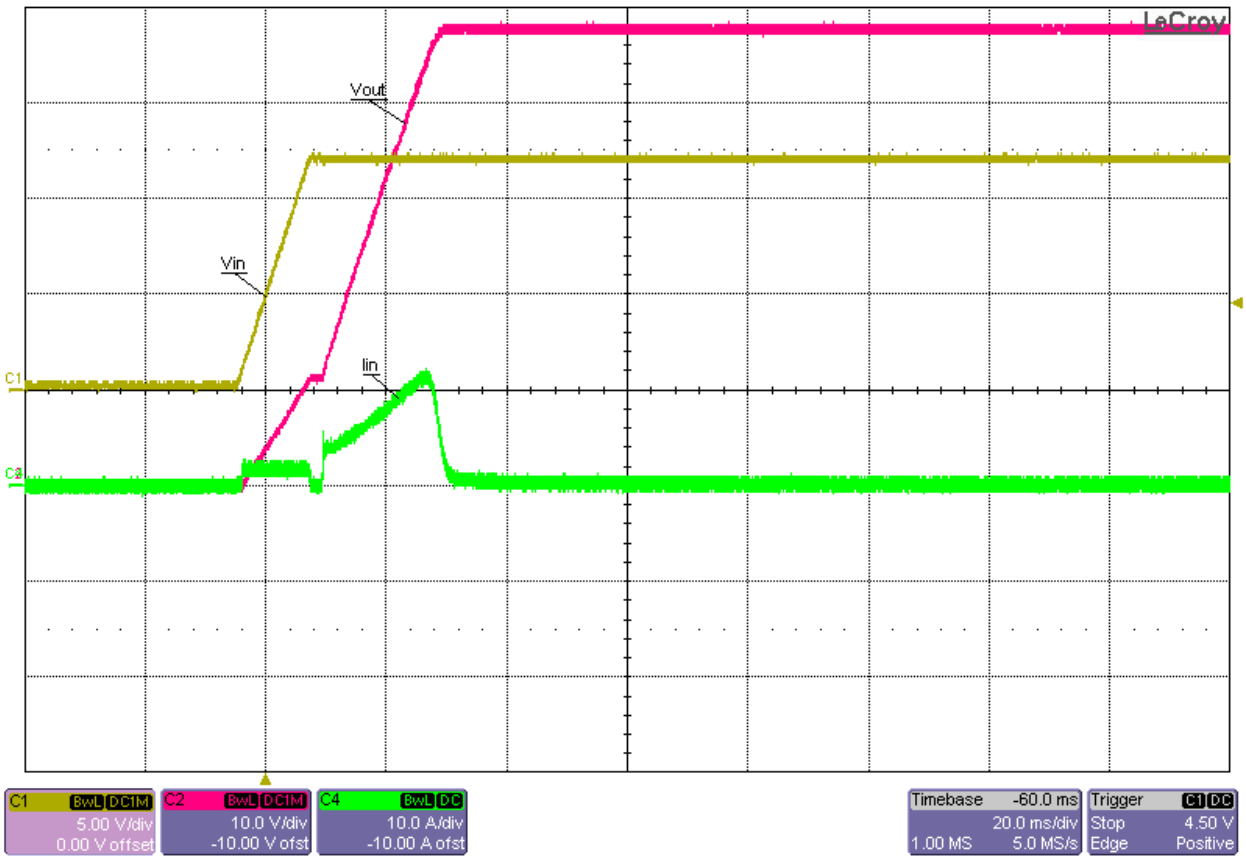
6.2 Startup



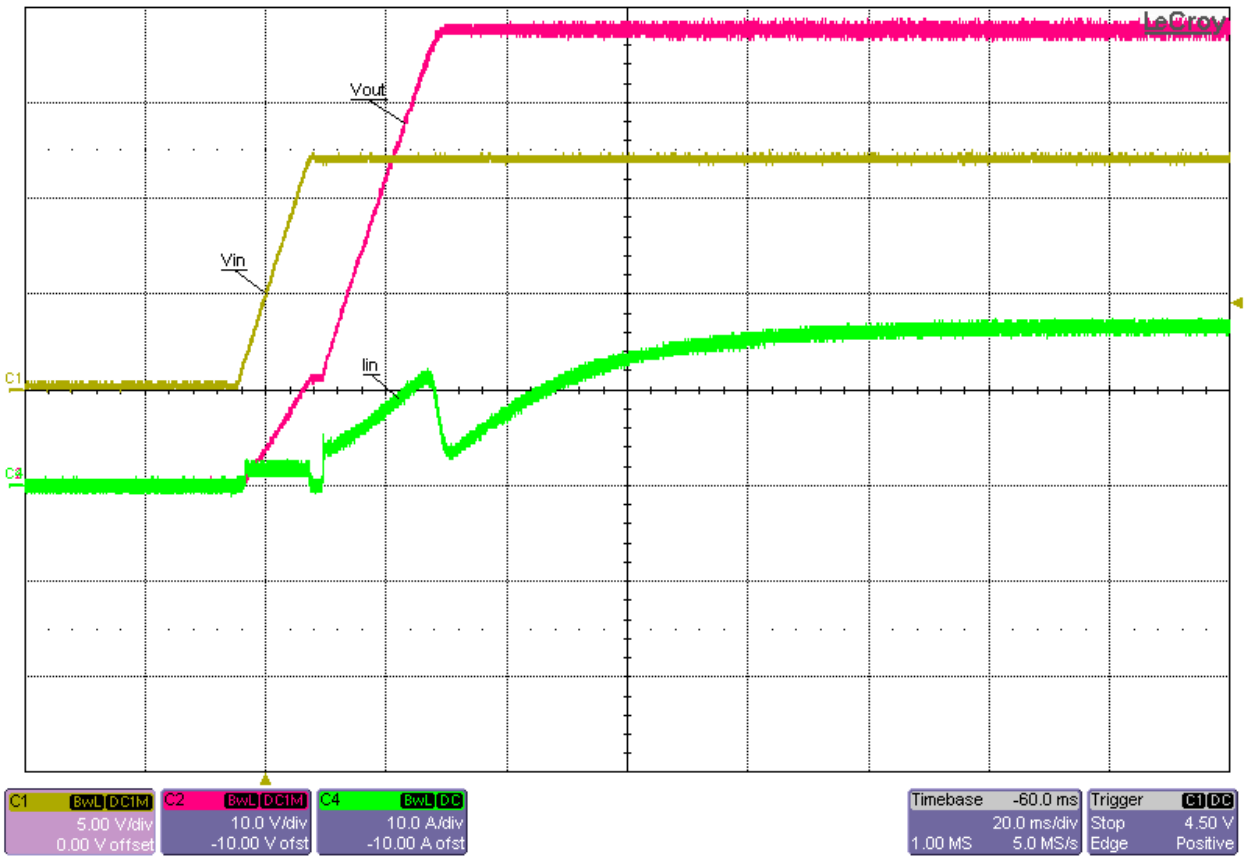
Startup into No Load at 9Vin



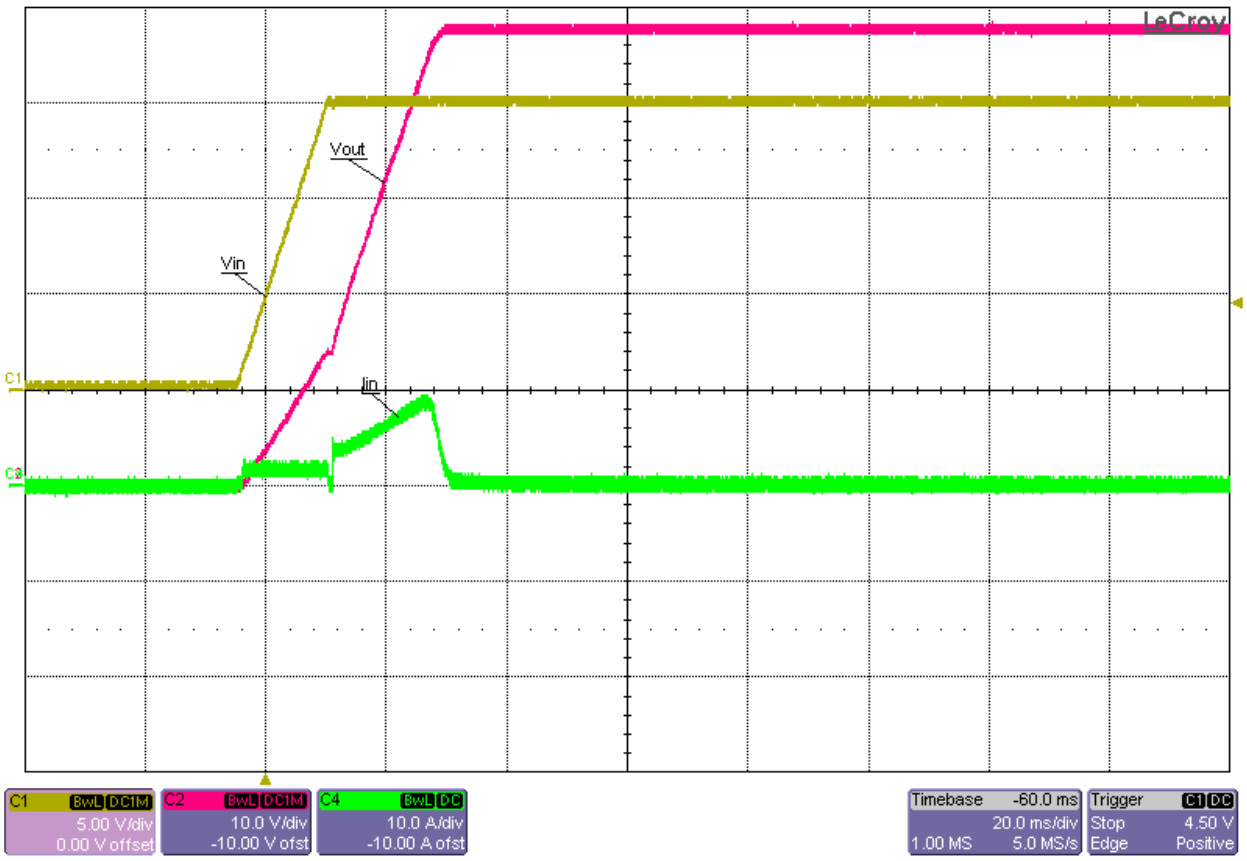
Startup into Full (4A) Load at 9Vin



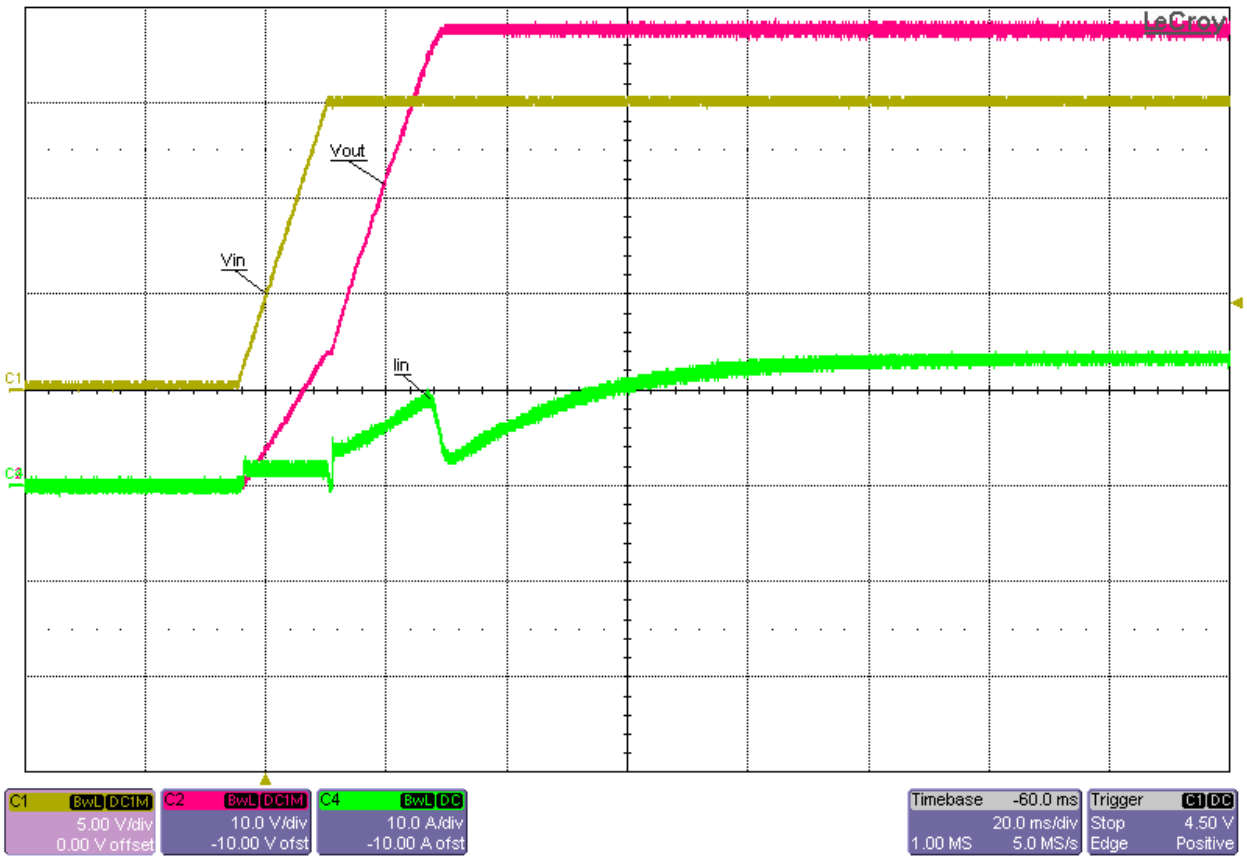
Startup into No Load at 12Vin



Startup into Full (4A) Load at 12Vin

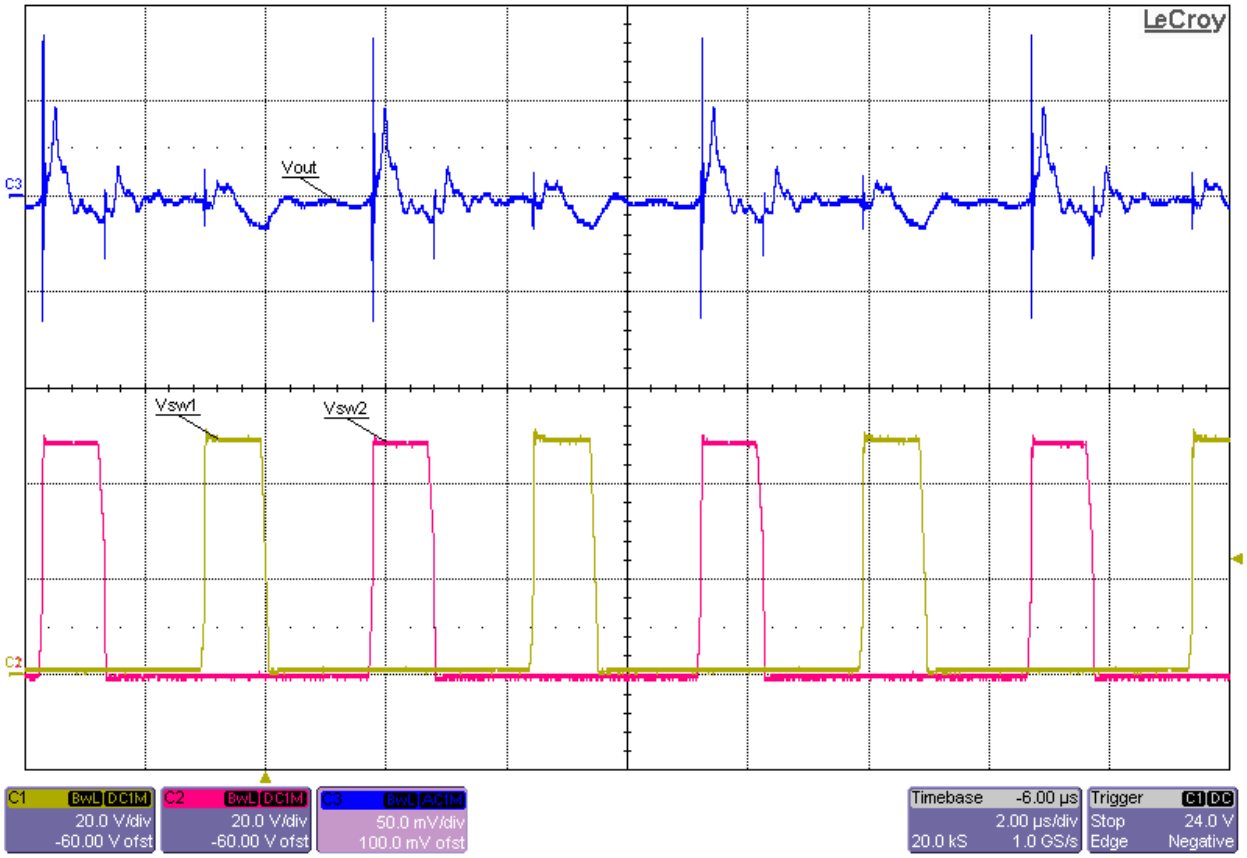


Startup into No Load at 15Vin

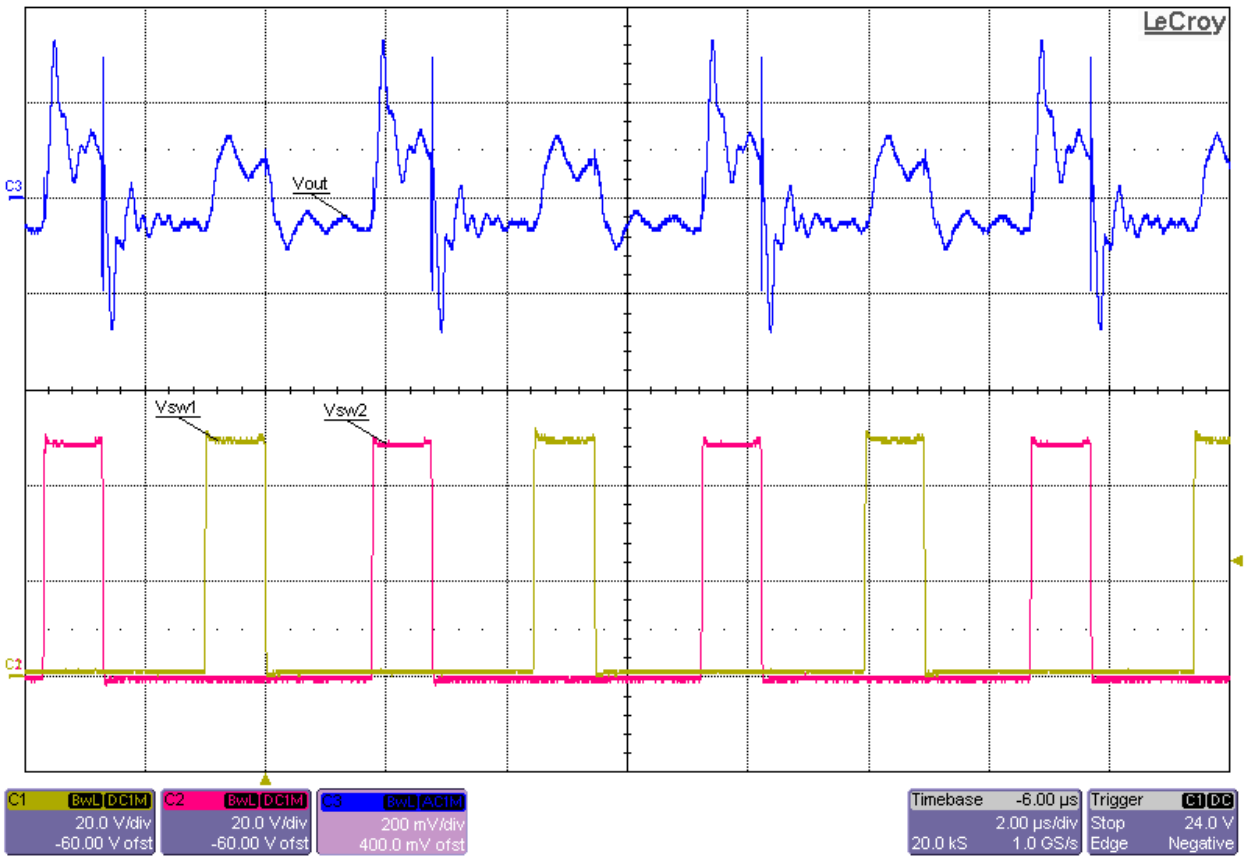


Startup into Full (4A) Load at 15Vin

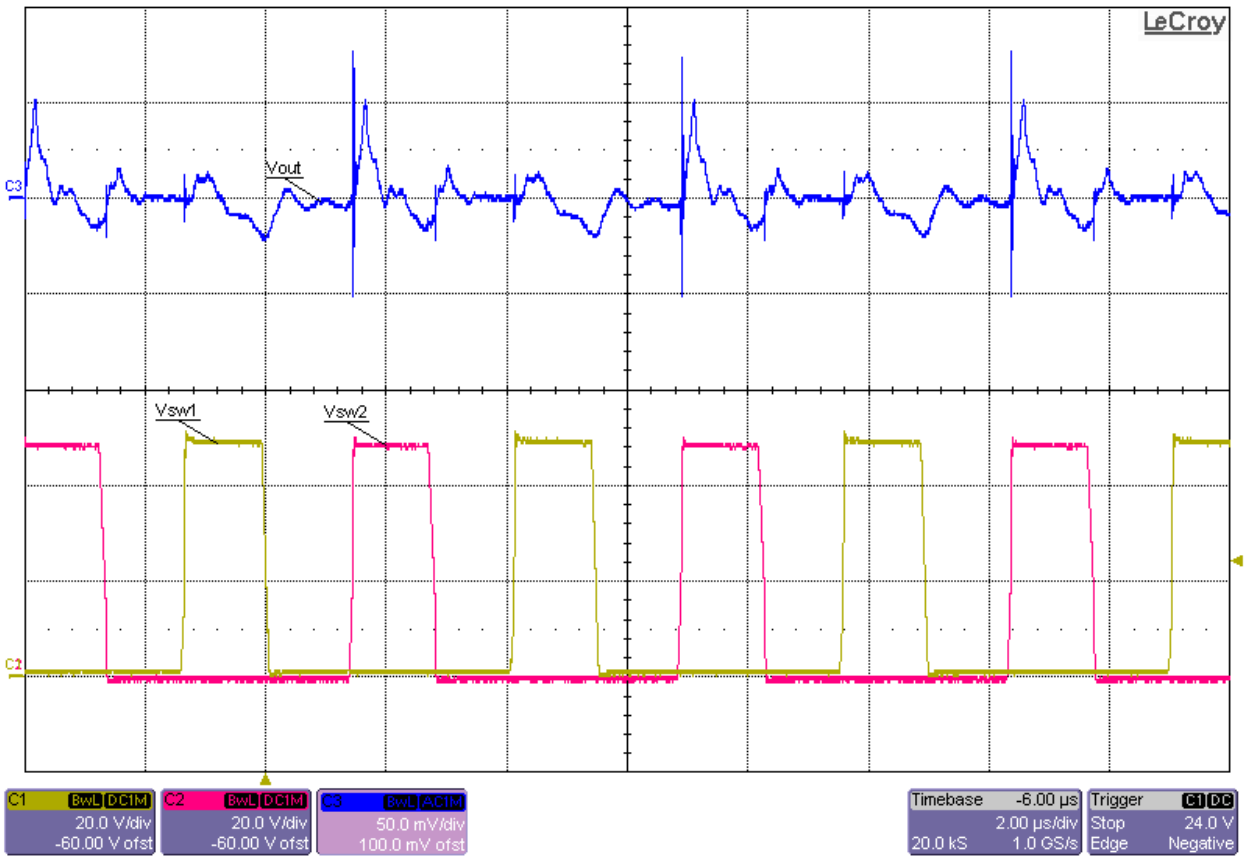
6.3 Output Voltage Ripple and Switch Node Voltage



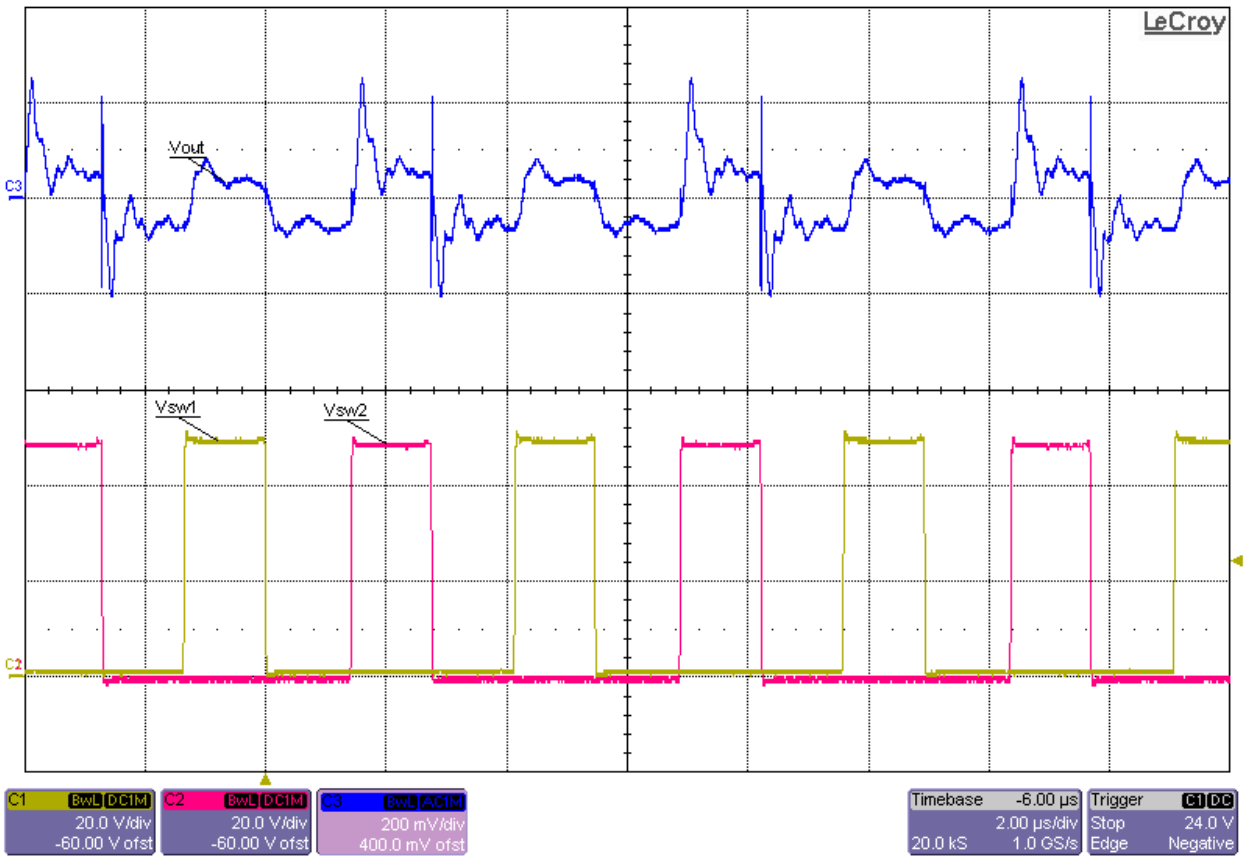
Switch Node Voltage and Output Voltage Ripple at 9Vin and No Load (Vripple ≈ 60mVp-p)



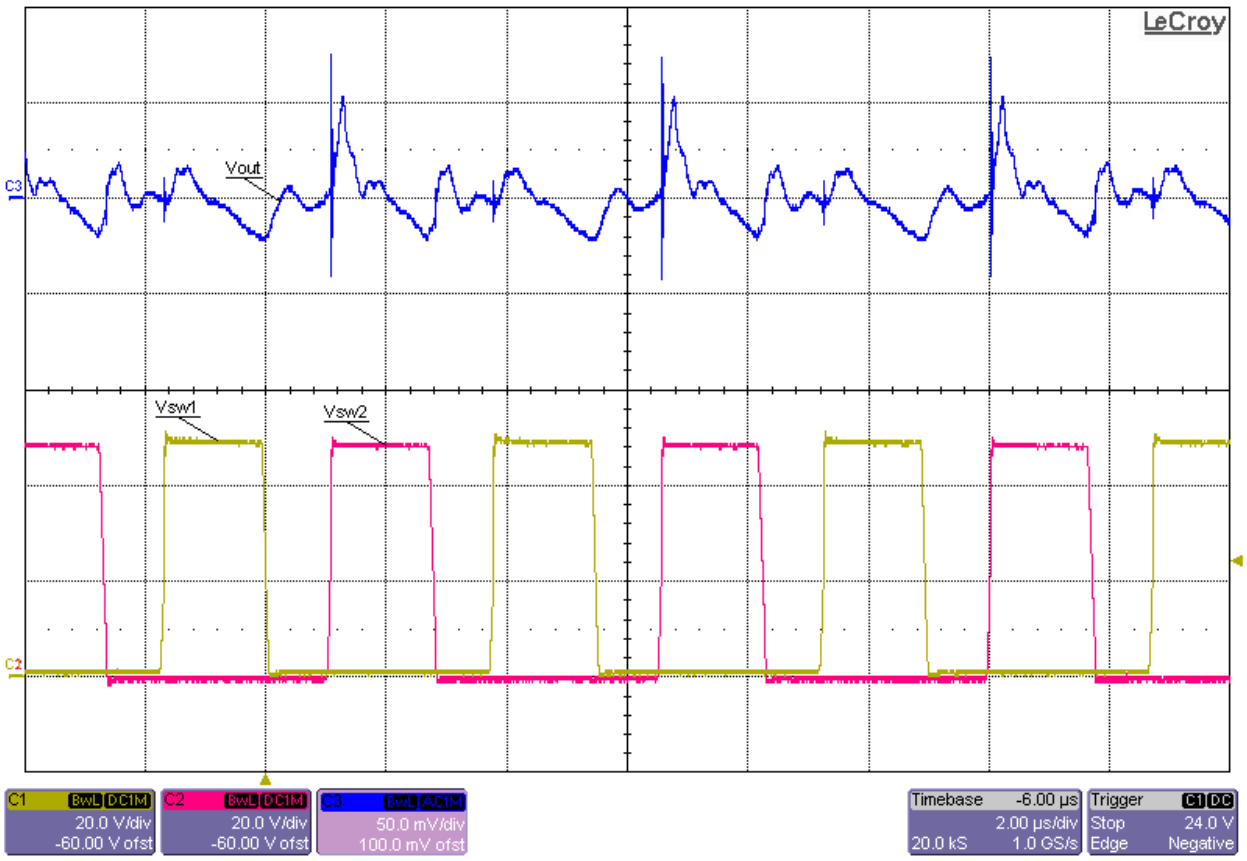
Switch Node Voltage and Output Voltage Ripple at 9Vin and Full (4A) Load (Vripple ≈ 600mVp-p)



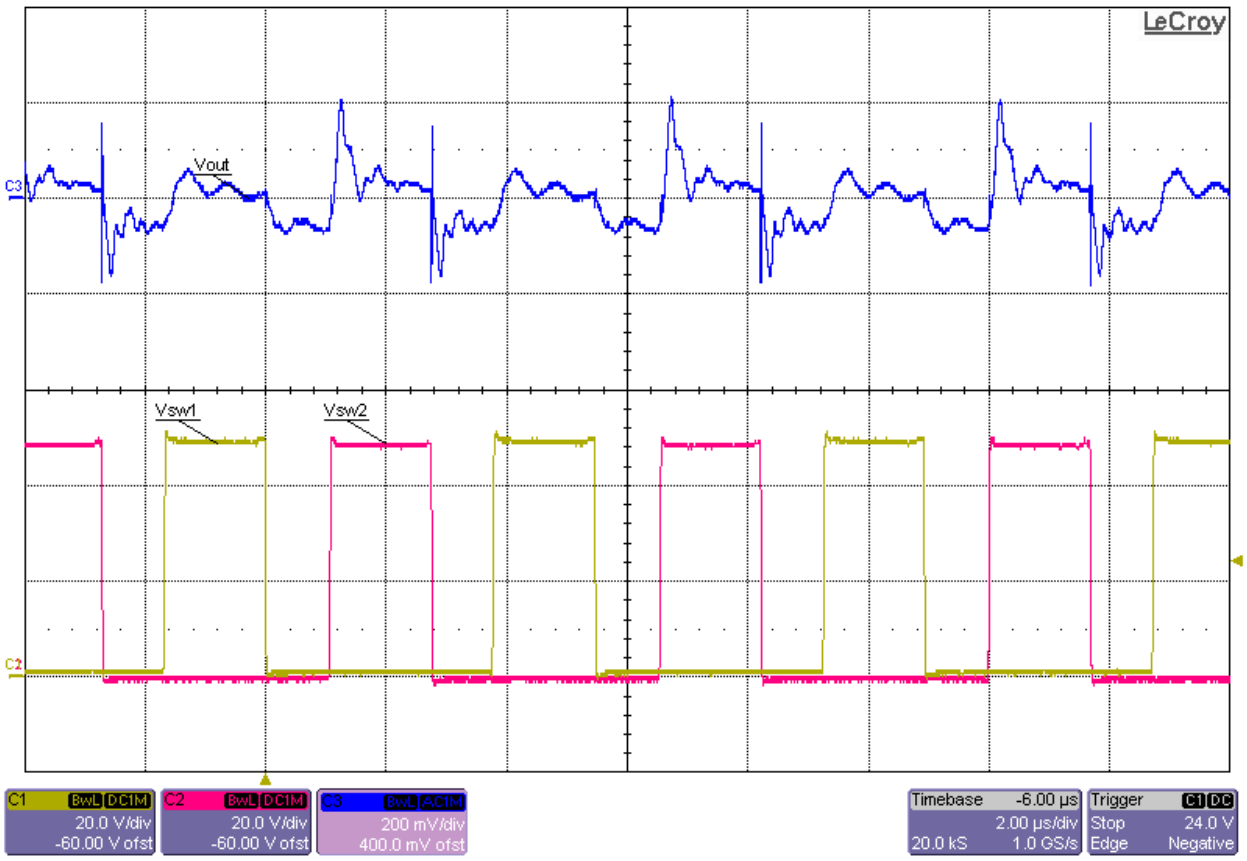
Switch Node Voltage and Output Voltage Ripple at 12Vin and No Load (Vripple ≈ 70mVp-p)



Switch Node Voltage and Output Voltage Ripple at 12Vin and Full (4A) Load (Vripple ≈ 450mVp-p)



Switch Node Voltage and Output Voltage Ripple at 15Vin and No Load (Vripple ≈ 70mVp-p)



Switch Node Voltage and Output Voltage Ripple at 15Vin and Full (4A) Load (Vripple ≈ 380mVp-p)

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265