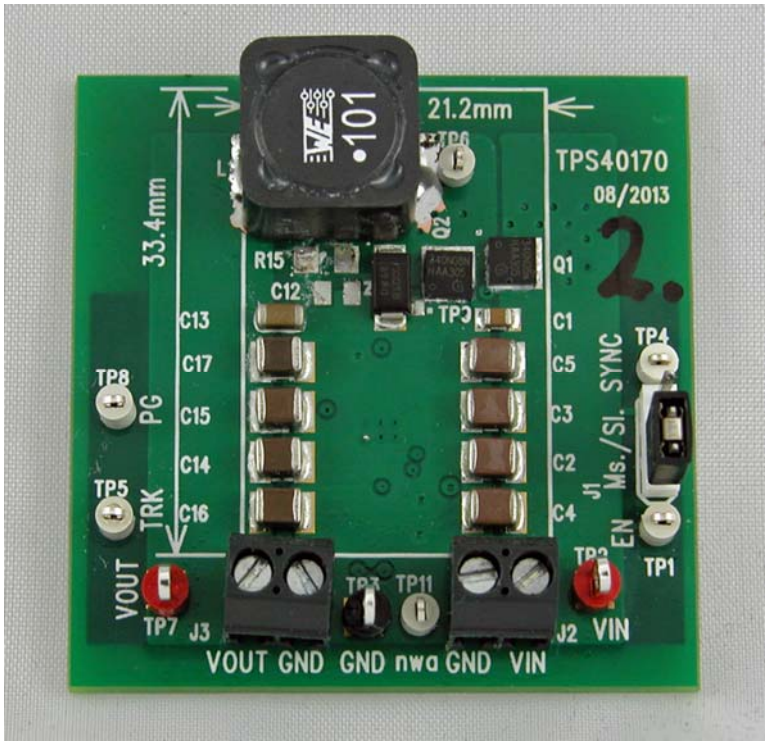
High-Vin Synchronous Buck Converter

- Input 46..50V DC
- Output 31.0V @ 1.3A
- Controller TPS40170
- Free-Running switching frequency of 400 kHz
- Working in continuous conduction mode
- Built on PCB PMP8665 Rev.A



1 Startup & Shutdown

The startup waveform is shown in Figure 1. The input voltage is set at 48.0V, with no load on the 31.0V output.

Channel C1: **48.0V Input voltage**
10V/div, 10ms/div

Channel C2: **31.0V Output voltage**
10V/div, 10ms/div

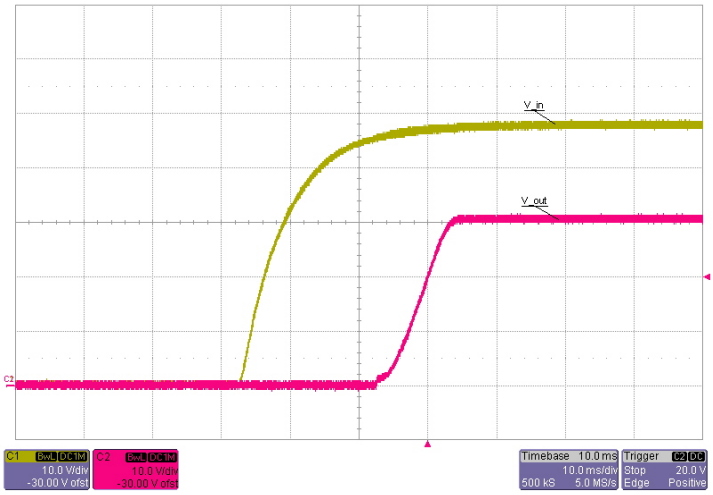


Figure 1

The shutdown waveform is shown in Figure 2. The input voltage is set at 48.0V with a 1.3A load on the 48.0V output.

Channel C1: **48.0V Input voltage**
10V/div, 5ms/div

Channel C2: **31.0V Output voltage**
10V/div, 5ms/div

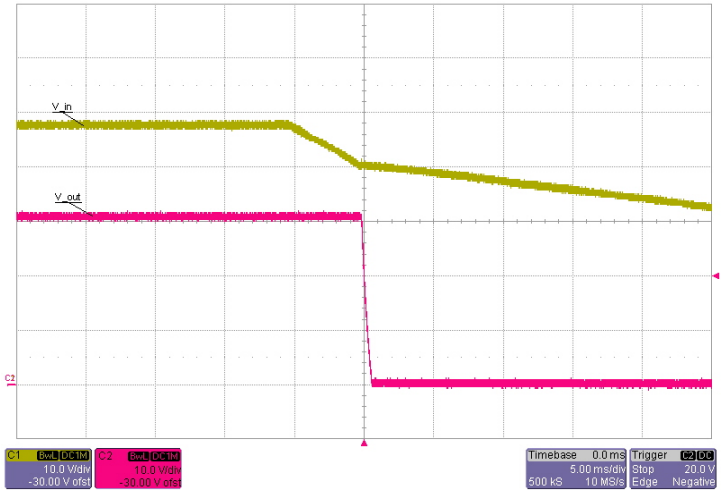


Figure 2

2 Efficiency

The efficiency and load regulation are shown in Figure 3 and Figure 4.

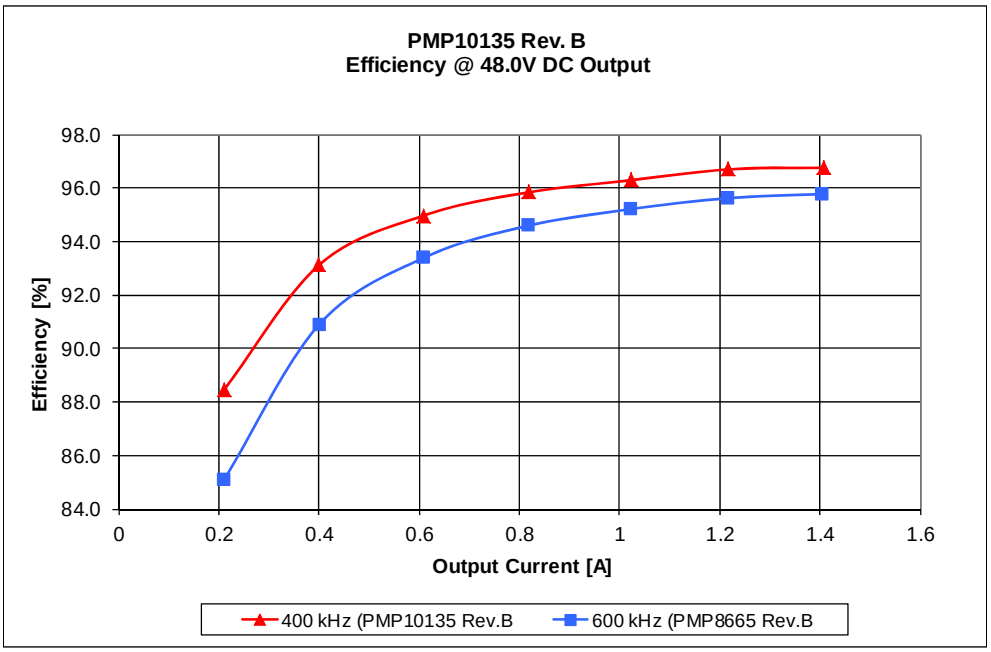


Figure 3

PMP8665RevB is modified to Vout 31V / Fsw 600kHz, PMP10135RevB chops at 400kHz

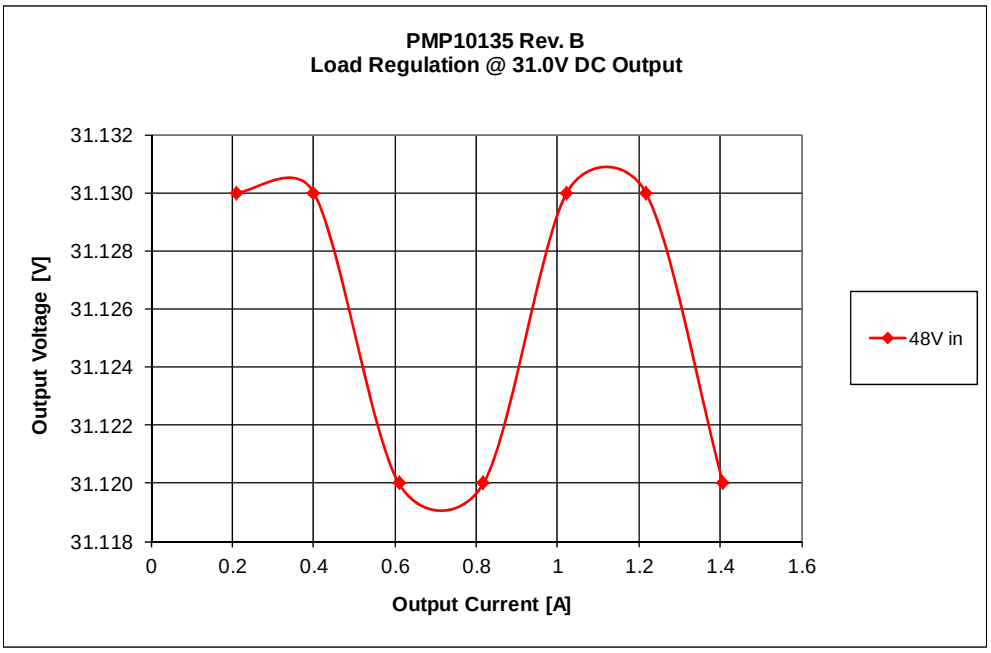


Figure 4

3 Load step

The response to a load step and a load dump for the 31.0V output at an input voltage of 48.0V is shown in Figure 5.

Channel C2: **Output voltage**, -210mV undershoot (0.7%), 206mV overshoot (0.7%)
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.65A to 1.30A and vice versa
500mA/div, 1ms/div

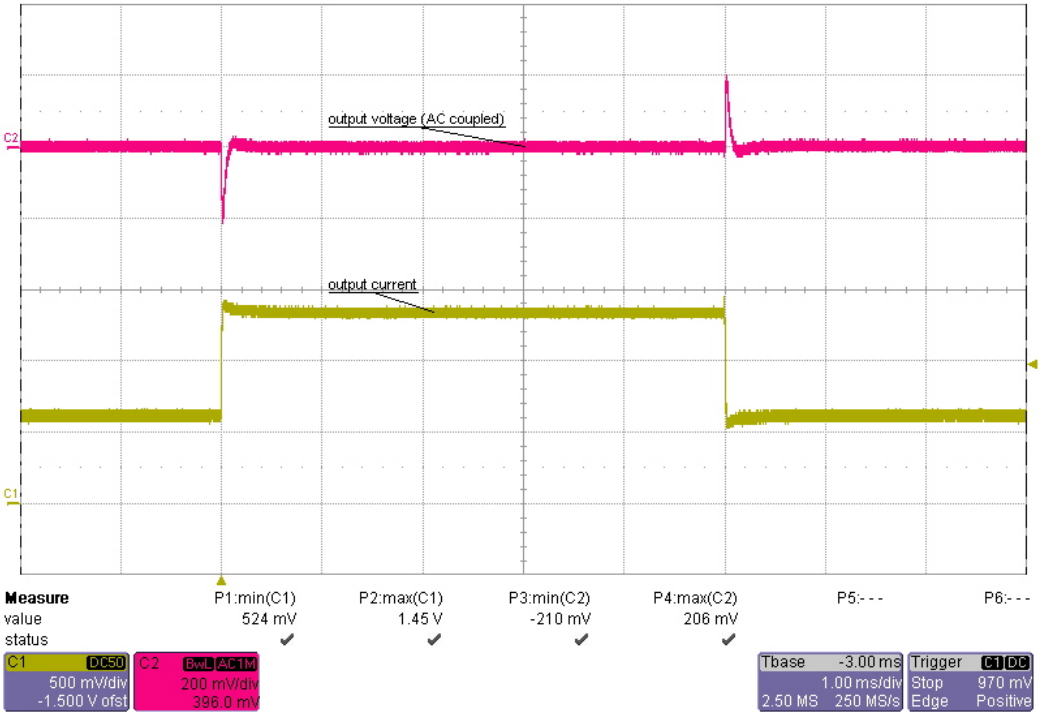


Figure 5

4 Frequency response

Figure 6 shows the loop response at 48.0V input voltage and 1.3A load.

48.0V input

- 71 deg phase margin @ crossover frequency 29.6 kHz
- -16 dB gain margin

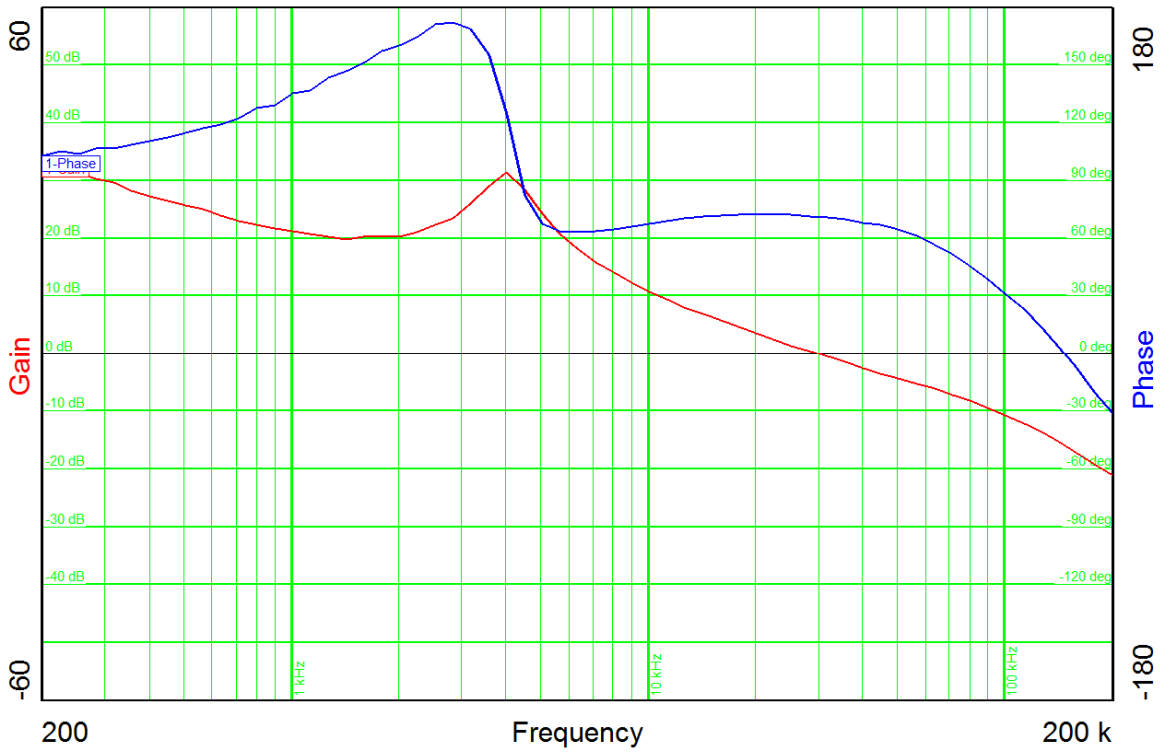


Figure 6

5 High-side FET

The drain-source voltage of the high-side FET is shown in Figure 7. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**, -1.7V minimum voltage, 50.2V maximum voltage
10V/div, 1us/div

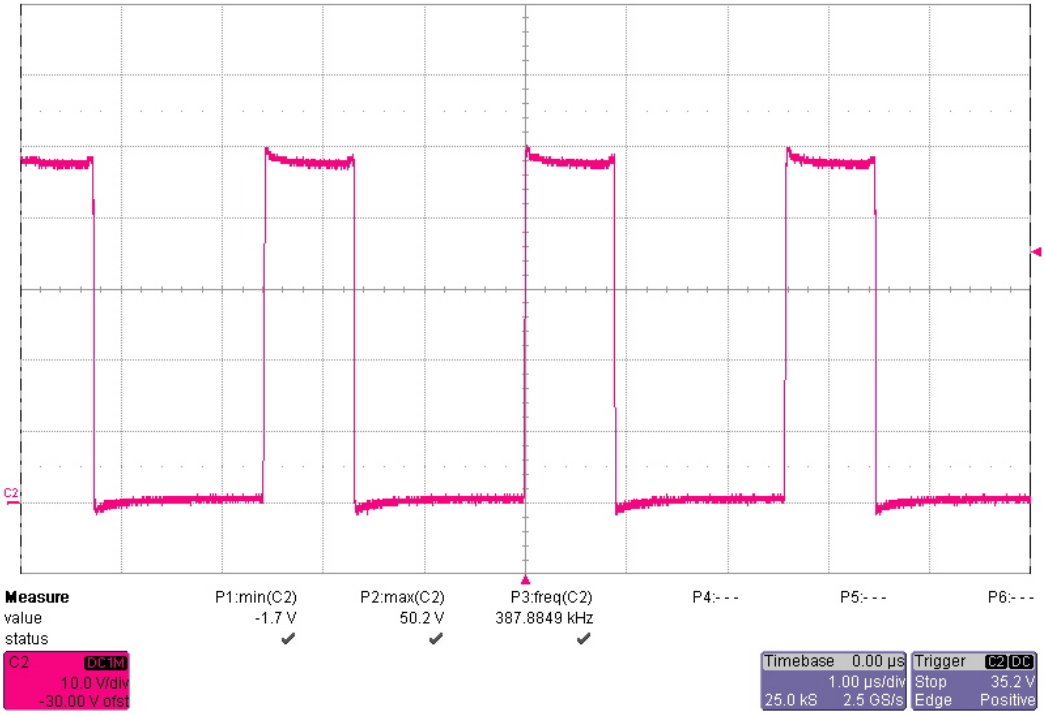


Figure 7

The rising and falling edge are shown in Figure 8 and Figure 9. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**
10V/div, 20ns/div

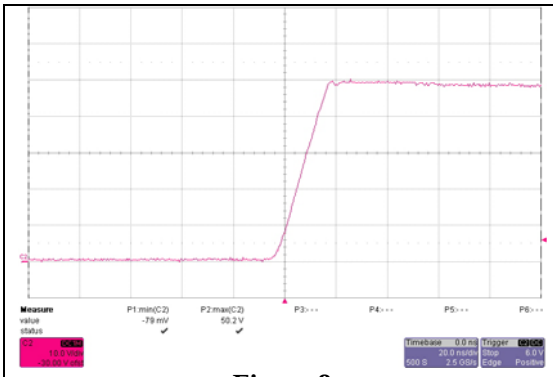


Figure 8

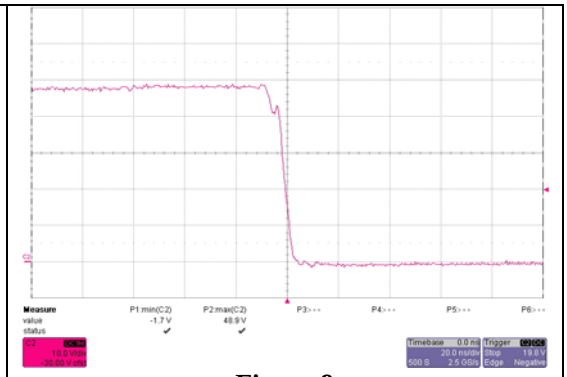


Figure 9

The gate-source voltage of the high-side FET is shown in Figure 10. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Gate-source voltage**, -0.4V minimum voltage, 7.8V maximum voltage
2V/div, 1us/div

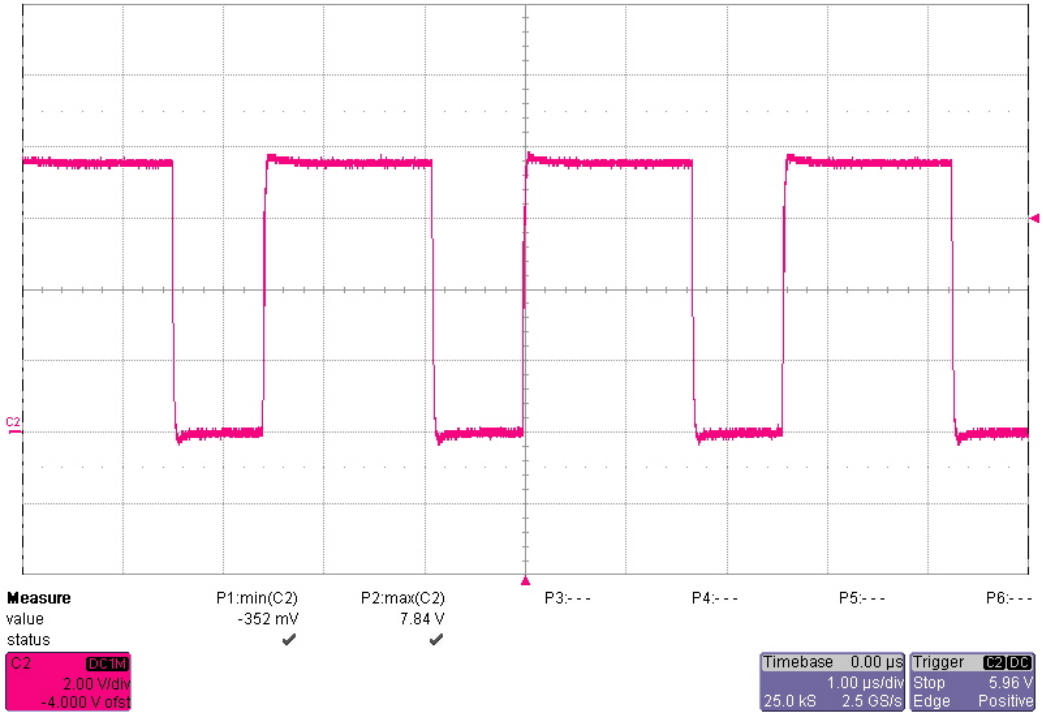


Figure 10

The rising and falling edge are shown in Figure 11 and Figure 12. The image was captured with 48.0V input and 1.3A load. Gate resistor mandatory !

Channel C2: **Gate-source voltage**
2V/div, 20ns/div

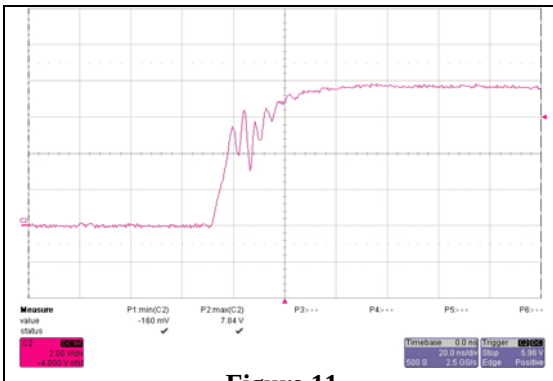


Figure 11

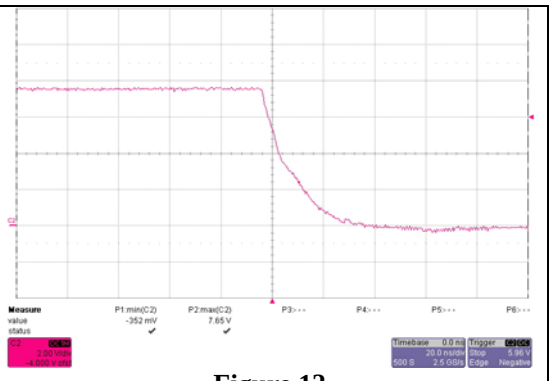


Figure 12

6 Low-side FET

The drain-source voltage of the low-side FET is shown in Figure 13. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**, -2.0V minimum voltage, 52.4V maximum voltage
10V/div, 1us/div

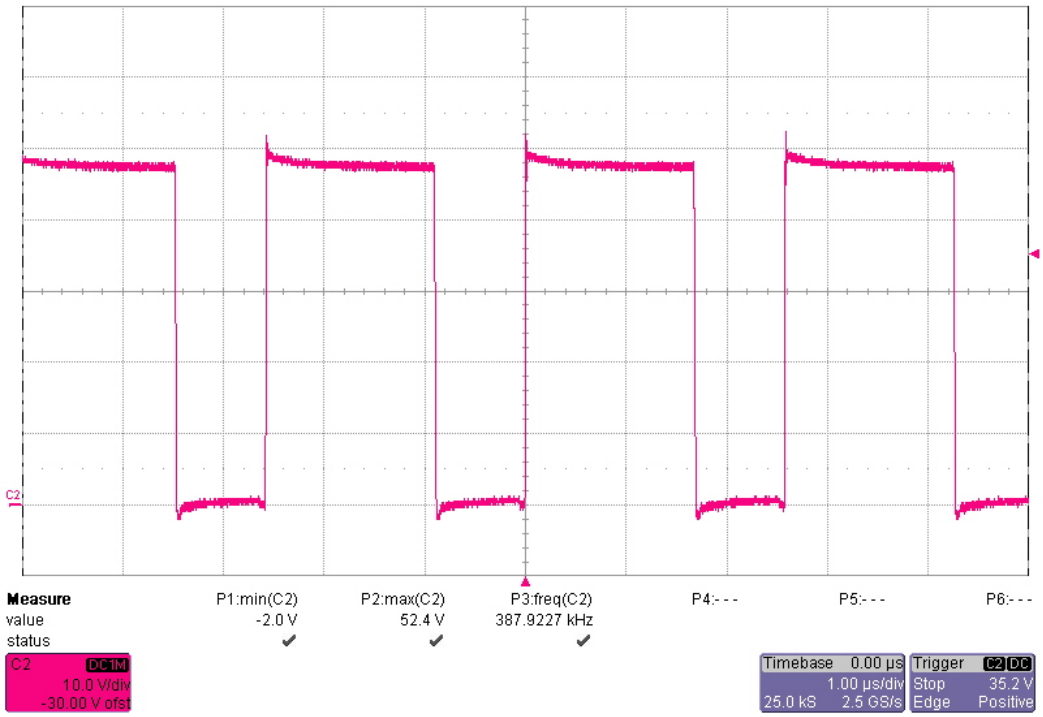


Figure 13

The rising and falling edge are shown in Figure 14 and Figure 15. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Drain-source voltage**
10V/div, 20ns/div

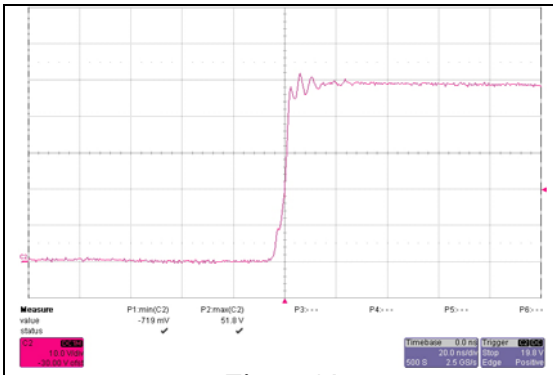


Figure 14

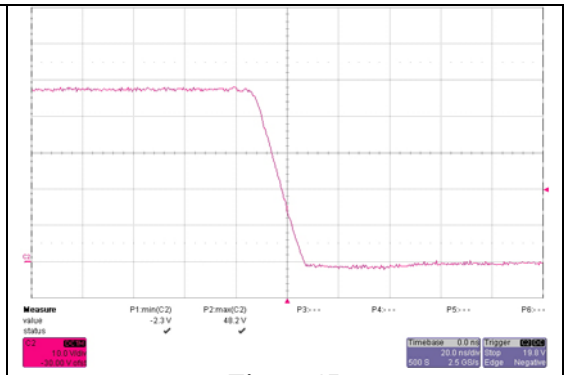


Figure 15

The gate-source voltage of the low-side FET is shown in Figure 16. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Gate-source voltage**, -2.0V minimum voltage, 8.8V maximum voltage
2V/div, 1us/div

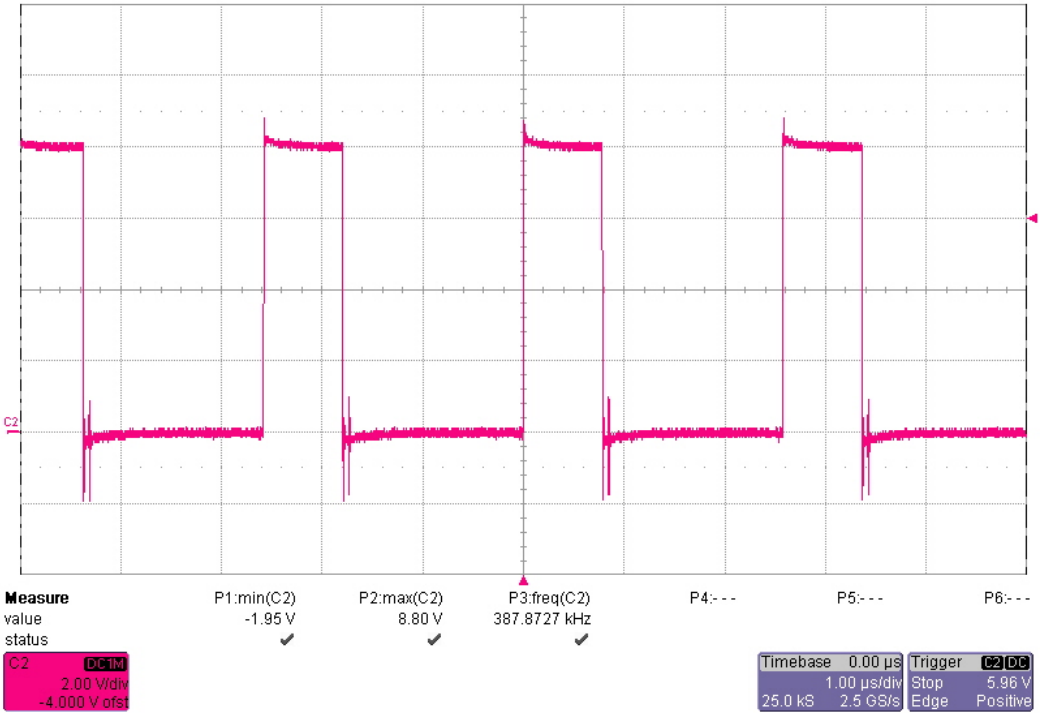


Figure 16

The rising and falling edge are shown in Figure 17 and Figure 12. The image was captured with 48.0V input and 1.3A load.

Channel C2: **Gate-source voltage**
2V/div, 20ns/div

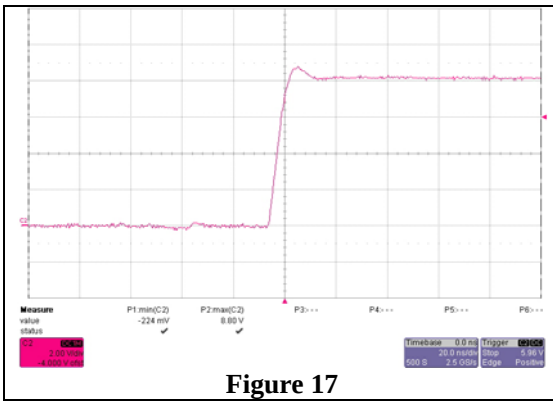


Figure 17

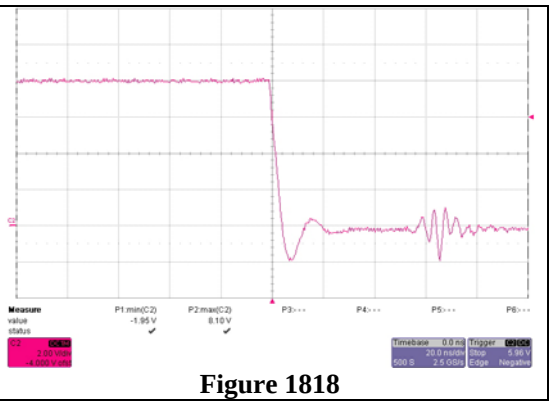


Figure 1818

7 Output and input ripple voltage

The output ripple voltage at 1.3A load and 48.0V input voltage is shown in Figure 19.

Channel M3: **Output voltage @ 48.0 input**, 18mV peak-peak
20mV/div, 2us/div, AC coupled

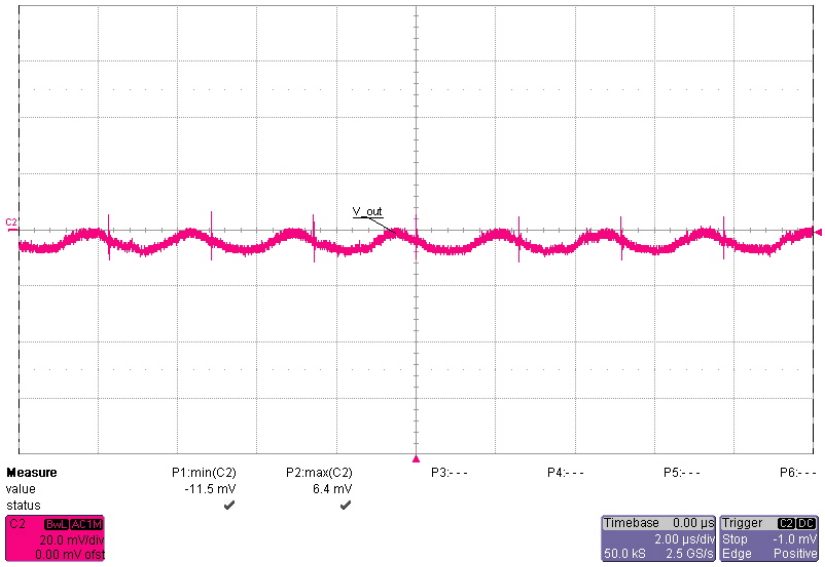


Figure 19

The input ripple voltage at 1.3A load and 48.0V input voltage is shown in Figure 20.

Channel M3: **Output voltage @ 48.0 input**, 227mV peak-peak
50mV/div, 2us/div, AC coupled

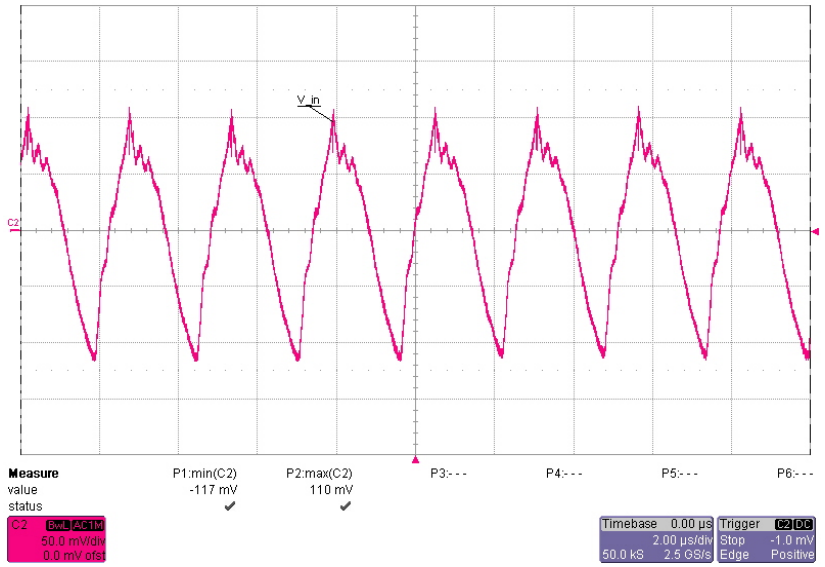


Figure 20

8 Thermal measurement

The thermal image (Figure 21) shows the circuit at an ambient temperature of 21 °C with an input voltage of 48.0V and a load of 1.3A.

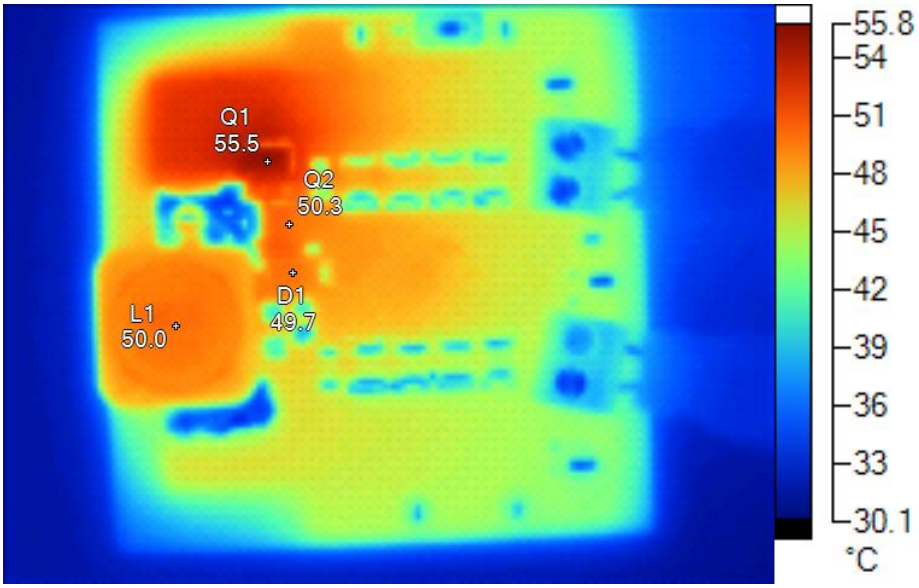


Figure 21

Markers

Label	Temperature	Emissivity	Background
L1	50.0 °C	0.95	21.0 °C
Q1	55.5 °C	0.95	21.0 °C
Q2	50.4 °C	0.95	21.0 °C
D1	49.7 °C	0.95	21.0 °C

Due to Vin 48V max. stress are the switching losses at HS FET; at Fsw 400kHz temperature rise dT is around 33K. PMP8665B set to Fsw 600kHz to use smaller inductor 47uH.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265