

Description & Features

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Xilinx® Zynq® 7000 series (XC7Z045) FPGA. This design uses several LMZ3 series modules, LDOs, and a DDR termination regulator to provide all the necessary rails to power the FPGA. It also features one LM3880 for power up and power down sequencing. This design uses a 12V input.

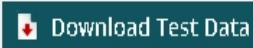
- Provides all the power supply rails needed for a Xilinx® Zynq® 7000 series (XC7Z045)
- Design optimized to support a 12V input
- On board power up and power down sequencing
- Supports DDR3 memory device
- Module design for ease of use

 The Standard Terms and Conditions for Evaluation Modules apply.

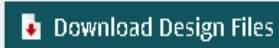
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	PMP10613.2
V _{in} (Min) [V]	10.8
V _{in} (Max) [V]	13.2
V _{out} (Nom) [V]	1.8
I _{out} (Max) [A]	3
Output Power	5.4
Isolated/Non-Isolated	Non-Isolated
Input Type	DC
Topology	Buck- Integrated Switch

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Part #	Package Pins	CAD File (.bxl)	STEP Model (.stp)
LM3880	SOT (DBV) 6	Download	Download
LMZ31503	B1QFN (RUQ) 47	Download	-
LMZ31520	B4QFN (RLG) 72	Download	-
LP2998	SOIC (D) 8	Download	Download
	HSOP (DDA) 8	Download	Download
LP3892	TO-263 (KTT) 5	Download	Download
	HSOP (DDA) 8	Download	Download
LP3981	WSON (NGC) 6	Download	Download
	VSSOP (DGK) 8	Download	Download
TPS560200	SOT (DBV) 5	Download	Download
TPS7A3501	WSON (DRV) 6	Download	-

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Title	Abstract	Type	Size (KB)	Date	Views	T1 Recommends
 PMP10613 Test Results		PDF	914	28 Apr 2015	35	☒
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Title	Abstract	Type	Size (KB)	Date	Views
PMP10613 Gerber		ZIP	2781	28 Apr 2015	19
PMP10613 Altium		ZIP	10039	28 Apr 2015	37
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