

TI Designs PLC Lite Communication Module for Smart Homes Design Guide



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[TIDM-PLCLITE-PLUGMODULE](#)

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Design Files

[TMS320F28035](#)

Product Folder

[AFE031](#)

Product Folder



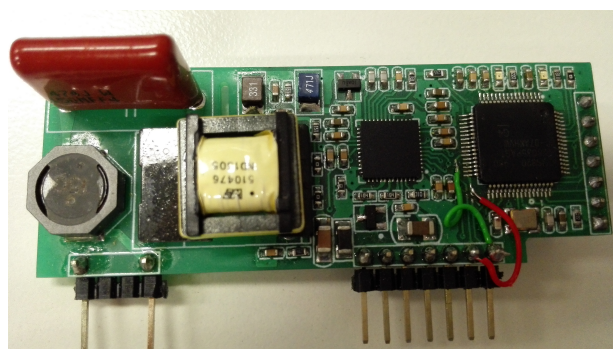
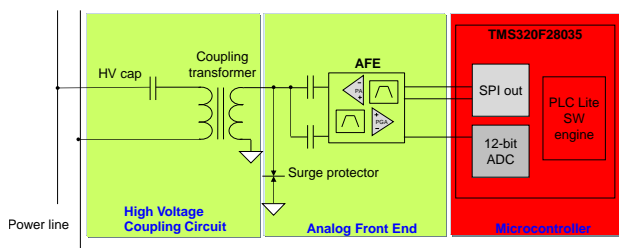
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Design Features

- Low-Cost, NB-OFDM-Based Power Line Communication (PLC) Solution
- From 200- to 300-m Smart Home and Smart Building Cross-Walls Communication Without Adding Wires
- Flexible Configuration for Robustness and Data Rate up to 21 kbps
- Carrier-Sensing Multiple-Access With Collision Detect (CSMA/CA) Integration for Peer-to-Peer (P2P) and Broadcast Network Without User Concern
- Universal TI All PLC Solution Protocol
- Minimum PCB Size

Featured Applications

- E-Meter With Integrated PLC for Monitoring
- E-Meters With Host Application, Metrology, and PLC on a Single Chip Requiring 32-Bit Processing Power
- Grid Infrastructure Meters



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1 System Description

To fit the smart home definition requires that most home electronic devices have the ability to communicate and receive commands from a user or to transmit control functional information. Using internet of things (IoT)-related communication methods, home electronics typically use wireless applications such as Wi-Fi, Bluetooth, or ZigBee to deploy smart control. In other larger systems, such as the central heating, ventilating, and air conditioning (HVAC) system of a skyscraper, the remote controller may use a wired solution such as an RS-485, M-Bus, homebus, or even a current ring. However, all of the previously mentioned wireless methods experience difficulty dealing with the attenuation caused by wall structures; and all of the wired solutions may involve extensive cable use with the increase in number of connected devices. Using a PLC system (particularly the narrow band PLC, which is below the FCC band < 500 KHz) to avoid this attenuation can be a useful solution to achieve the required control signal data rate for home appliances and a robust connection to every plug in the house, without adding any extra channel cable.

This PLC Lite™ communication module is designed to be a plug-in module for any home-appliance power input part that can use the low-voltage (LV) power grid to communicate with other home appliances or the house network switch by power line. The PLC Lite is a TI-property, low-cost PLC technology that combines the PRIME and G3-PLC standard physical interface device (PHY) layers. The PRIME and G3-PLC PHY layers are generally used in automatic meter reading (AMR), combined with CSMA/CA functional MAC layers, and then reduced in the millions of instructions per second (MIPS) of the software to input the communication functions in a Piccolo-B™ TMS320F28035 microcontroller (MCU). Using an AFE031 analog front-end, the module can directly send and receive PLC signals on a 220-V, 50-Hz power line or a 110-V, 60-Hz power line, while transmitting and receiving messages to the host processor with an easy to configure universal asynchronous receiver and transmitter (UART) interface.

2 Design Features

2.1 Low-Cost Narrowband-OFDM

Compared with the generally used PRIME or G3-PLC solutions (which mainly focus on the AMR application of the smart grid), PLC Lite is a low-cost orthogonal frequency division multiplexing (OFDM) solution that does not require many MIPS of MCU that can be integrated on F28035 rather than an F28069 or PLC83 MCU. At the same time, the PLC Lite is still an OFDM-based PLC technology that can deliver more data through speed when compared with traditional binary phase shift key and spread frequency shift key (BPSK/S-FSK) solutions, such as IEC 61334. The PLC Lite is also more robust when avoiding narrow band interference, which can exist on varying frequencies in the channel.

2.2 200- to 300-m LV Line Transmission Distance

Upon smart home or smart building deployment, wireless products can experience difficulty connecting from top floors to basements due to walls and other structures that do not allow line-of-sight propagation (LoS) between certain corner points. However, using the power cable as the communication channel, the PLC signal can reach every socket of each home appliance. The TI PLC solution has a strong algorithm to deal with interferences and attenuations; the LV transformer used most often causes approximately 30-dB of attenuation. Field test results that have been run in different countries show that this TI PLC solution can deliver a 200- to 300-m transmission distance on a 220-V/50-Hz or 110-V/60-Hz citizen grid environment.

2.3 Flexible Configuration

The PLC Lite software can be configured in four different modulation modes. The maximum data rate uses BPSK on 48 subcarriers for each OFDM symbol, which has a 21-Kbps rate. For common use, the source stream must have a depth equal to five convolutional codes for forward error correction (FEC), which causes a $K = \frac{1}{2}$ rate reduction and results in a useable data rate of approximately 11 Kbps. If the user desires a more robust transmission stability, the software can be configured to ROBO-4 or ROBO-8 modulation, which indicates the use of four or eight subcarriers to repeat the code of one bit, which can increase the signal-to-noise ratio (SNR) but reduce the data rate to 2.6 or 1.3 Kbps.

2.4 CSMA/CA

The PLC Lite software has an inner MAC layer for network topology design that includes a CSMA/CA algorithm. This algorithm can help to construct the broadcast system so that the user does not have to worry about multi-node transmitting jams.

2.5 Universal HCT Protocol

All of TI's PLC software is designed to use a single UART to communicate with a host processor, including PRIME, G3, IEEE P1901.2, and PLC Lite. The UART uses a universal command protocol called host control transport (HCT). The HCT protocol delivers the most basic frame format for command messages and operation commands to host, including send and receive content, PHY and MAC configurations, system configurations, attach and detach to network, and so forth. The HCT protocol is easy to use and helps users to save on the cost of development.

2.6 Minimum PCB Size

This design module is initially used for an HVAC system. Certain parts that are not commonly used in the circuit were left out to save space and size, and the layout of key components has been optimized, resulting in the minimum PCB size of a two-layer solution for a ready-to-use PLC module.

3 Block Diagram

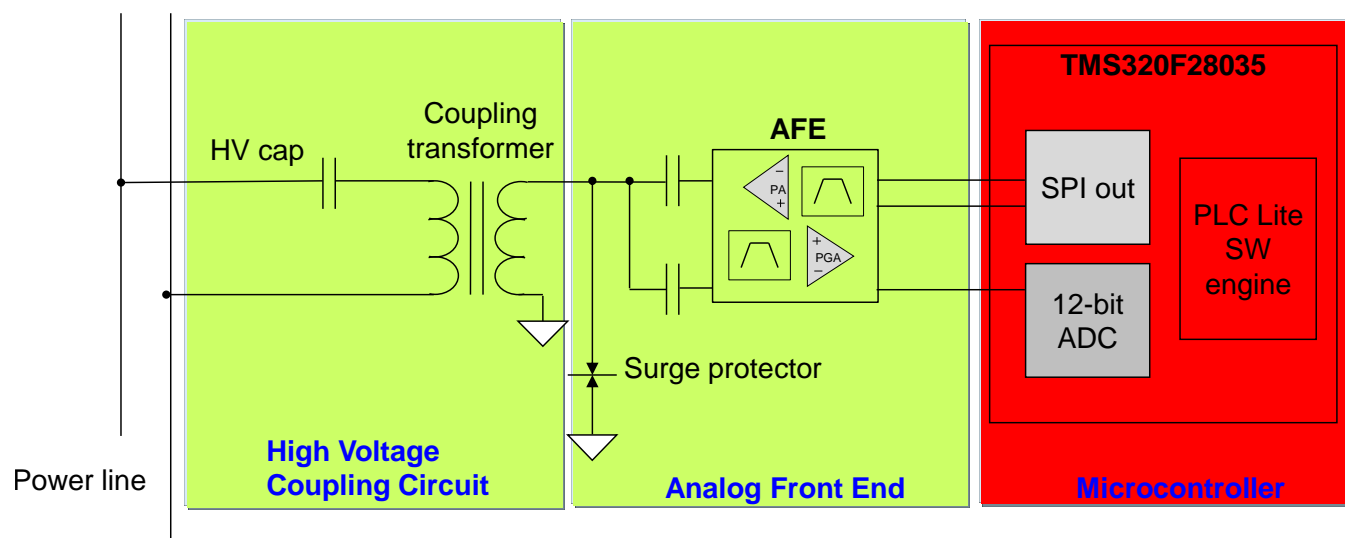


Figure 1. System Block Diagram

4 Circuit PCB Photo

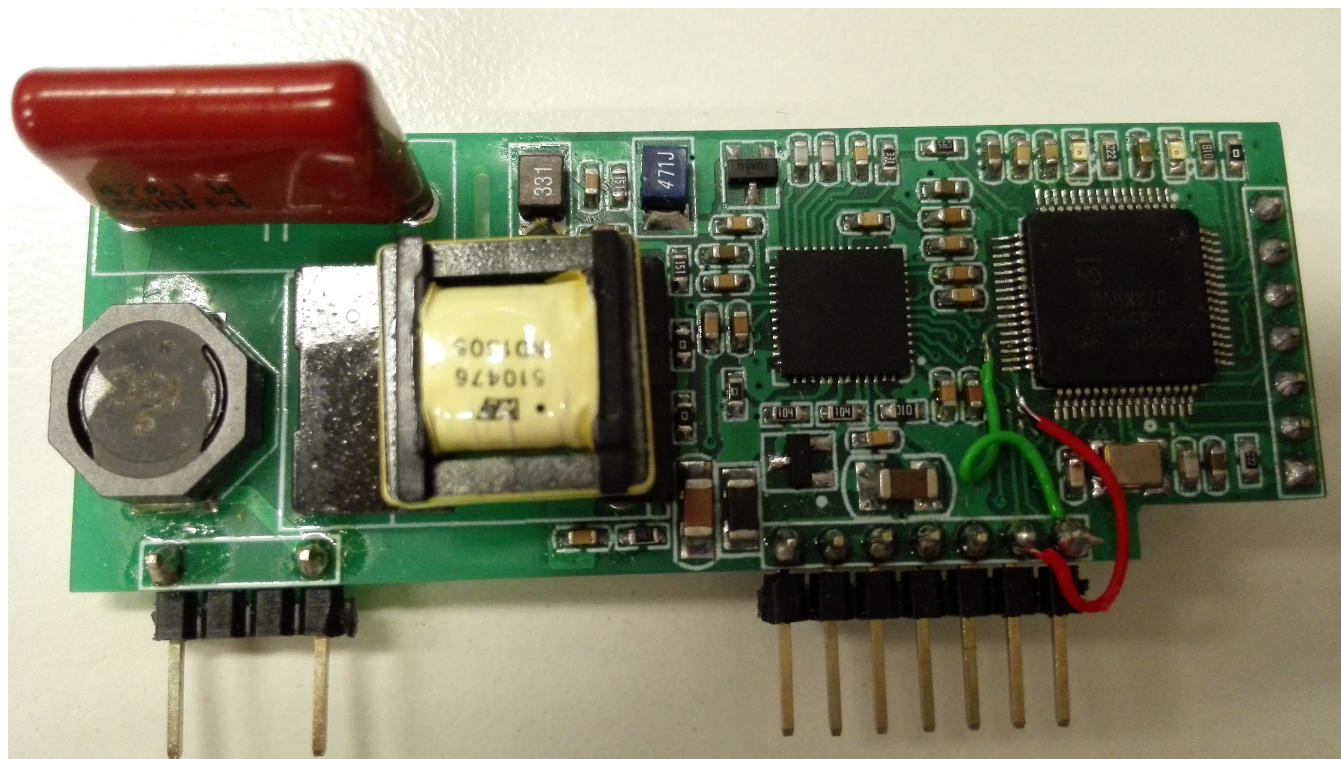


Figure 2. Main Board

The board generally includes three parts. The left side of the board includes one polyphenylene sulfide (PPS) film capacitor, one inductor, and one transformer as the power line coupling component, which passes the 62- to 89-KHz band signal and prevents 50- to 60-Hz of AC power to the low voltage area. The two lower-left corner pins connect to power lines L and N. The AFE031 device, related TX and RX filters, and amplifier passive parts are located in the central area. The right side of the board contains the TMS320F28035 MCU with related clock and decoupling caps and includes the Joint Test Action Group (JTAG) interface. The seven lower-right corner pins are the power and communication pins of the module, which are (from left to right) defined as: 3.3 V, GND, GND, 12 V, Empty, PLC UART TX, and PLC UART RX.

5 Hardware Design Description

The hardware circuit of the PLC Lite communication module includes six parts.

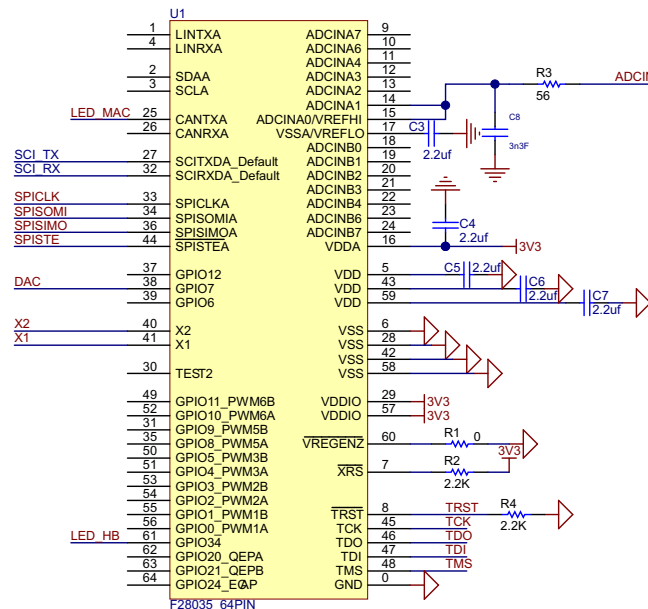


Figure 3. MCU

Figure 3 shows the TMS320F28035 MCU, which uses three main peripherals: ADC channel 1, SPIA, and SCIA as UART. The ADCINA0 input side uses an RC filter part, where the resistor and capacitor must be placed as close as possible to the MCU. The ADC trace is the only trace to pass the analog signal on the board, so the trace length must be as short as possible. The GPIO34 as pin 61 is reserved to indicate the light-emitting diode (LED) signal of the PLC Lite software heartbeat. The TI™ publication PLC Lite software also uses GPIO31 to indicate MAC layer activity with an LED. However, the MAC indication LED is controlled by the GPIO0 in the module and requires software configuration for use.

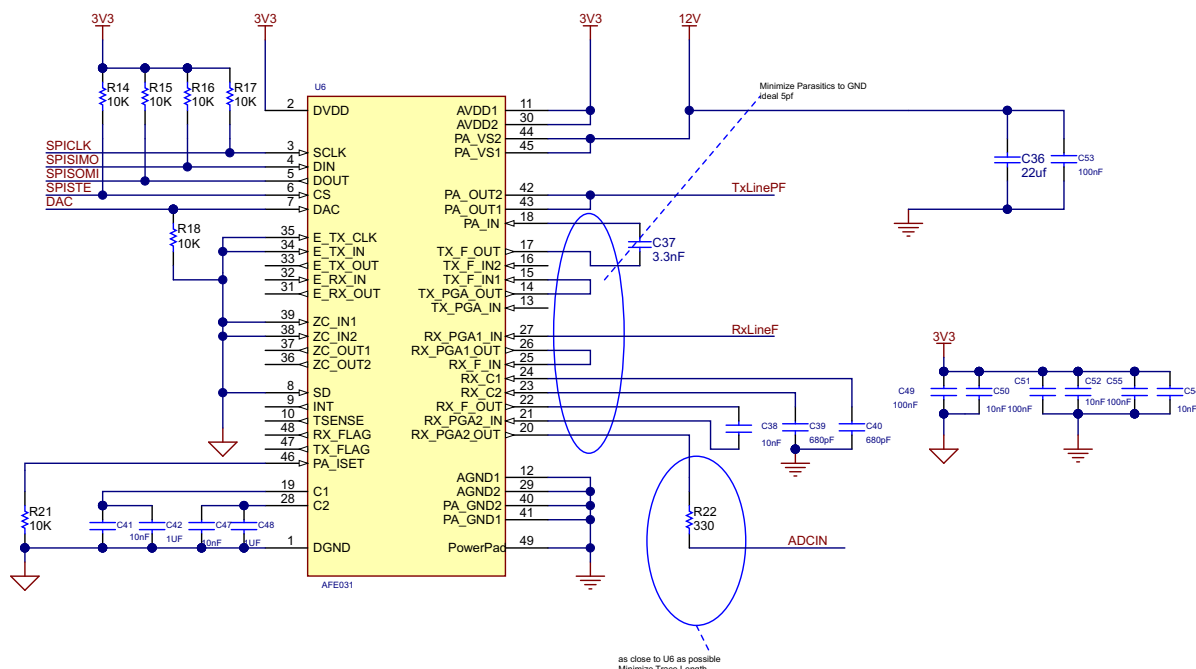


Figure 4. Analog Front End (AFE)

Figure 4 shows the AFE031 circuit. The user must ensure a minimum space between the trace between pins 25 and 26 (RX_PGA1 to filter) and the trace between pins 14 and 15 (TX_PGA to filter) on the AFE031 circuit. This space distribution is due to the inner components of the AFE031: the TX and RX, PGAs and LPFs, and a PA (which all need to manually connect from outer traces). All trace capacitors (C37, C38, C39, and C40) must be placed as close to the AFE device as possible. While the PA is designed to use the 12-V DC as a power supply, the AFE can use a 7- to 24-V DC of any value, provided that the PA voltage is kept stable during usage.

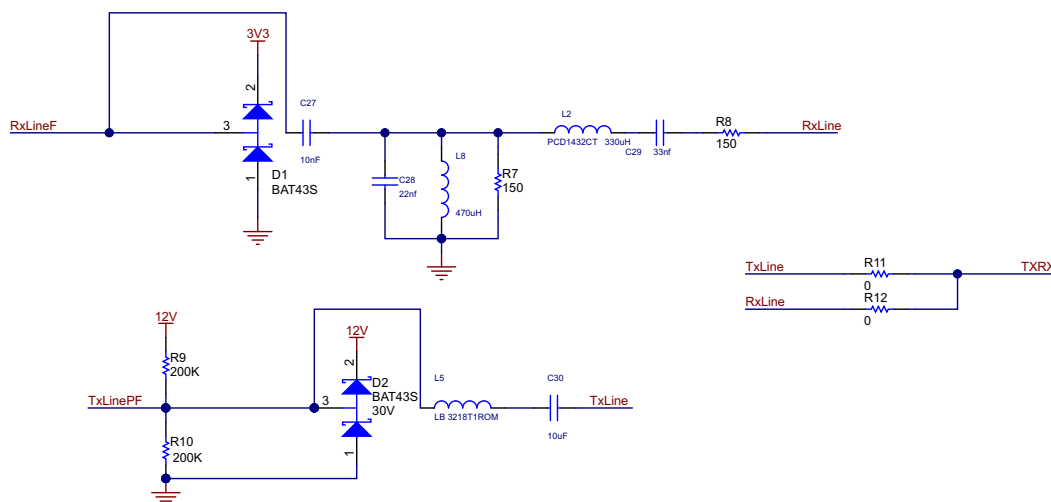


Figure 5. TX and RX Passive Link

Figure 5 shows the TX and RX passive link. The TX and RX passive link components are designed to have rapid learning cycle (RLC) filters, which must all have an approximate 65- to 70-KHz range center frequency. The two Schottky diodes are used to limit the signal range within the power-ground limitation. For the RX link, use the shunt and serial RLC to adjust the Q value and obtain a higher bandwidth.

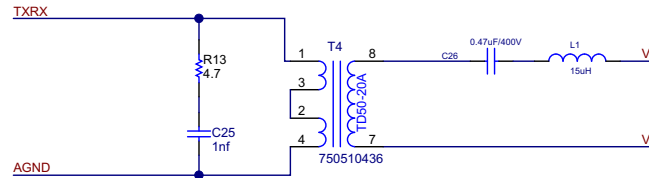


Figure 6. Transformer and Coupling Part

The left side connects to the TX and RX passive link, which connects to the AFE031 device; the right side connects to the power line. Be sure to consider the following key points during hardware design:

1. The ratio of the transformer: Because of the EN50065-1 limitation, the PLC signal transferred to the power line must not be over 120 dB μ V for a 2- Ω load. Results from previous tests show that if the user uses 15 V to power the PA of the AFE, the ratio of the transformer LV:HV (left versus right) must be approximately 1.3:1 (TX link attenuates, RS link amplifies), and the software can select a maximum TX amplitude. If the user uses 12 V to power the PA of the AFE, the transformer ratio can be 1:1, but the software must set the TX PHY parameters to set the maximum amplitude to attenuate 3 dB of power. The transformer affects the coupling emission performance of the EN50065-1 when under a 2-MHz frequency; to compensate, TI recommends using products from Wurth Elektronik.
2. HV side coupling LC: The center frequency of the LC must be approximately 60- to 70-KHz to pass the signal. While using high voltage CBB capacitors, the maximum voltage range must exceed the amplitude of the power grid AC voltage (220-V AC must be over 311 V). So if the PLC module is used in a higher voltage environment, the capacitor must be checked for voltage. For European product standards, the device attached to the power grid must have a reactive power < 10 Var, which results in a cap that must be < 0.67 μ F, from which L can also be selected to match the frequency.
3. Possible surge protection: To save size on the PCB, this module does not design the surge protection parts. If the user wants the option to design surge protection parts, he or she can add a bi-direction transient-voltage suppression (TVS) diode with a shunt connection to attach on the LV side of the transformer. The stable voltage of the TVS must be exactly $\frac{1}{2}$ of the PA voltage of the AFE, which means a 12-V AFE must use a 6-V TVS and a 15-V AFE must use a 7.5-V TVS. This $\frac{1}{2}$ ratio is based on the fact that:
 - (a) The PA of the AFE is a type AB, which uses a single power rail. So, the 12-V powered PA TX output is at a 6-V bias with a ± 6 -V amplitude, meaning that the signal has a ± 6 -V range. While on transmission, the TVS must not be allowed to saturate the signal, so the stable voltage must be kept to $\geq \frac{1}{2}$ of the PA power rail.
 - (b) If a 12-V PA uses a 7.5-V TVS, during the arrival of a surge pulse, the LV side bias is locked-on at 7.5 V, but if the surge occurs at the exact moment of a TX maximum amplitude (which is 6 V), then the signal on the TX route is 7.5 V + 6 V = 13.5 V, which is higher than the power rail and causes damage to the PA of the AFE. So, the TVS voltage must be $\leq \frac{1}{2}$ of the PA power rail.
 - (c) TVS = $\frac{1}{2}$ of the PA rail.

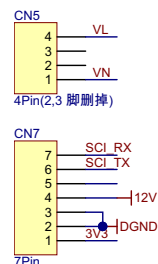


Figure 7. Interface

The user can use the pins in [Figure 7](#) to implement this PLC Lite module, which includes two power grid pins, a 3.3-V DC supply, a 12-V DC supply, and a UART interface.

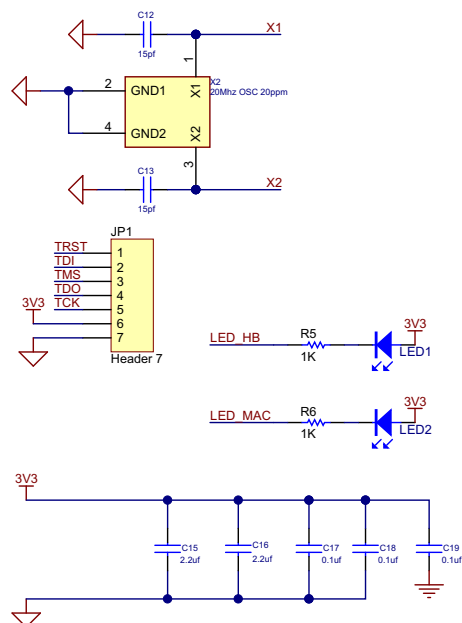


Figure 8. JTAG and Other Parts

Figure 8 shows the JTAG interface, MCU, external oscillator (OSC), and other parts. As Figure 2 shows, the JTAG is located on the right-side edge of the device and displays pins 7 through 1 from top to bottom.

6 Using the Module

The module must use the software implemented on <http://www.ti.com/tool/TIDM-PLCLITE-PLUGMODULE>. After flashing the firmware and powering on the 3.3-V DC input, the user can connect the UART to the PC while using a baud rate of 57600, 8 bits, 1 bit stop, and without parity. The debugging process must use hex input and output.

The detailed HCT protocol definitions must refer back to the TI_PLCLite_Host_Msg.pdf downloadable document from the preceding link. The following are examples of HCT protocol definitions:

Example 1. TX

Host sends: 00 80 08 00 F3 B2 00 00 01 00 (2 bytes of message).

By the definition of HCT protocol, the first byte of every message is a command type of code. Here code 00 represents a "DATA_TRANSFER" type of command. The PLC Lite software delivers several types of command codes in addition to 00; there is 01, which indicates "GET_SYSTEM_INFO"; there is 0C, which indicates "LOAD_SYSTEM_CONFIG"; there is 04, which indicates "SET_INFO"; and there is 14, which indicates "GET_INFO".

80: This code indicates that "this message is from the host to the PLC module", while 00 indicates that "this message is from the PLC module to the host".

08 00: The length of bytes in the rest of the package. HCT protocol requires that all package sections are 16-bit aligned and that the LSB be counted first. So in the length section, 08 00 means 0x0008, which is 8 bytes. The 8 bytes include 4 bytes CRC (F3 B2 00 00), 2 bytes submode code (01 00), and the user's 2-byte message. Due to a 16-bit alignment requirement, if the user wants to transmit an odd length message (such as 3 bytes AB CD EF), the message part must input AB CD EF 00 for a 16-bit alignment, and this section of length must input 09 00 (4 bytes CRC + 2 bytes submode code + 3 bytes of useful payload length = 9 bytes).

F3 B2: Header CRC, the CRC-16 of 00 80 08 00, LSB first.

00 00: Payload CRC, the CRC-16 of 01 00 (2 bytes of message), LSB first, 00 00 means to notice the software "Do not be concerned with the payload CRC, accept it".

01 00: The submode of the "DATA_TRANSFER" and 0001, which is "Request", indicates to send the payload next to the power line.

Host receives: 00 00 08 00 A9 89 00 00 02 00 00 00.

The other parts have the same meaning. The 02 00 is the submode of the "DATA_TRANSFER", "Confirm" is 0002, and the last 00 00 indicates "Success". This message must be sent from the PLC module to the host, which means that the PLC sent out the message.

Example 2. RX

Host receives: 00 00 10 00 73 03 00 00 03 00 (10 bytes received in this message).

As above, 00 indicates that the message is received, 10 00 (or 0x0010) indicates that the message contains $16 - 6 = 10$ bytes of content (CRC 4, Indication 2), and 03 00 is the submode of the "DATA_TRANSFER" Indication. This message tells the host which nodes send out 10 bytes of information to other nodes on the PLC module-mounted grid network.

7 Design Files

7.1 Schematics

To download the schematic, see the design files at [TIDM-PLCLITE-PLUGMODULE](#).

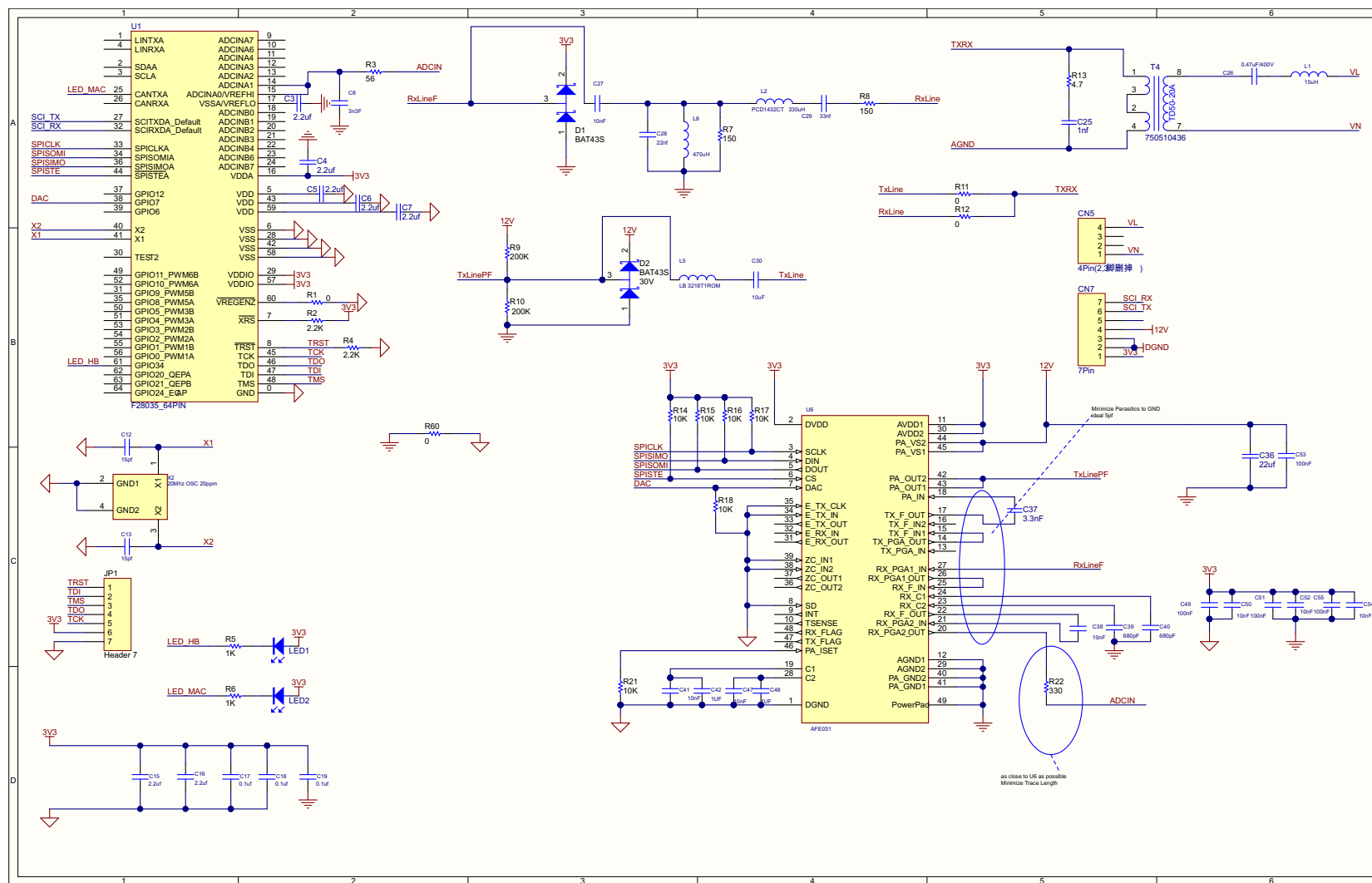


Figure 9. TIDM-PLCLITE-PLUGMODULE Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDM-PLCLITE-PLUGMODULE](#).

7.3 PCB Layout

To download the layer plots, see the design files at [TIDM-PLCLITE-PLUGMODULE](#).

7.4 Altium Project

To download the Altium project files, see the design files at [TIDM-PLCLITE-PLUGMODULE](#).

7.5 Gerber Files

To download the Gerber files, see the design files at [TIDM-PLCLITE-PLUGMODULE](#).

7.6 Software Files

To download the software files, see the design files at [TIDM-PLCLITE-PLUGMODULE](#).

8 References

1. Texas Instruments, *TMS320F28030/28031/28032/28033/28034/28035 Piccolo Microcontrollers*, Datasheet, ([SPRS584](#)).
2. Texas Instruments, *Powerline Communications Analog Front-End*, Datasheet, ([SBOS531](#)).

9 About the Author

HARVEY WANG is a systems application engineer for TI China MCU SAE since joining TI in July 2012. Harvey's work focuses mainly on smart grid power line communication technology and support for other C2000™-related digital power and motor control technologies.

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