AKD4634EN-A

AK4634EN Evaluation board Rev.2

GENERAL DESCRIPTION

AKD4634EN-A is an evaluation board for the AK4634EN, 16bit mono CODEC with MIC/SPK/VIDEO amplifier. The AKD4634EN-A can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). AKD4634EN-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4634EN-A --- Evaluation board for AK4634EN
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

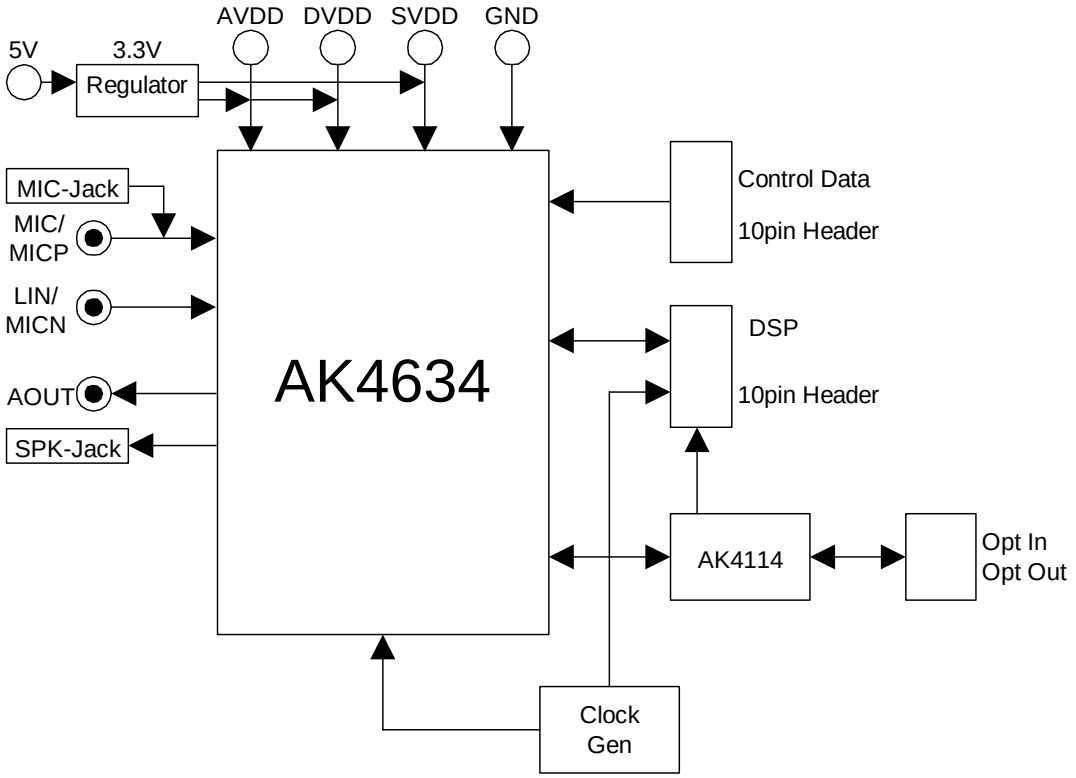


Figure 1. AKD4634EN-A Block Diagram

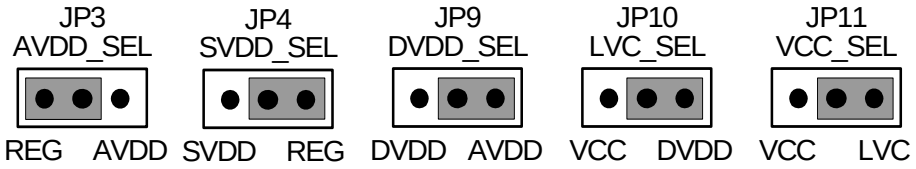
* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

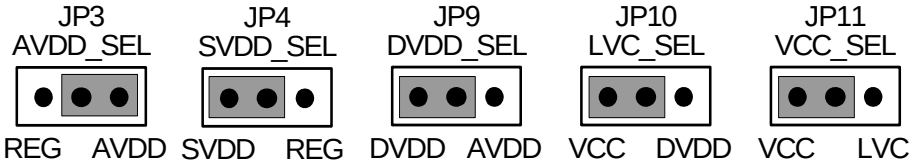
1) Set up the power supply lines.

1-1) When AVDD, DVDD, SVDD and VCC are supplied from the regulator. <Default>



[REG]	(red)	= 5V	
[AVDD]	(orange)	= open	: 3.3V is supplied to AVDD of AK4634EN from regulator.
[DVDD]	(orange)	= open	: 3.3V is supplied to DVDD of AK4634EN from regulator.
[SVDD]	(blue)	= open	: 3.3V is supplied to SVDD of AK4634EN from regulator.
[VCC]	(orenge)	= open	: 3.3V is supplied to logic block from regulator.
[AVSS]	(black)	= 0V	: for analog ground
[SVSS]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

1-2) When AVDD, DVDD, SVDD and VCC are supplied from the power supply connectors.



[REG]	(red)	= open.	
[AVDD]	(orange)	= 2.2 ~ 3.6V	: for AVDD of AK4634EN (typ. 3.3V)
[DVDD]	(orange)	= 2.7 ~ 3.6V	: for DVDD of AK4634EN (typ. 3.3V)
[SVDD]	(blue)	= 2.2 ~ 4.0V	: for SVDD of AK4634EN (typ. 3.3V)
[VCC]	(orenge)	= 2.7 ~ 3.6V	: for logic (typ. 3.3V)
[AVSS]	(black)	= 0V	: for analog ground
[SVSS]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

* Each supply line should be distributed from the power supply unit.
DVDD and VCC must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

The AK4634EN and AK4114 should be reset once bringing SW1, 2 “L” upon power-up.

■ Evaluation mode

In case of AK4634EN evaluation using AK4114, it is necessary to correspond to audio interface format for AK4634EN and AK4114. About AK4634EN's audio interface format, refer to datasheet of AK4634EN. About AK4114's audio interface format, refer to Table 2 in this manual.

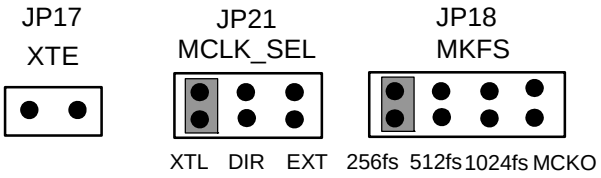
Applicable Evaluation Mode

(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode (Default)
(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode
(PLL Reference CLOCK: MCKI pin)
(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode
(PLL Reference CLOCK: BICK or FCK pin)
(4) Evaluation of loop-back mode (A/D → D/A) : EXT, Master Mode
(5) Evaluation of using DIR/DIT of AK4114 (opt-connector) : EXT, Slave Mode

(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode (Default)

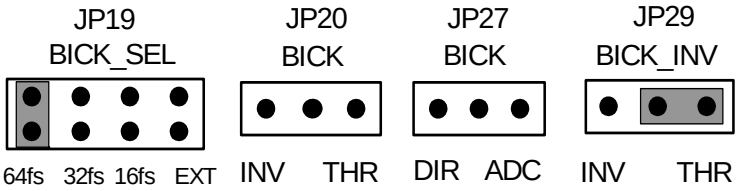
a) Set up jumper pins of MCKI clock

Set "No.8 of SW3" to "H". X'tal of 12MHz, 13.5MHz, 24MHz or 27MHz can be set in X1. X'tal of 12MHz (Default) is set on the AKD4634EN-A.
When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz) through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

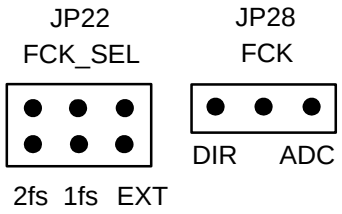


b) Set up jumper pins of BICK clock

Output frequency (16fs/32fs/64fs) of BICK should be set by "BCKO1-0 bit" in the AK4634EN.
There is no necessity for set up JP19.

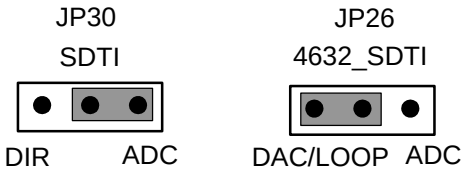


c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

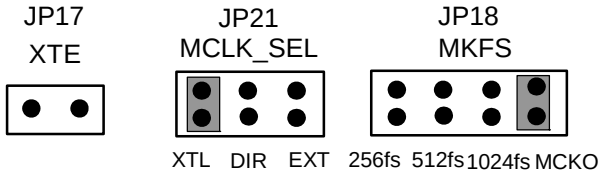
When the AK4634EN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)

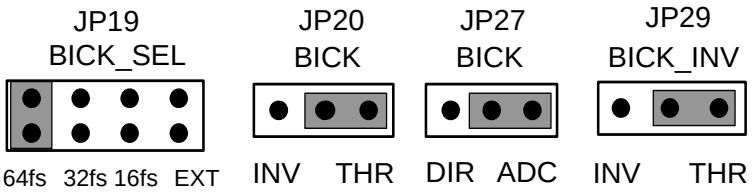
a) Set up jumper pins of MCKI clock

X'tal of 12MHz, 13.5MHz, 24MHz or 27MHz can be set in X1. X'tal of 12 MHz (Default) is set on the AKD4634EN-A. In this case, the AK4634EN corresponds to PLL reference clock of 12MHz. In this evaluation mode, the output clock from MCKO-pin of the AK4634EN is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Then "MCKO bit" in the AK4634EN is set to "1". When an external clock through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

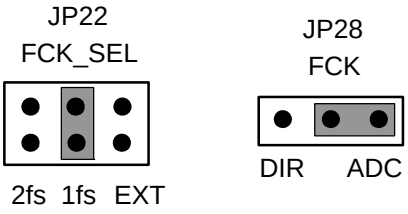


b) Set up jumper pins of BICK clock

Input frequency of BICK should be set 64fs/32fs/16fs by JP19.

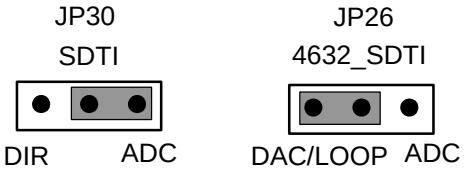


c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

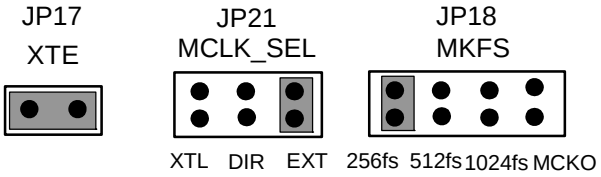
When the AK4634EN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode
(PLL Reference CLOCK: BICK or FCK pin)

a) Set up jumper pins of MCKI clock

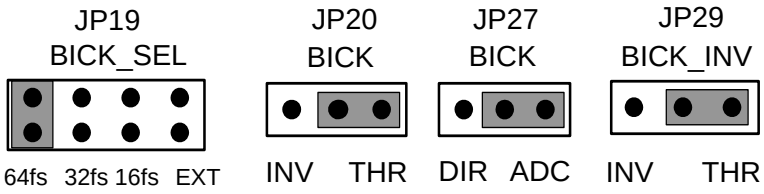
An external clock through a RCA connector (J8: EXT/BICK), BICK and FCK clocks are generated by the divider. JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.



*When BICK and FCK clocks through a RCA connector (J8, J9) is supplied, select XTL on JP21.
*When X'tal is used, X'tal of 256fs, 512fs or 1024fs can be set in X1. Set OPEN on JP17, and select XTL on JP21.

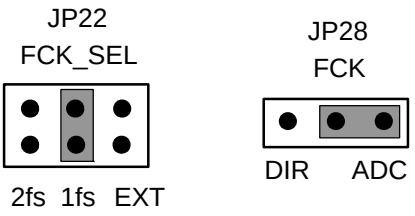
b) Set up jumper pins of BICK clock

Input frequency of BICK should be set 64fs/32fs/16fs by JP19.



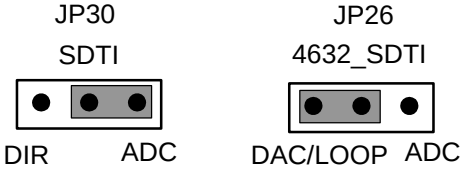
*When BICK and FCK clocks through a RCA connector (J8, J9) is supplied, select EXT on JP19. JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

c) Set up jumper pins of FCK clock



*When BICK and FCK clocks through a RCA connector (J8, J9) is supplied, select EXT on JP22. JP24 (EXT1) and R27 should be properly selected in order to much the output impedance of the clock generator.

d) Set up jumper pins of DATA



When the AK4634EN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.

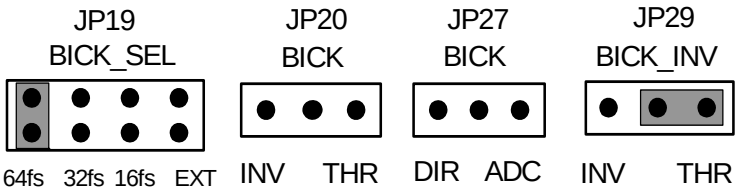
(4) Evaluation of loop-back mode (A/D → D/A) : EXT, Master Mode

a) Set up jumper pins of MCKI clock

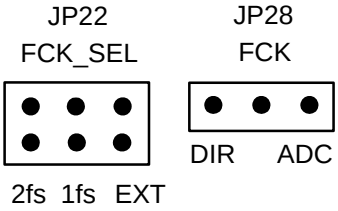
Set "No.8 of SW3" to "H". An external clock (256fs, 512fs or 1024fs) through a RCA connector (J8: EXT/BICK) is supplied. JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

b) Set up jumper pins of BICK clock

Output frequency (32fs or 64fs) of BICK should be set by "BCKO1-0 bit" in the AK4634EN.
There is no necessity for set up JP19.

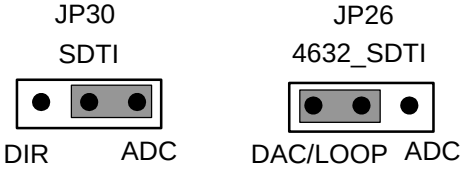


c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

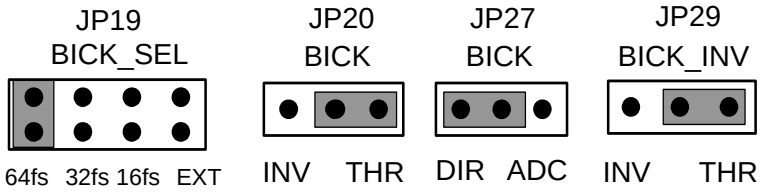
When the AK4634EN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



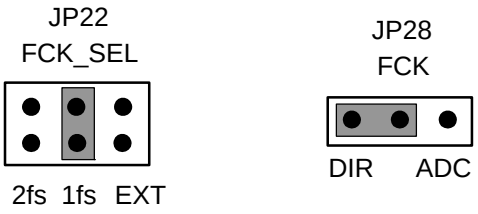
(5) Evaluation of using DIR/DIT of AK4114 (opt-connector) : EXT, Slave Mode

a) Set up jumper pins of MCKI clock

b) Set up jumper pins of BICK clock

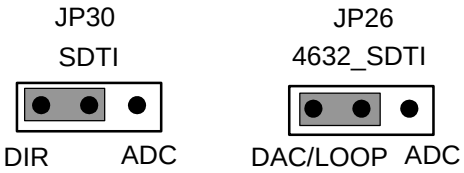


c) Set up jumper pins of FCK clock

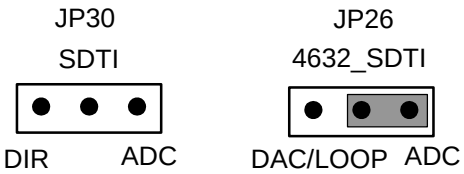


d) Set up jumper pins of DATA

When D/A converter of the AK4634EN is evaluated by using DIR of AK4114, the jumper pins should be set to the following.



When A/D converter of the AK4634EN is evaluated by using DIT of AK4114, the jumper pins should be set to the following.



■ DIP Switch set up

[SW3] (MODE) : Mode Setting of AK4634EN and AK4114
ON is "H", OFF is "L".

No.	Name	OFF ("L")	ON ("H")	Default
1	DIF0	AK4114 Audio Format Setting		Off
2	DIF1	See Table 2		Off
3	DIF2			On
4	CM0	Clock Operation Mode select		Off
5	CM1	See Table 3		On
6	OCKS0	Master Clock Frequency Select		Off
7	OCKS1	See Table 4		Off
8	M/S	Slave mode	Master mode	On

Note. When the AK4634EN is evaluated Master mode, "M/S" is set to "H".
Table 1. Mode Setting for AK4634EN and AK4114

Register setting for AK4634EN		Setting for AK4114 Audio Interface Format					
DIF1 bit	DIF0 bit	DIF0	DIF1	DIF2	DAUX	SDTO	
0	1	L	L	L	24bit, Left justified	16bit, Right justified	
1	0	L	L	H	24bit, Left justified	24bit, Left justified	Default
1	1	H	L	H	24bit, I^2S	24bit, I^2S	

Note. When the AK4634EN is evaluated by using DIR/DIT of AK4114, "No.8 of SW3" is set to "L".
Table 2. Setting for AK4114 Audio Interface Format

Mode	CM0	CM1	UNLOCK	PLL	X'tal	Clock source	SDTO	
0	L	L	-	ON	OFF	PLL	RX	
1	H	L	-	OFF	ON	X'tal	DAUX	
2	L	H	0	ON	ON	PLL	RX	Default
			1	ON	ON	X'tal	DAUX	
3	H	H	-	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-down)

Table 3. Clock Operation Mode select

No.	OCKS0	OCKS1	MCKO1	MCKO2	X'tal	
0	L	L	256fs	256fs	256fs	Default
2	L	H	512fs	256fs	512fs	

Table 4. Master Clock Frequency Select

■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   - OPEN : Separated.
   - SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP3 (AVDD_SEL) : AVDD of the AK4634EN
   - REG : AVDD is supplied from the regulator ("AVDD" jack should be open). < Default >
   - AVDD : AVDD is supplied from "AVDD " jack.

3. JP4 (SVDD_SEL) : SVDD of the AK4634EN
   - REG : SVDD is supplied from the regulator ("SVDD" jack should be open). < Default >
   - SVDD : SVDD is supplied from "SVDD " jack.

4. JP9 (DVDD_SEL) : DVDD of the AK4634EN
   - AVDD : DVDD is supplied from "AVDD". < Default >
   - DVDD : DVDD is supplied from "DVDD " jack.

5. JP10 (LVC_SEL) : Logic block of LVC is selected supply line.
   - DVDD : Logic block of LVC is supplied from "DVDD". < Default >
   - VCC : Logic block of LVC is supplied from "VCC " jack.

6. JP11 (VCC_SEL) : Logic block is selected supply line.
   - LVC : Logic is supplied from supply line of LVC. < Default >
   - VCC : Logic block of LVC is supplied from "VCC " jack.

7. JP25 (MCKO_SEL) : Master Clock Frequency is selected clock from MCKO1 or MCKO2 of the AK4114.
   - MCKO1 : The check from MCKO1 of AK4114 is provided to MCKI of the AK4634EN. < Default >
   - MCKO2 : The check from MCKO2 of AK4114 is provided to MCKI of the AK4634EN.

8. JP102 (I2C) : Control Interface is selected mode.
   - OPEN : 3-wire Serial Control Mode. < Default >
   - SHORT : I^2C-bus Control Mode. (Not used in this board.)

9. JP103 (MCKO) : Master Clock Frequency is selected from AK4634EN.
   - OPEN : Not supply.
   - SHORT : Supplied from AK4634EN. < Default >

■ The function of the toggle SW

[SW1] (DIR) : Power control of AK4114. Keep "H" during normal operation.
Keep "L" when AK4114 is not used.

[SW2] (PDN) : Power control of AK4634EN. Keep "H" during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4634EN can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4634EN-A

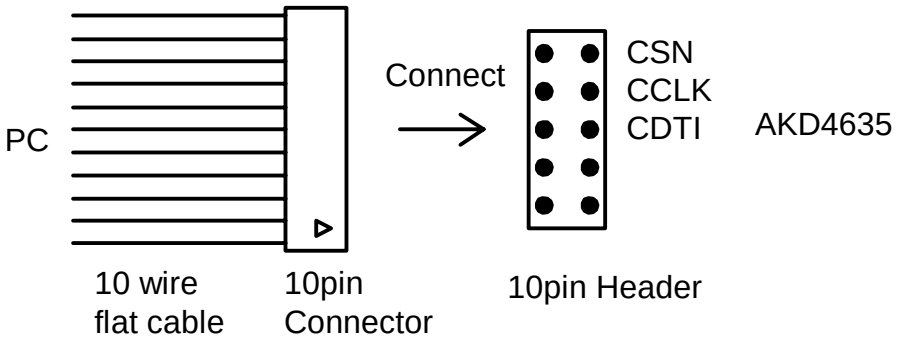


Figure 2. Connect of 10 wire flat cable

■ Analog Input / Output Circuits

(1) Input Circuits

a) MIC/MICP Input Circuit

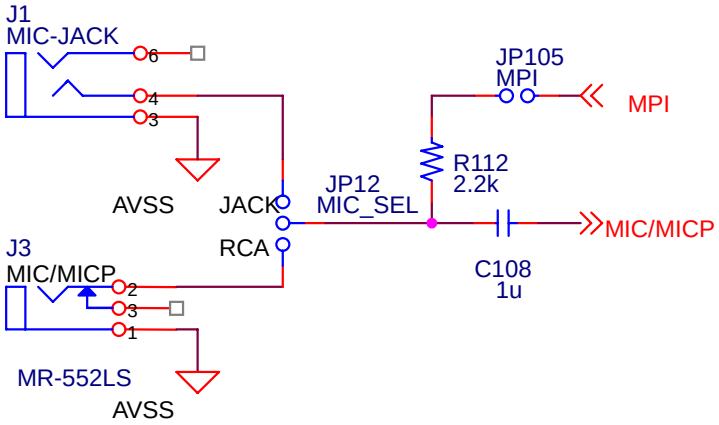
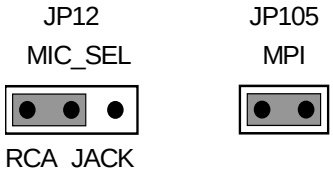


Figure 3. MIC/MICP Input Circuit

(a-1) Analog signal is input to MIC pin via J1 connector.

(a-2) Analog signal is input to MIC/MICP pin via J3 connector.



b) LIN/MICN Input Circuit

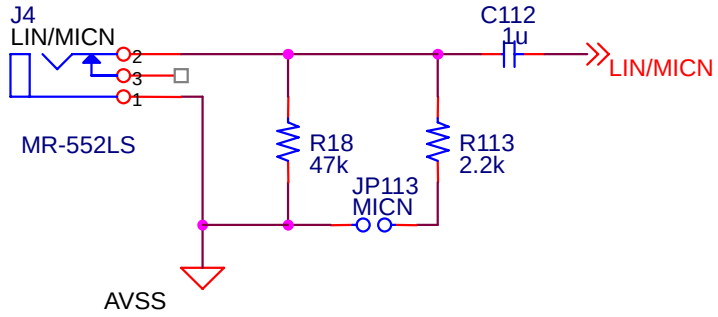
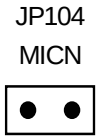


Figure 4. LIN/MICN Input Circuit

(b-1) LIN is input from J4.



(b-2) MICN is input from J4.

(2) Output Circuits

a) AOUT Output Circuit

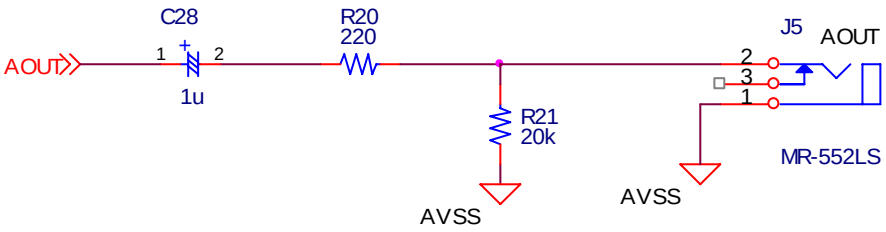


Figure 5. AOUT Output Circuit

C) SPK Output Circuit

Note. When mini-jack is inserted or pulled out J2 (SPK-JACK) connector, JP13 (SPP_SEL) and JP14 (SPN_SEL) should be open, or "PMSPK bit" in the AK4634EN should be set to "0".

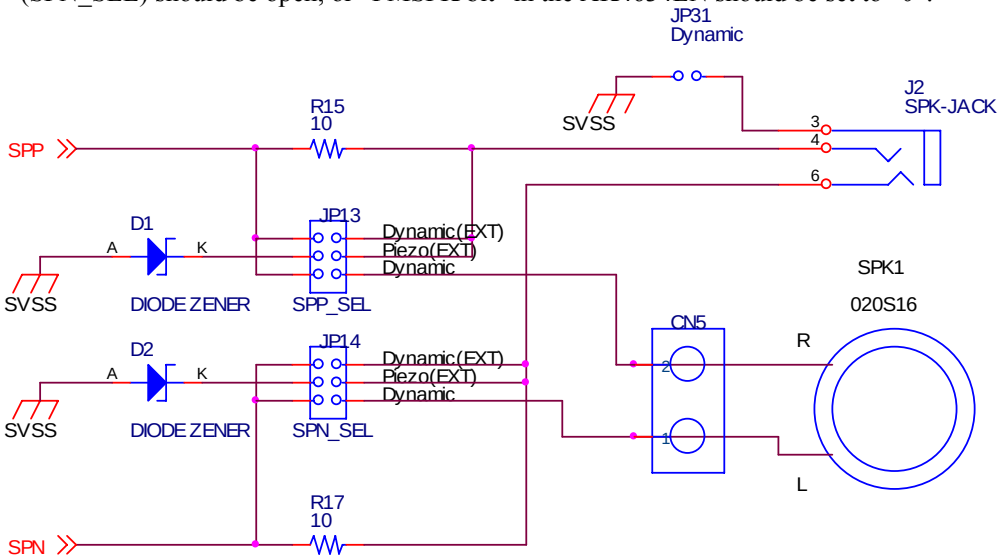
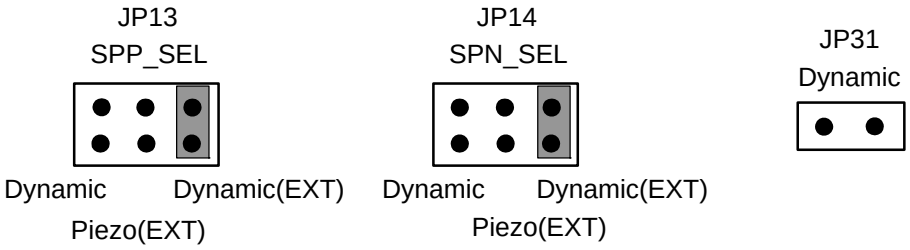
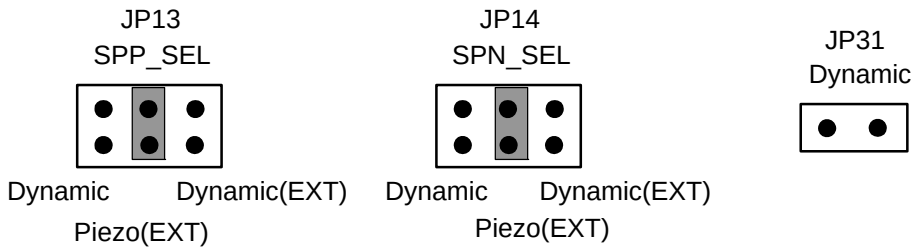


Figure 6. SPK Output Circuit

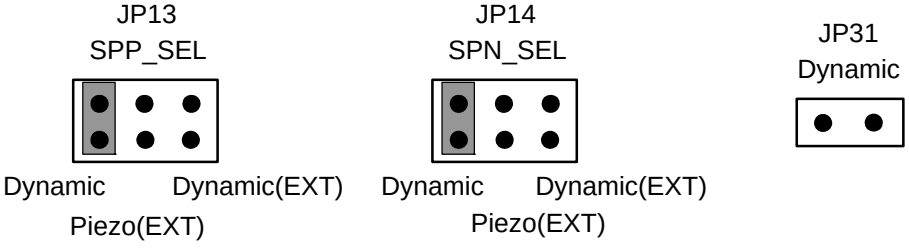
(C-1) "Dynamic Speaker" of external is evaluated by using J2 (SPK-JACK) connector.



(C-2) "Piezo (Ceramic) Speaker" of external is evaluated by using J2 (SPK-JACK) connector.



(C-3) Analog signal of SPP/SPN pins are output "Dynamic Speaker" on the evaluation (SPK1).



∗ AKEMD assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4634EN-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4634EN-A by 10-line type flat cable (packed with AKD4634EN-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4634EN Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "AKD4634EN.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default] : Initialize the register of the AK4634EN.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to write data by keyboard operation.
6. [Function3] : The sequence of register setting can be set and executed.
7. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5] : The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE] : Save the current register setting.
10. [OPEN] : Write the saved values to all register.
11. [Write] : Dialog to write data by mouse operation.
12. [Filter] : Set Programmable Filter (HPF, LPF, EQ1~5) of AK4634EN easily.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to the AK4634EN, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4634EN, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate IVOL, OVOL.

There are dialogs corresponding to register of 09h and 0Ah.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to the AK4634EN by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4634EN, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is "akr".

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is "akr".

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4634EN. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.

Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [OPEN] button on the Function3 window. The extension of file name is “aks”.

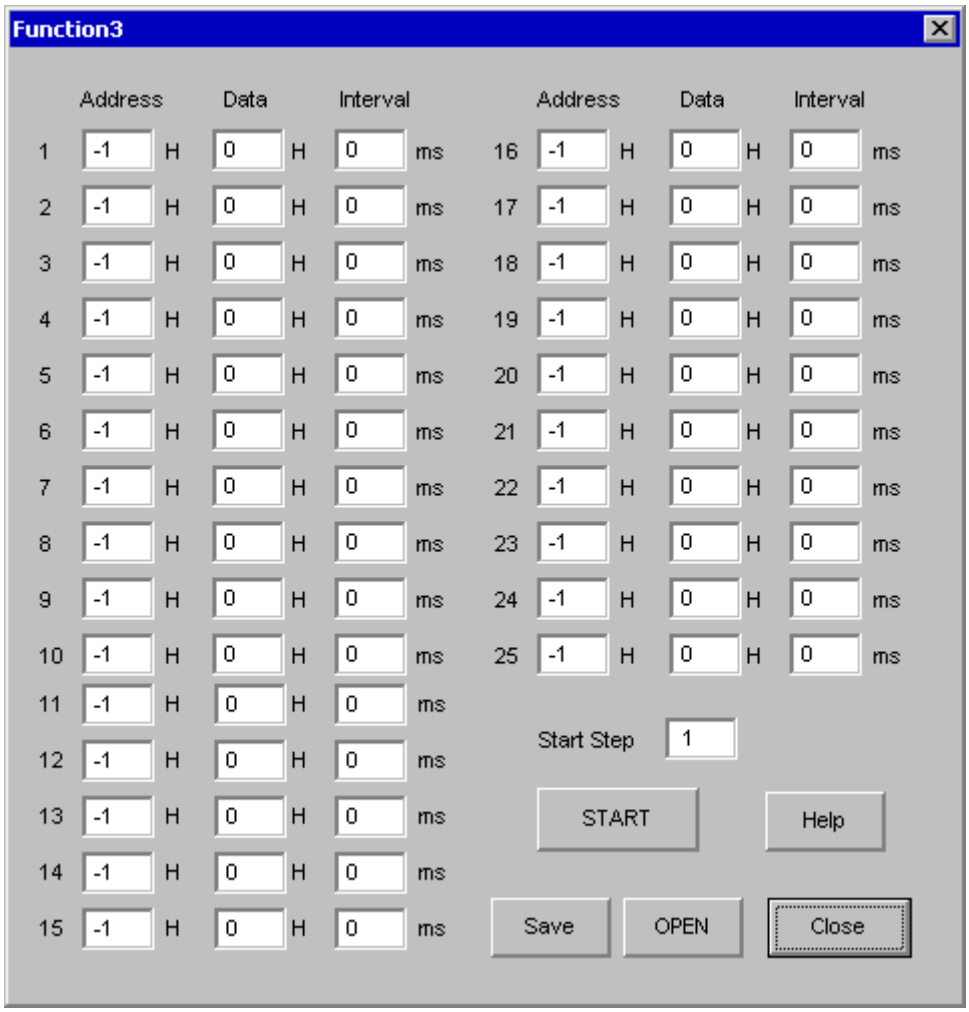


Figure 7. [F3] Window

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 8 opens.

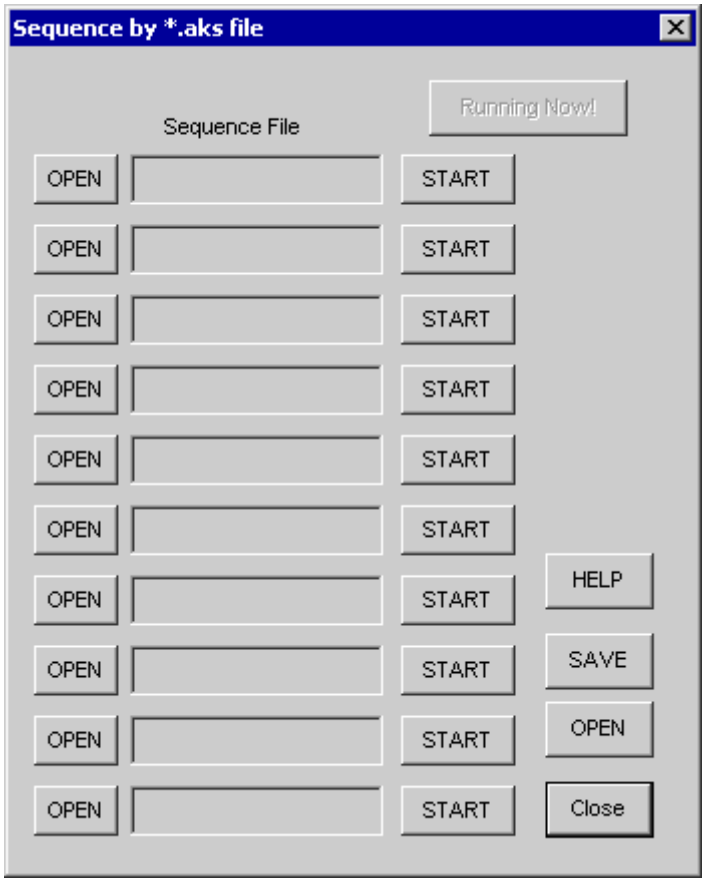


Figure 8. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 9.

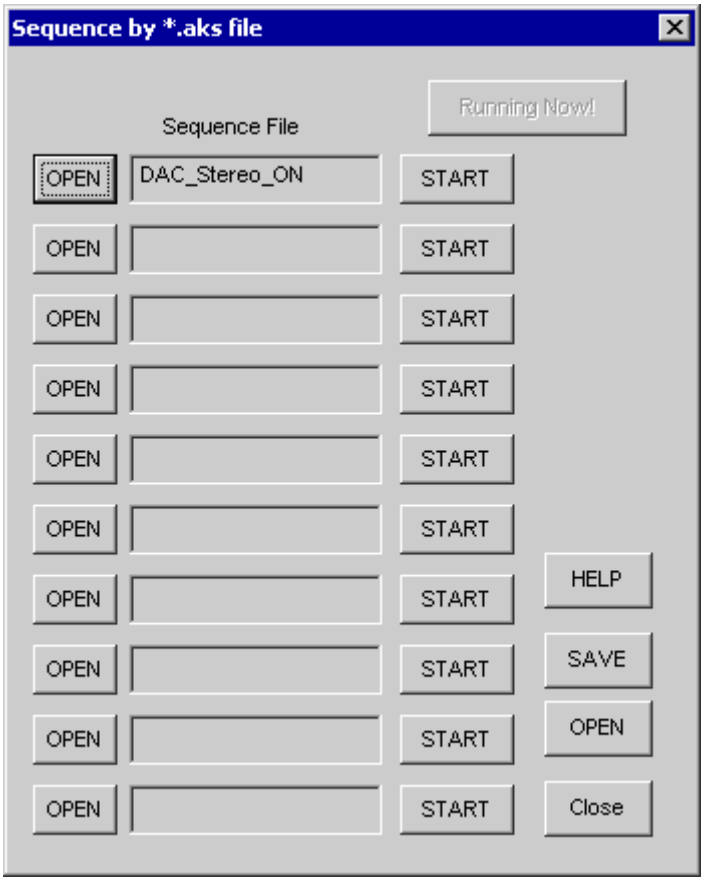


Figure 9. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 10 opens.

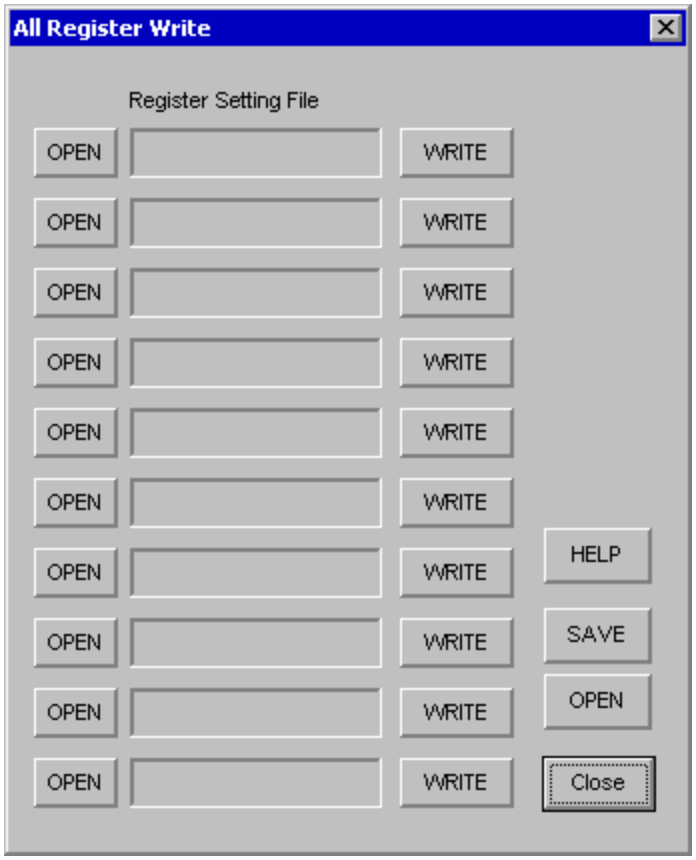


Figure 10. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 11.

(2) Click [WRITE] button, then the register setting is executed.

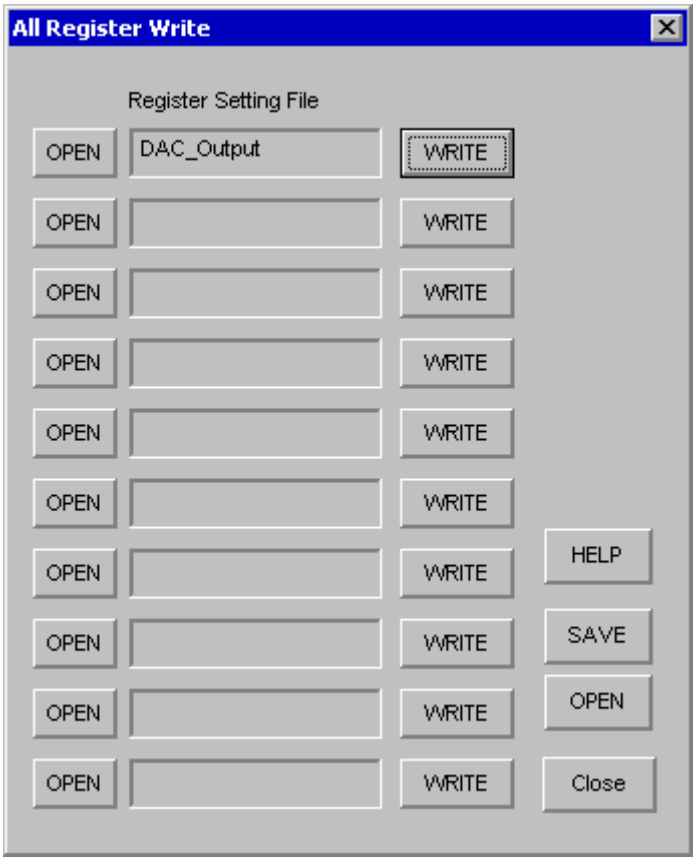


Figure 11. [F5] window (2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

8. [Filter Dialog]

A calculation of a coefficient of Digital Programmable Filter such as HPF,EQ filter ,a write to a register and check frequency response such as HPF,EQ filter.
Window to show to Figure 12 opens when push a [Filter] button .

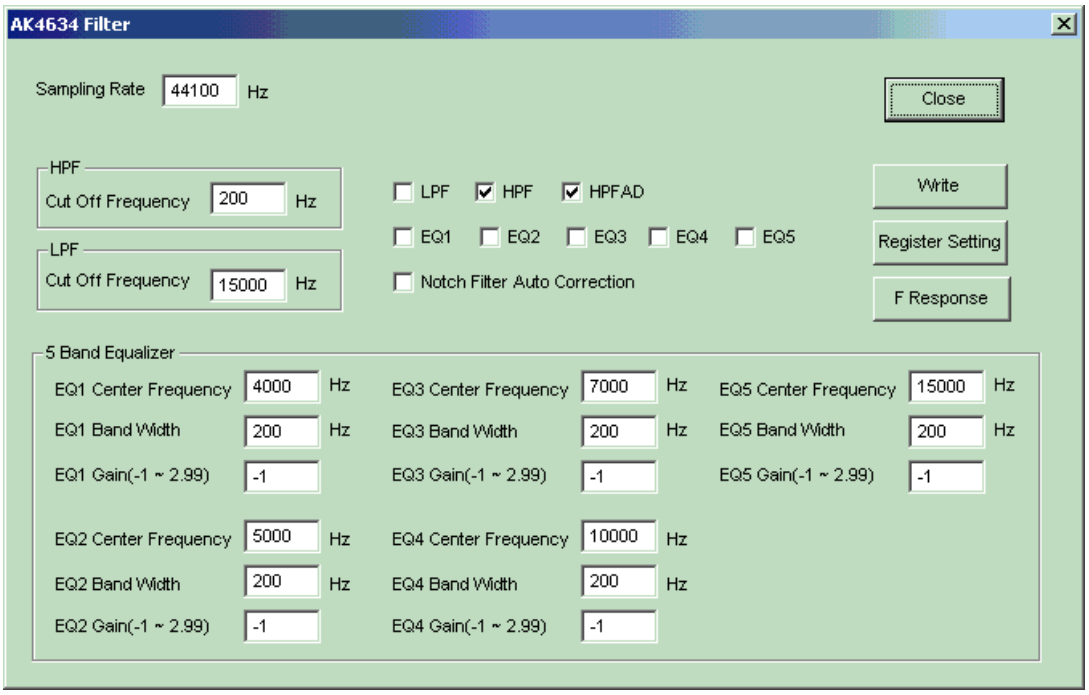


Figure12. [Filter] Window

8-1. Setting of a parameter

(1) Please set a parameter of each Filter.

Item	Contents	Setting range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
HPF		
Cut Off Frequency	High pass filter cut off frequency	fc/fs ≥ 0.0001 (fc min = 1.6Hz at 16kHz)
LPF		
Cut Off Frequency	Low pass filter cut off frequency	fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)
5 Band Equalizer		
EQ1-5 Center Frequency	EQ1-5 Center Frequency	fo_n / fs < 0.497
EQ1-5 Band Width	EQ1-5 Band Width (Note 1)	
EQ1-5 Gain	EQ1-5 Gain (Note 2)	$-1 \leq K_n < 3$

Note 1. A gain difference is a bandwidth of 3dB from center frequency.
Note 2. When a gain is smaller than 0 , EQ becomes a notch filter.

(2) “LPF”, “HPF”, “HPFAD”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5” Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON. When checked “Notch Filter Auto Correction”, perform automatic revision of center frequency of a notch filter. (“Cf. 8-4. automatic revision of center frequency of a notch filter”)

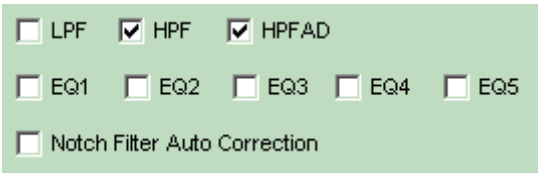


Figure13. Filter ON/OFF setting button

8-2. A calculation of a register

A register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and, a calculation of register setting is not carried out.

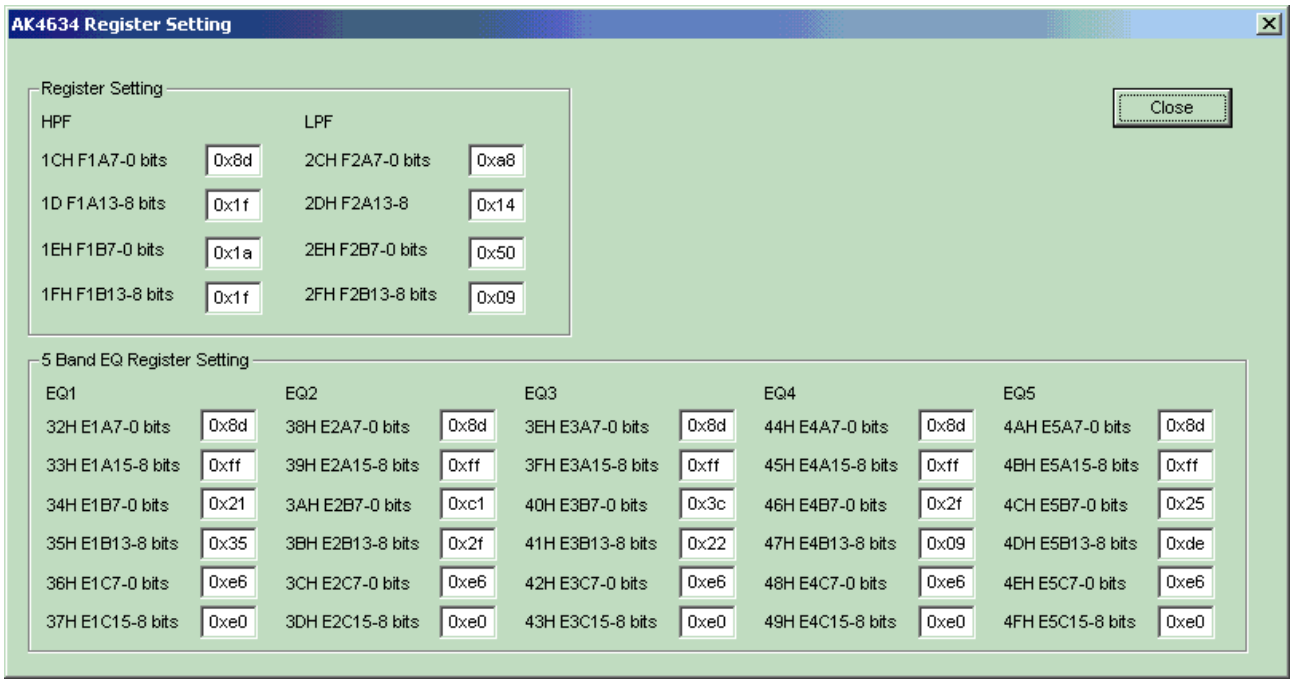


Figure14. A register setting calculation result

When it is as follows that a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

8-3.Indication of a frequency characteristic

A frequency characteristic is displayed when push a [Frequency Response] button. In addition, a register set point is updated then, too.
Change "Frequency Range", and indication of a frequency characteristic is updated when push a [UpDate] button.

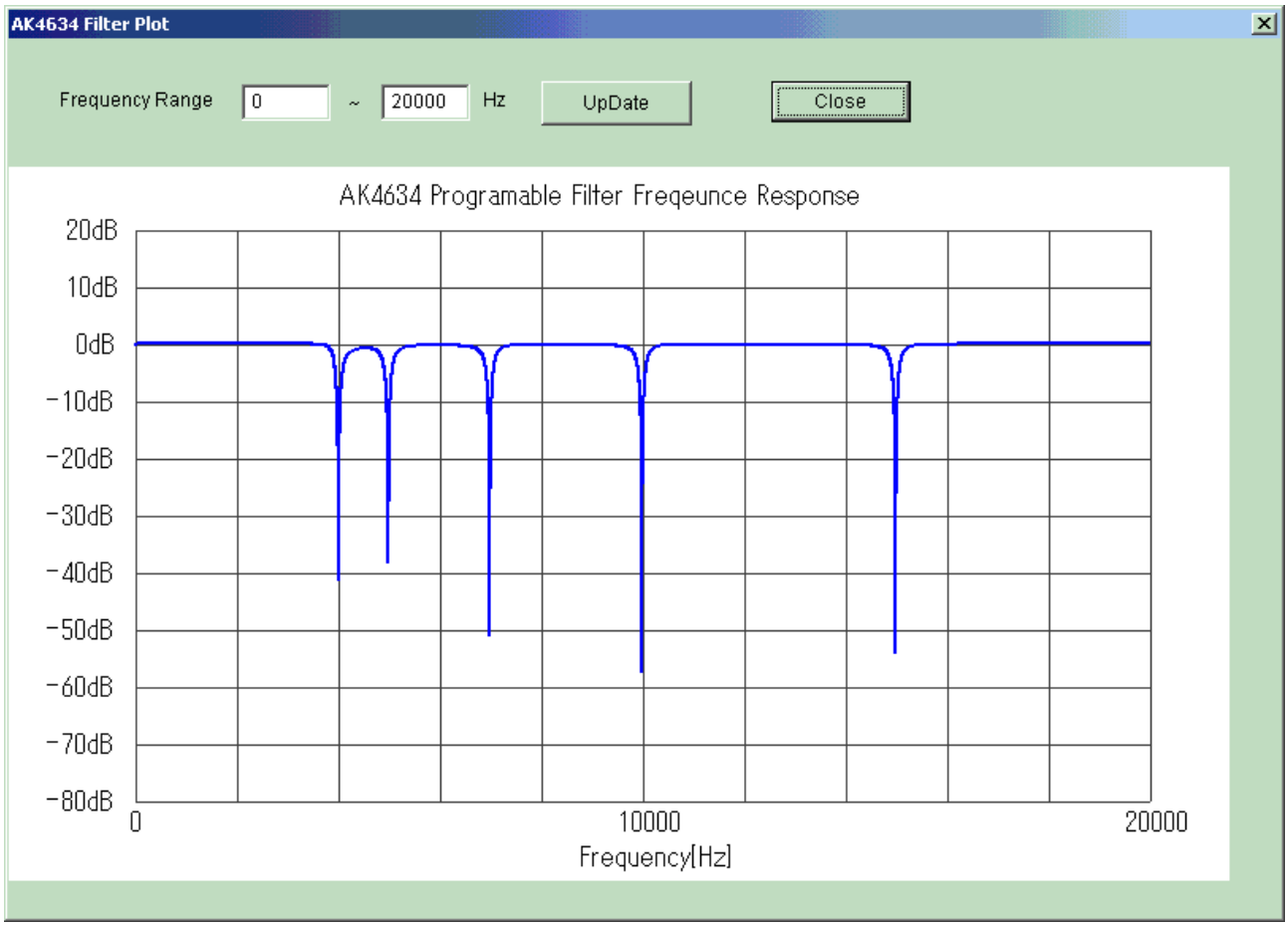


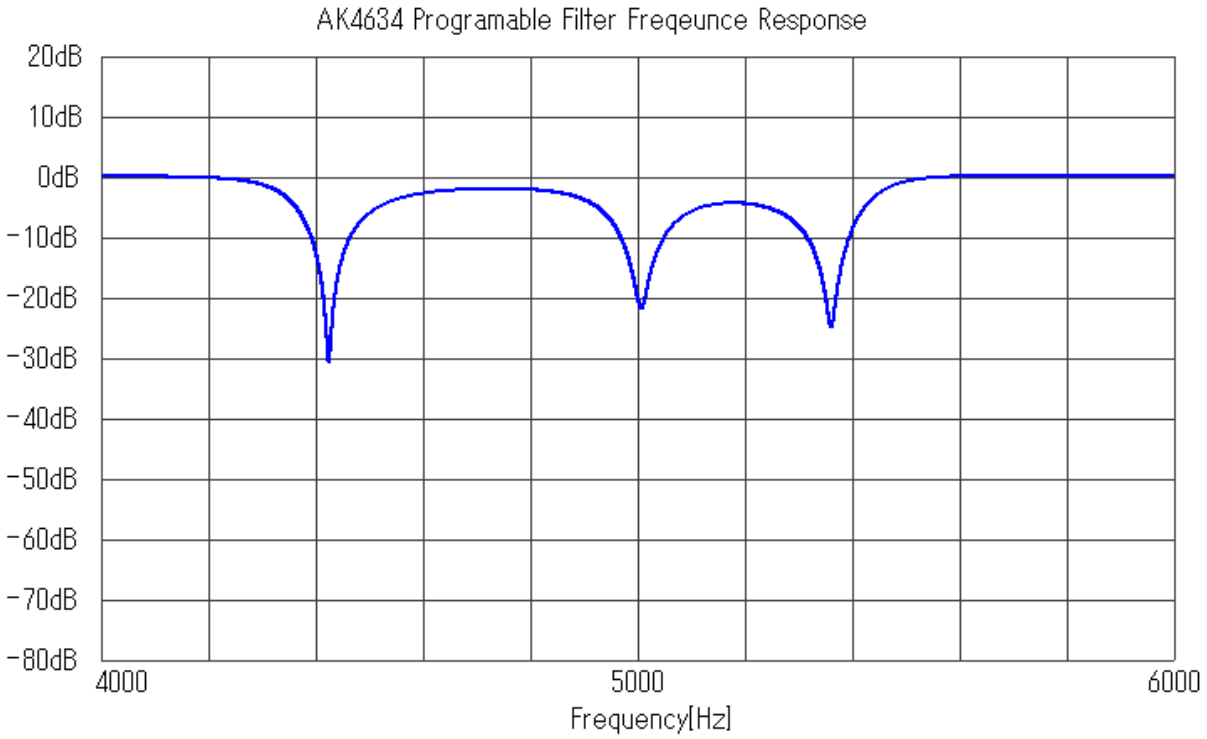
Figure15. A frequency characteristic indication result

When it is as follows that a register set point is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

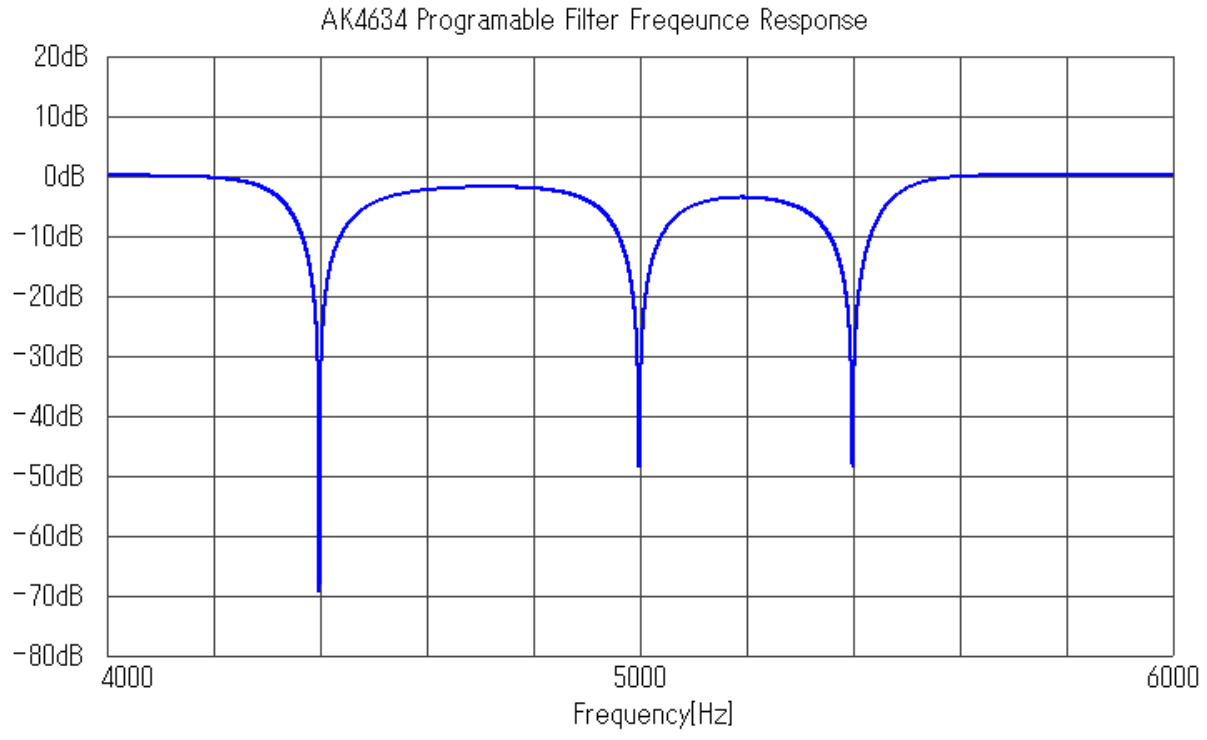
8-4. Automatic revision of center frequency of a notch filter

When set a gain of 5 band Equalizer to -1, Equalizer becomes a notch filter. When center frequency of plural notch filters is adjacent, produce a gap to central frequency (Figure 16). When check "a Notch Filter Auto Correction" button, perform automatic revision of central frequency of a notch filter, display register setting after automatic revision and a frequency characteristic (Figure 17). This automatic revision is availability for Equalizer Band which set a gain to "-1".

(Note) When distance among center frequency is smaller than band width, there is a possibility that automatic revision is not performed definitely. Please confirm a revision result by indication of a frequency characteristic.



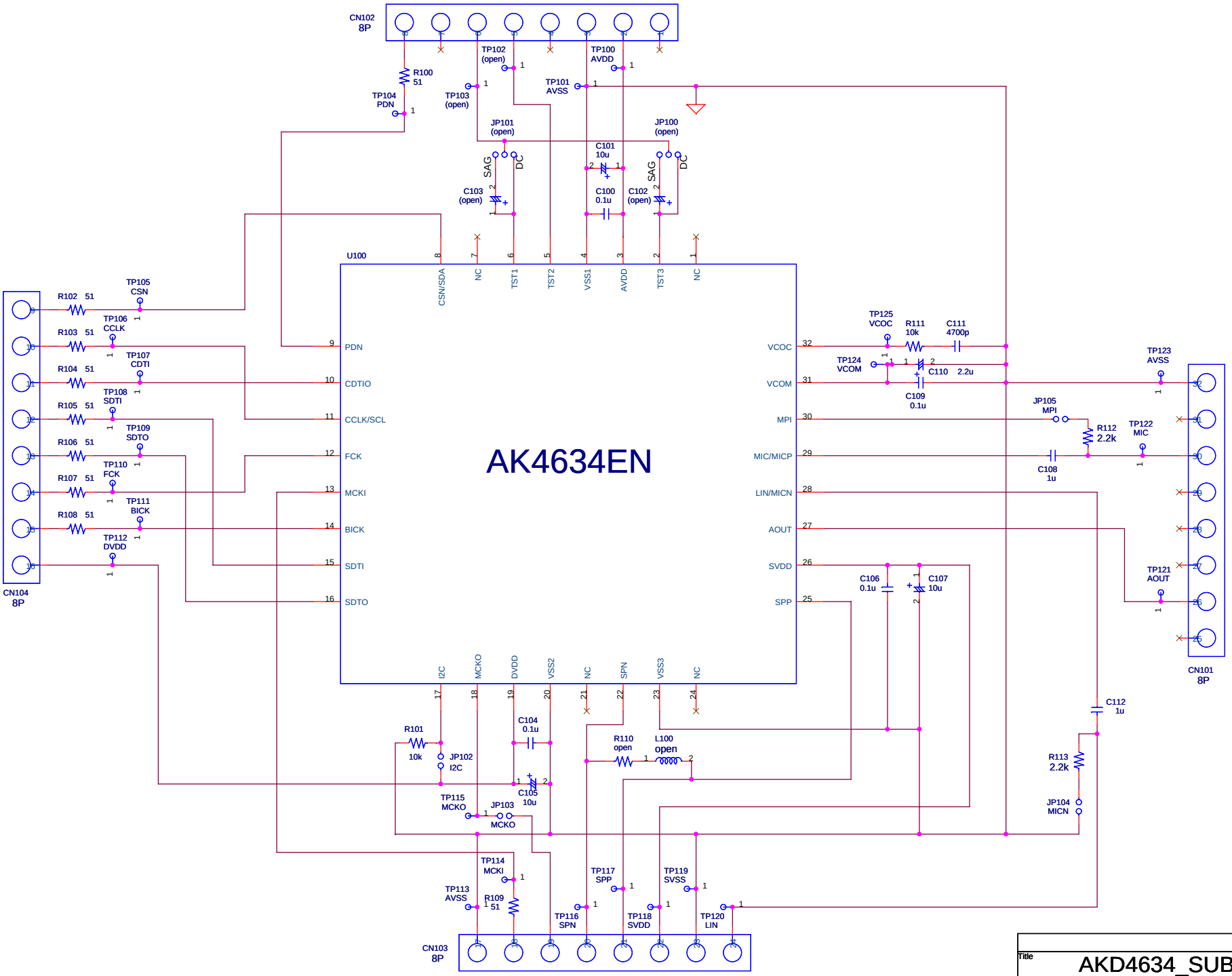
Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width : 200Hz(3 band common)
Figure16. When there is no revision of center frequency



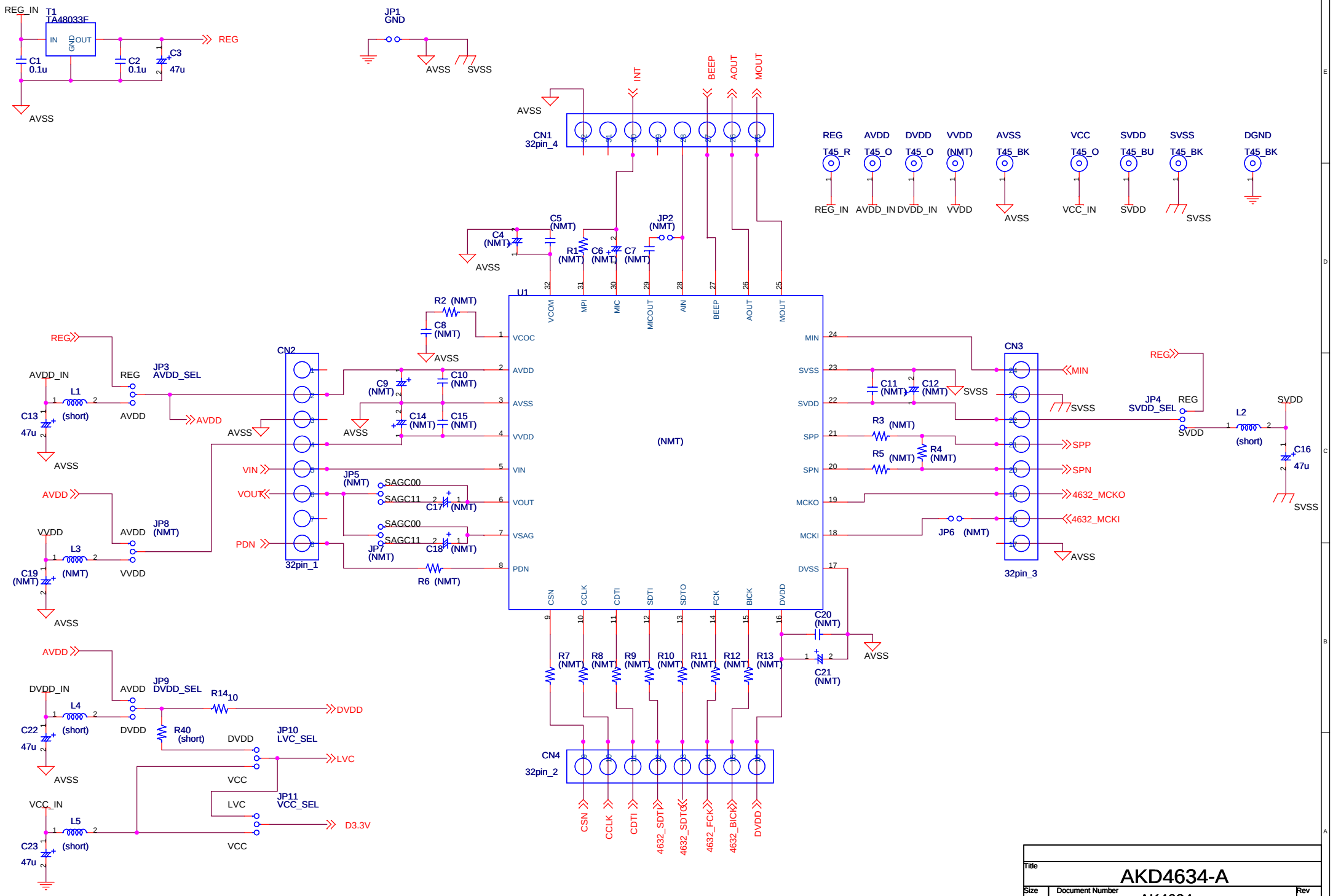
Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width : 200Hz(3 band common)
Figure17. When there is revision of center frequency

Revision History

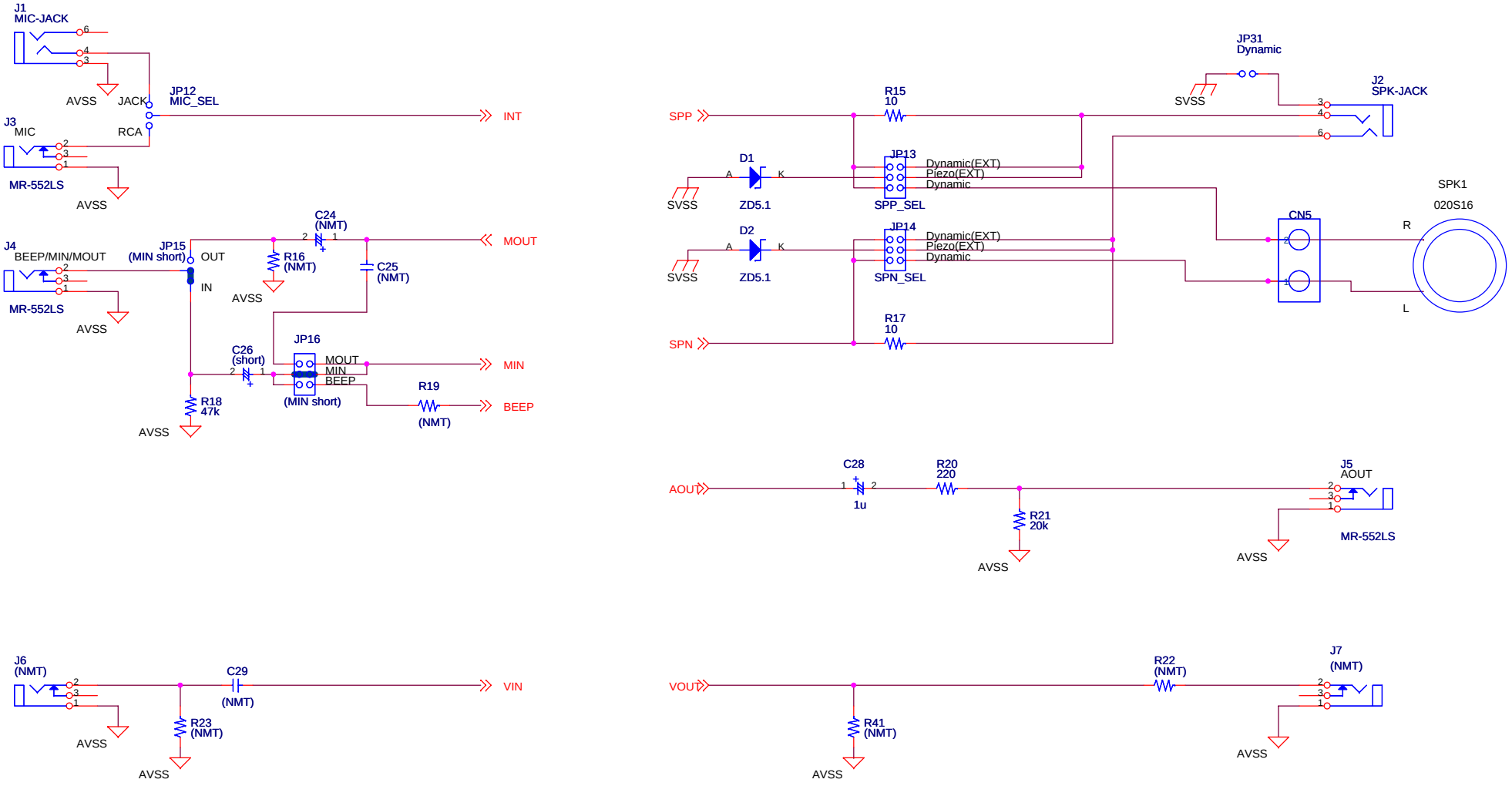
Date	Manual Revision	Board Revision	Reason	Contents
13/09/03	KM115300	2	First Edition	



Title	AKD4634_SUB_32QFN	
Size A3	Document Number AK4634EN	Rev 0
Date: Monday, July 23, 2007	Sheet 1 of 1	

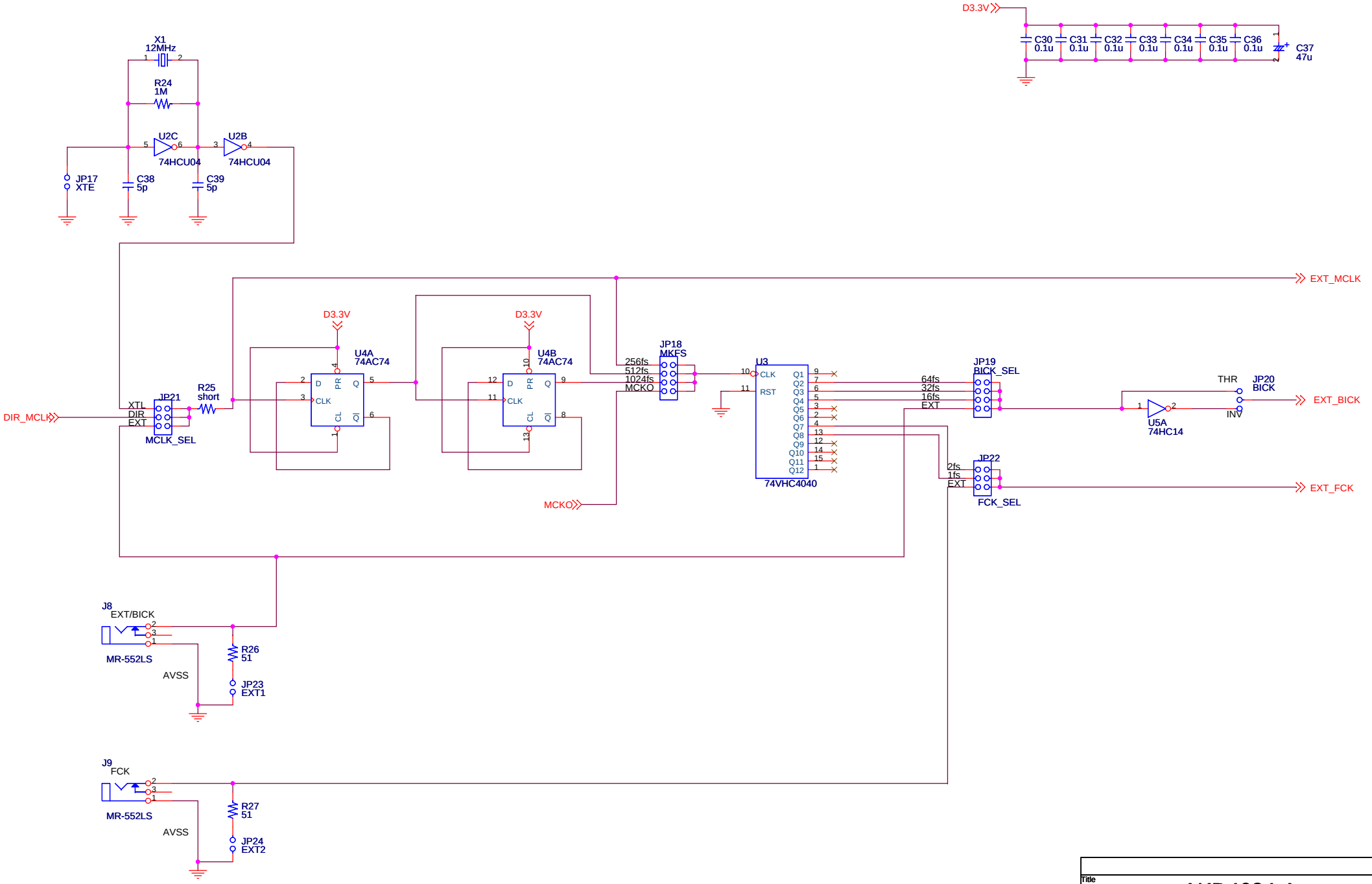


Title	AKD4634-A	
Size A3	Document Number AK4634	Rev 0
Date: Monday, February 26, 2007	Sheet 1 of 5	

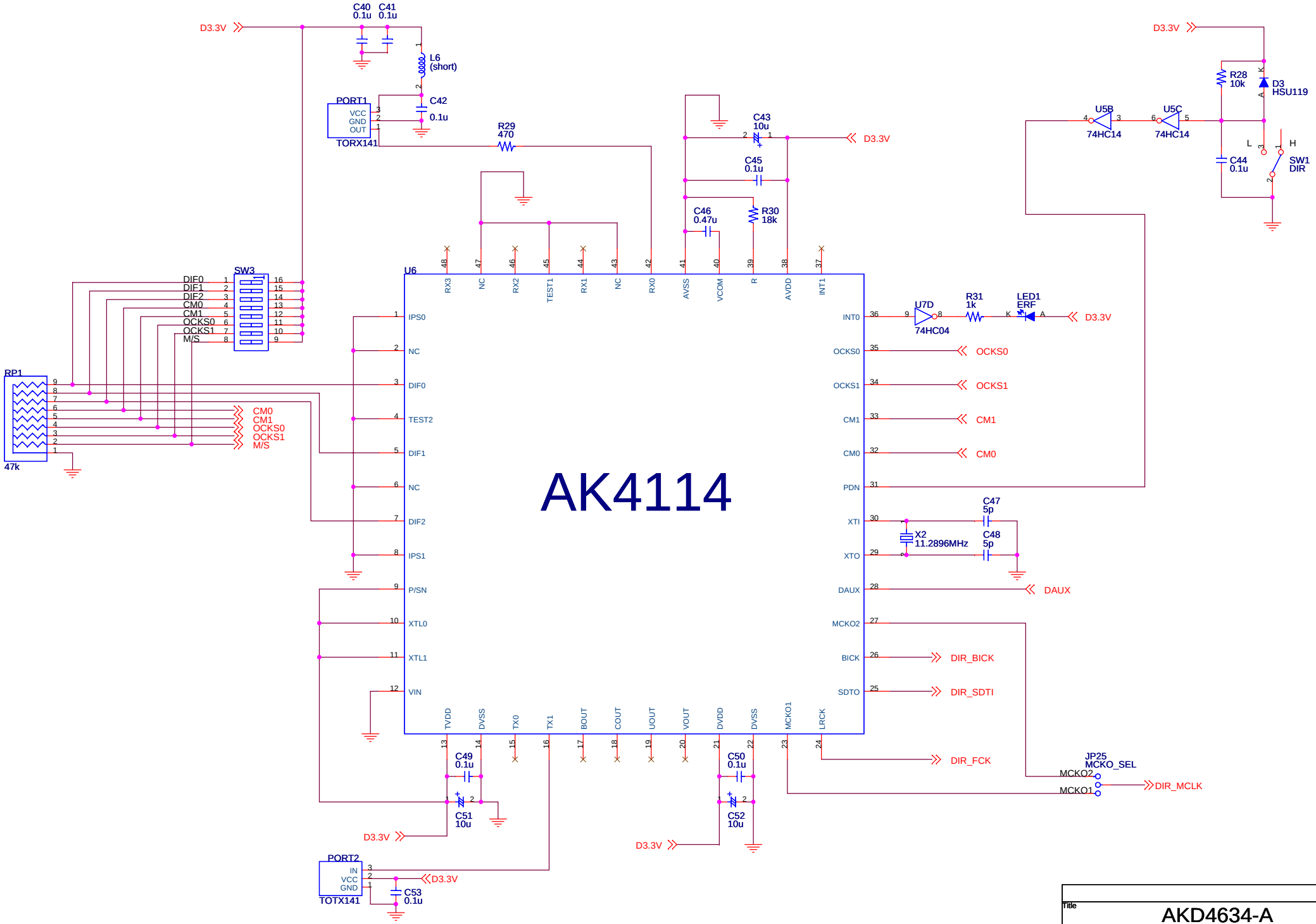


Title	AKD4634-A	
Size: A3	Document Number: Input/Output	Rev: 0
Date: Monday, February 26, 2007	Sheet 2 of 5	

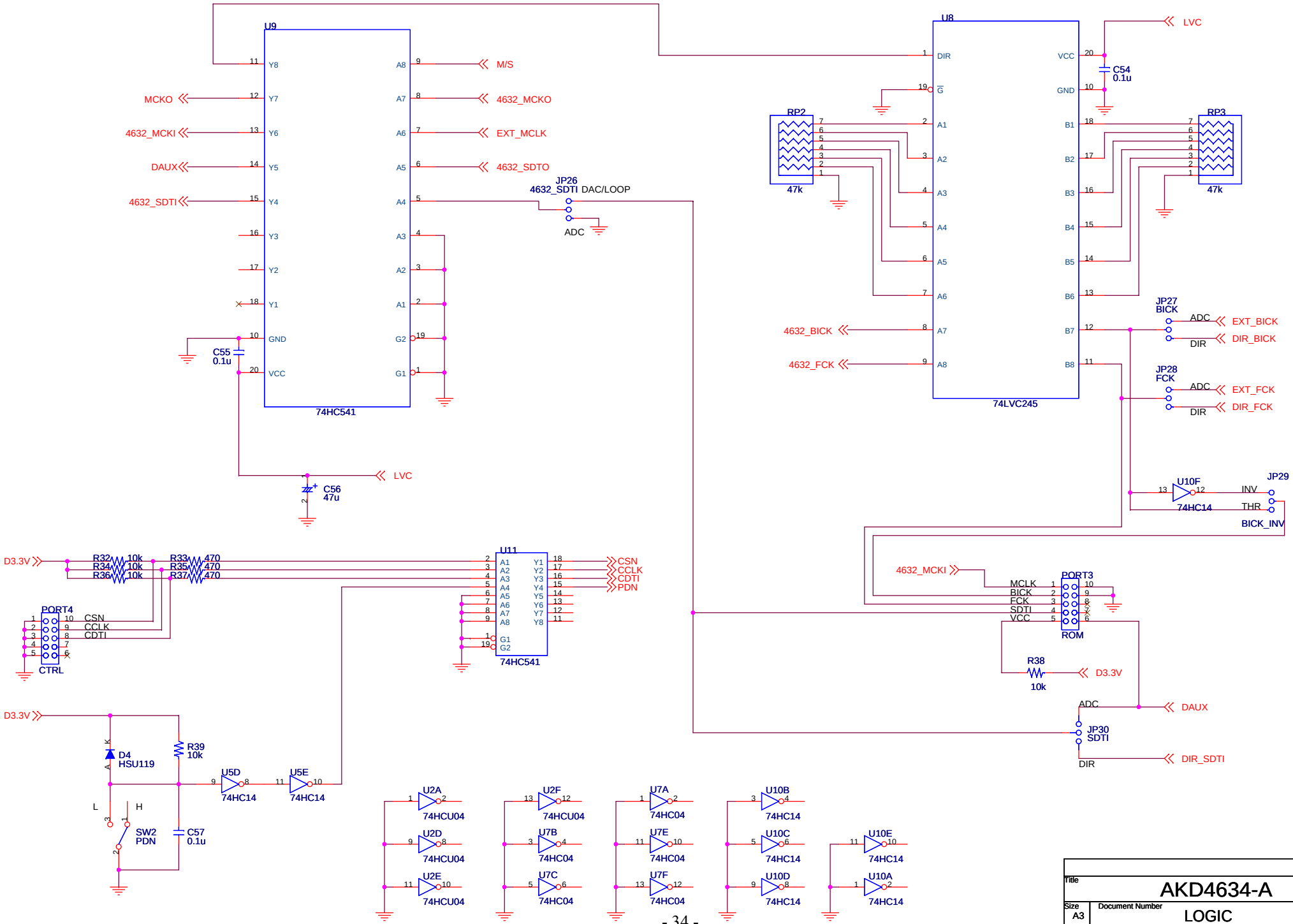
for
74HCU04,74AC74,74VHC4040,74HC14,74HC14,74HC541,74HCT04



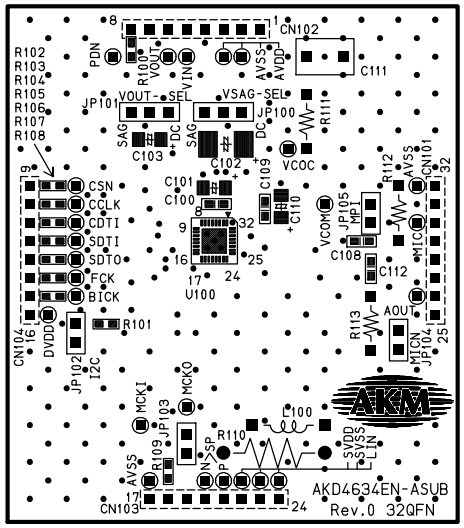
Title	AKD4634-A	
Size A3	Document Number CLOCK	Rev 0
Date: Monday, February 26, 2007	Sheet 3 of 5	



Title	AKD4634-A	
Size A3	Document Number DIR/DIT	Rev 0
Date: Monday, February 26, 2007	Sheet 4 of 5	

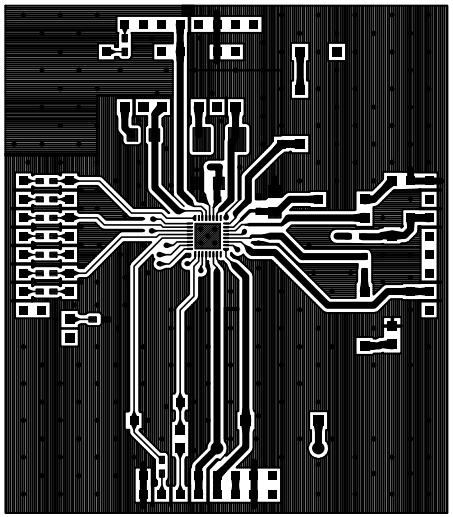


Title	AKD4634-A	
Size A3	Document Number LOGIC	Rev 0
Date: Monday, February 26, 2007	Sheet 5 of 5	



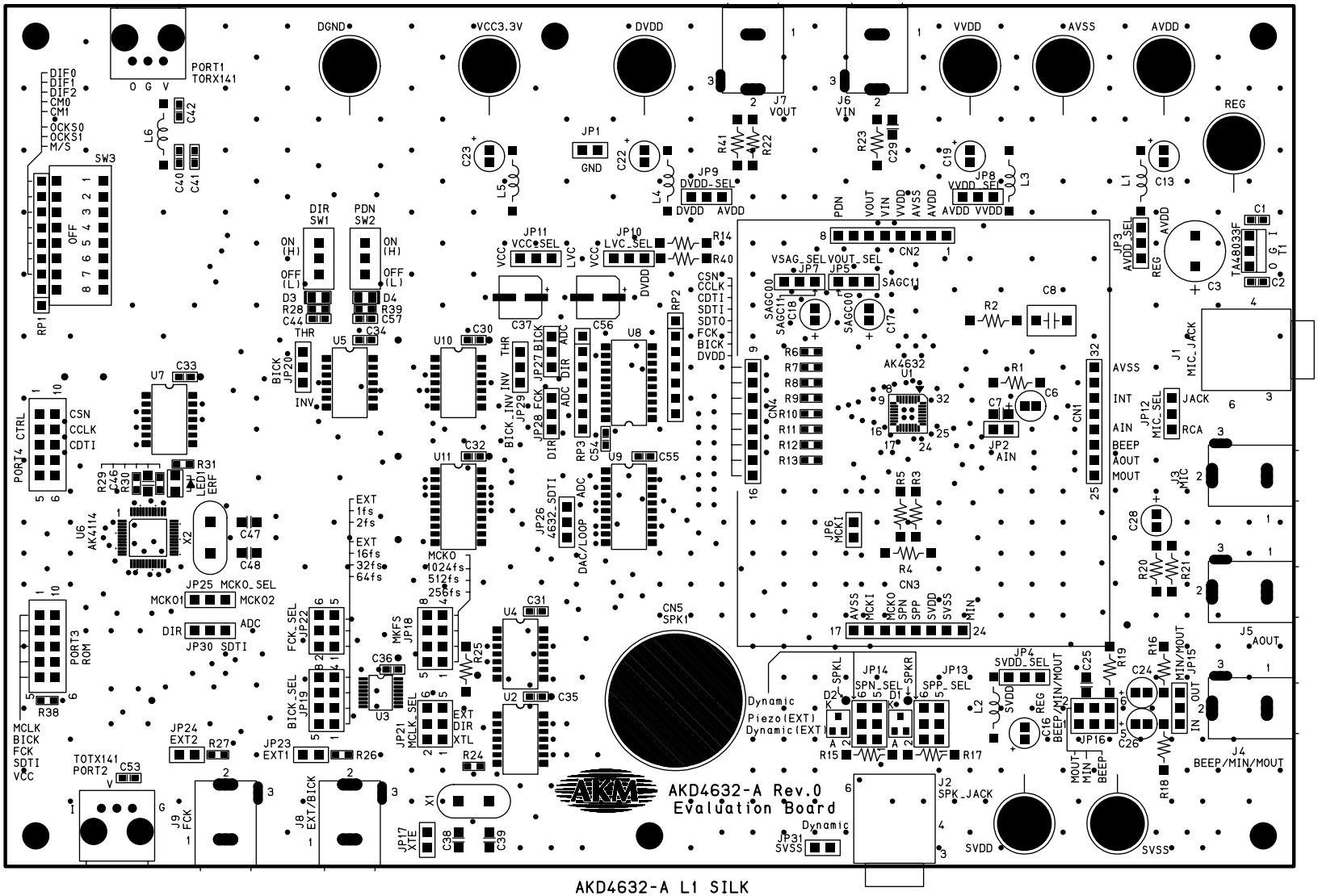
AKD4634EN-ASUB 32QFN L1 SILK

AKD6376EN-ASUB 32GFN L2 SILK

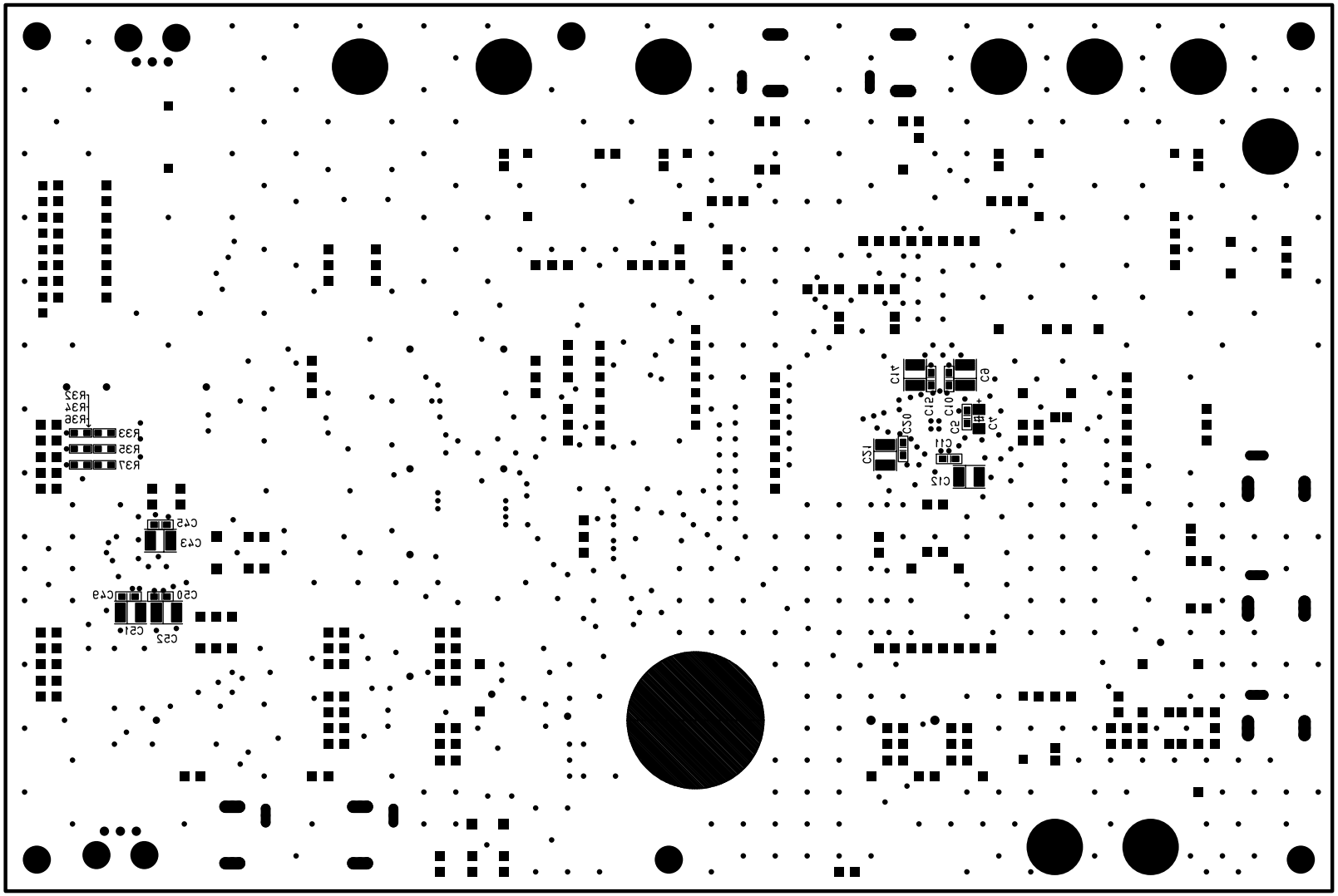


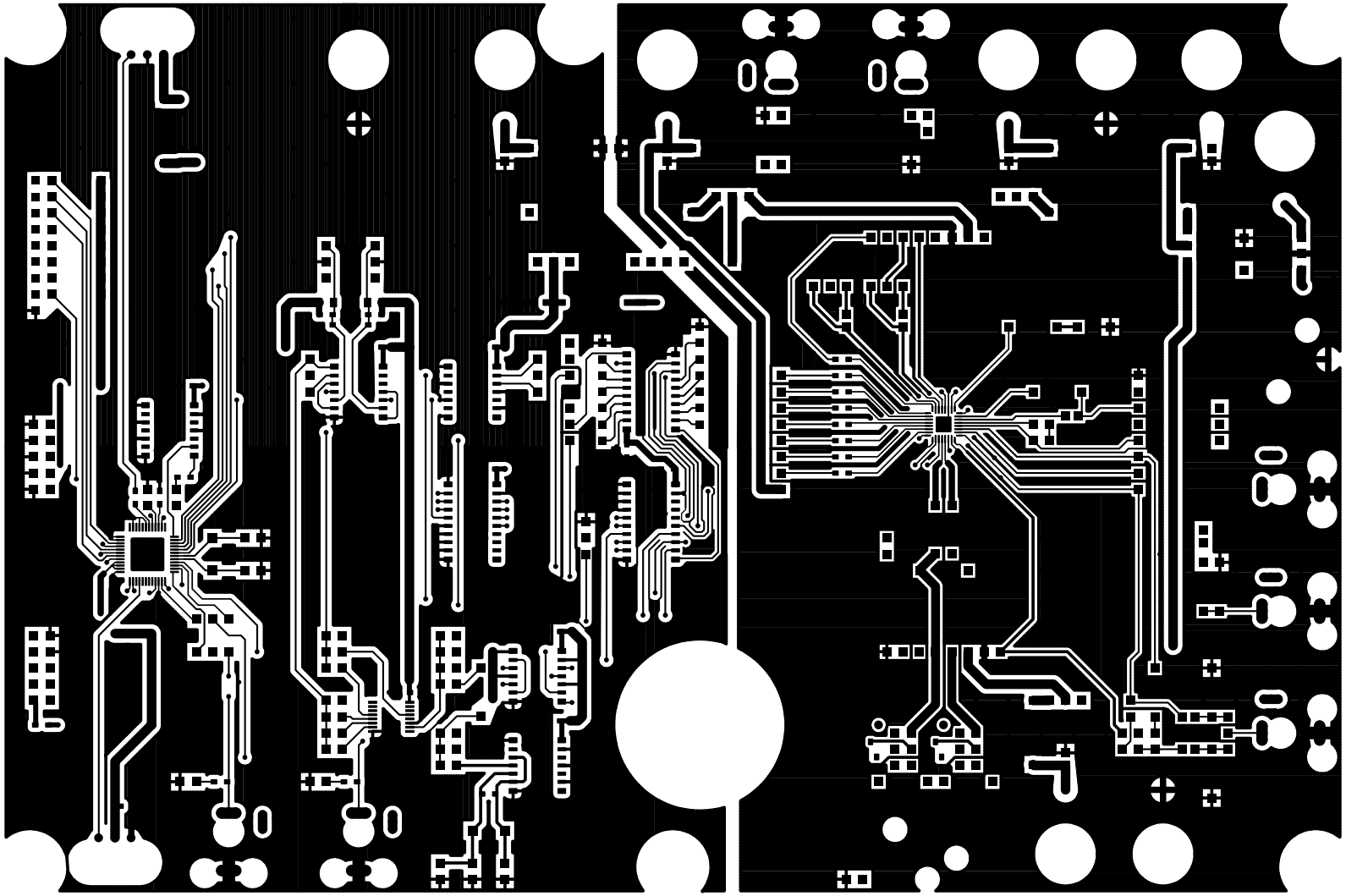
AKD4634EN-ASUB 32QFN L1

AKD4634EN-ASUB 320FN LZ



AKD4632-A L1 SILK


AKD4632-A L2 SILK



AKD4632-A L1

AKD4632-A L2