# AKD4954A-B

## Evaluation board Rev.0 for AK4954A

## GENERAL DESCRIPTION

The AKD4954A-B is an evaluation board for the AK4954A 32bit CODEC with built-in PLL and MIC/HP/SPK Amplifier. On-board USB port enables a GUI on Windows to control various settings. The AKD4954A-B has the interface with AKM's A/D evaluation boards. Therefore, it's easy to evaluate the AK4954A. The AKD4954A-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

### ■ Ordering Guide

AKD4954A-B --- Evaluation board for AK4954A
(Cable for connecting with USB port and control software are included in this package. This control software does not operate on Windows NT.)

## FUNCTION

- **Compatible with 2 types of interface**
  - **Direct interface with AKM's A/D converter evaluation boards**
  - **DIT/DIR with optical input/output**
- **USB port for board control**

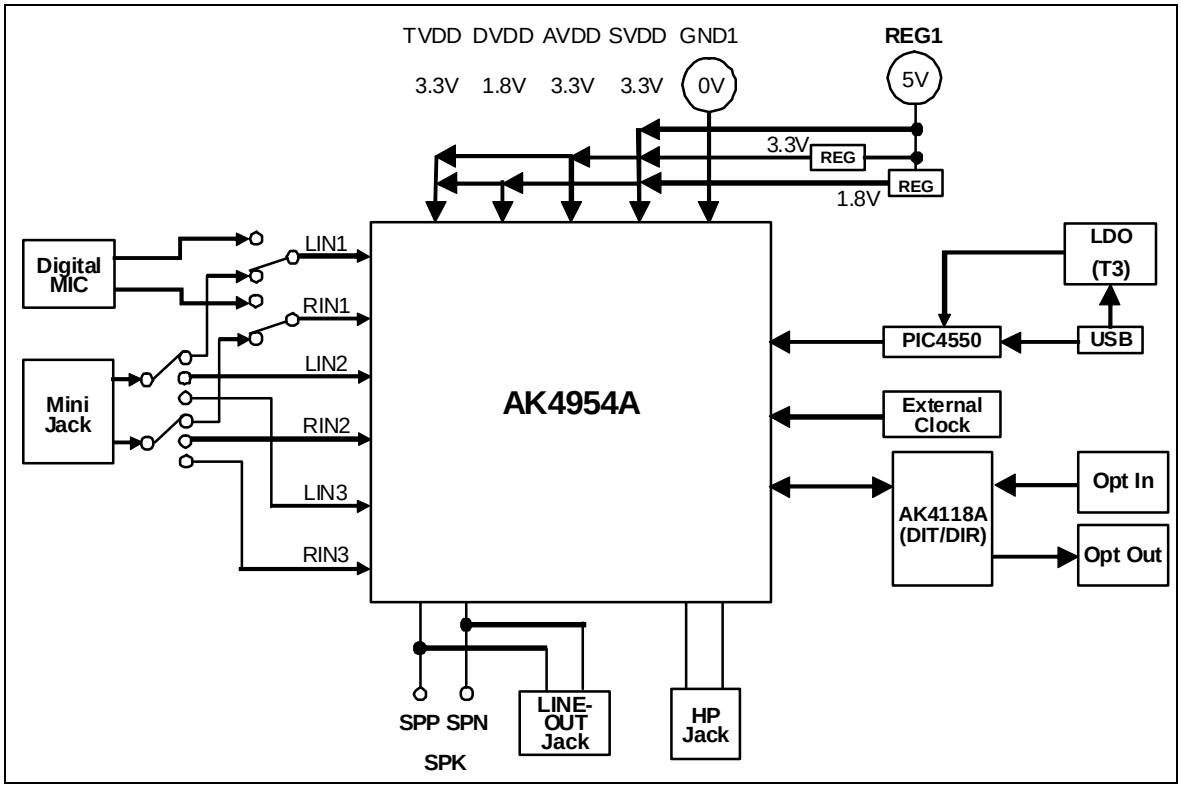


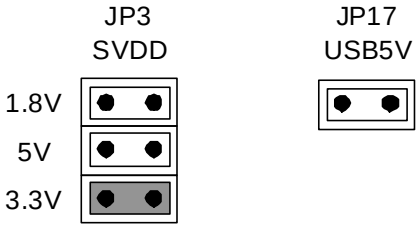

Figure 1. AKD4954A-B Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

## ■ Operation Sequence

(1) Set up the power supply lines.

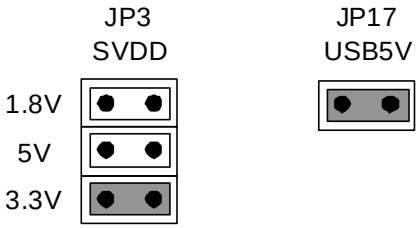
(1-1) In case of supplying the power from regulator. <Default>




| Name of Jack | Color | Default Setting | Using |
|---|---|---|---|
| REG1 | red | 5V | for regulator input |
| GND1 | black | 0V | ground |

Table 1. Set up of power supply lines

(1-2) In case of using the power supply connectors.




(2) Set up the evaluation mode, jumper pins and DIP switch. (See the followings.)

(3) Power on.

The AK4954A and AK4118A must be reset after the power supplies are applied.
The AK4954A and AK4118A should be reset once by bringing SW1 (PDN) “L” upon power-up. Click the Dummy Command button on the control software after releasing the reset by SW1= “H”.

## ■ Evaluation mode

In case of using the AK4118A when evaluating the AK4954A, audio interface format of both devices must be matched.
Reter to the datasheet for audio interface format of the AK4954A, and Table 2 for audio interface format of the AK4118A.
The AK4118A operates at fs of 32kHz or more. If the fs is slower than 32kHz, please use other mode.
In addition, MCLK of AK4118A supports 256fs and 512fs. When evaluating in a condition except above, please use other mode.
Refer to the datasheet for register setting of the AK4954A.

Applicable Evaluation Mode

(1) A/D Evaluation using the AK4118A (DIT).
  (1-1) Setting in External Slave Mode

(2) D/A Evaluation using the AK4118A (DIR). <Default>
  (2-1) Setting in External Slave Mode

(3) Evaluation of A/D or D/A using the external clock.
  (3-1) Setting in PLL Master Mode
  (3-2) Setting in PLL Slave Mode
  (3-3) Setting in External Slave Mode

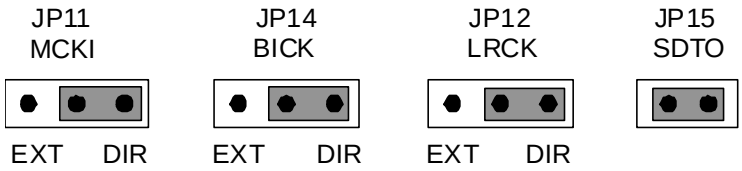
(4) Evaluation of Loop-back.
  (4-1) Setting in PLL Master Mode
  (4-2) Setting in PLL Slave Mode
  (4-3) Setting in External Slave Mode

### (1) A/D Evaluation using the AK4118A (DIT)

#### (1-1) Setting in External Slave Mode

X1 (X'tal: 11.2896MHz) and PORT2 (DIT) are used. Do not connect anything to PORT1 (DIR).
Registers of the AK4954A should be set to "EXT Slave Mode". MCKI, BICK and LRCK are supplied from the AK4118A, and SDTO of the AK4954A is output to the AK4118A.

The jumper pins should be set as follows.

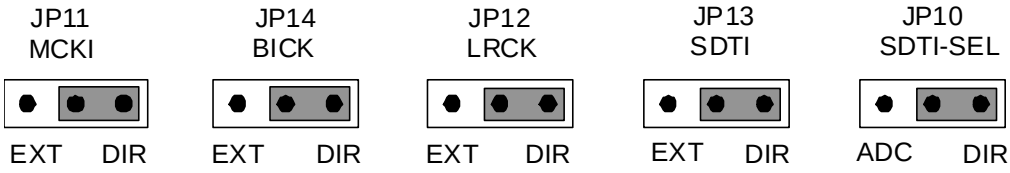



### (2) Evaluation of D/A using DIR of AK4118A. <Default>

#### (2-1) Setting in External Slave Mode

PORT1 (DIR) is used. Do not connect anything to PORT2 (DIT).
Registers of the AK4954A should be set to "EXT Slave Mode".

The jumper pins should be set as follows.



### (3) A/D or D/A Evaluation using the external clock.

External clocks are used. Do not connect anything to PORT1 (DIR) and PORT2 (DIT).

#### (3-1) Setting in PLL Master Mode

The master clock is input from the MCKI pin of JP11. An internal PLL circuit generates BICK and LRCK. Registers of the AK4954A should be set to "PLL Master Mode".

BICK, LRCK SDTI and SDTO are input into and output from JP14, JP12, JP13 and JP15.

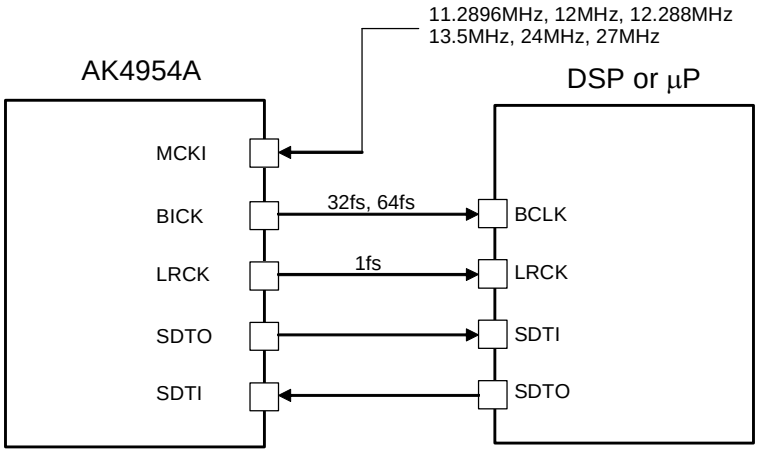



Figure 2. PLL Master Mode

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### (3-2) Setting in PLL Slave Mode

A reference clock of PLL is selected among the input clocks that are supplied to the BICK pin. The required clock to operate the AK4954A is generated by an internal PLL circuit.
Registers of the AK4954A should be set to "PLL Slave Mode" (Reference Clock = BICK).

BICK, LRCK SDTI and SDTO are input into and output from JP14, JP12, JP13 and JP15.

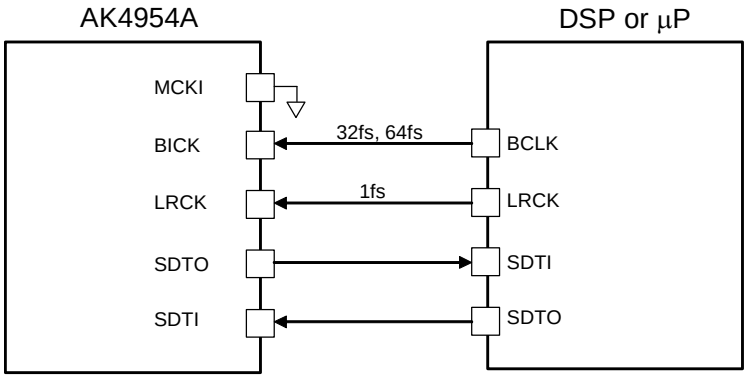
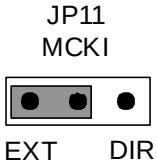


Figure 3. PLL Slave Mode 2(PLL Reference Clock: BICK pin)

The jumper pins should be set as follows.



### (3-3) Setting in External Slave Mode

Registers of the AK4954A should be set to “EXT Slave Mode”.

MCLK, BICK, LRCK SDTI and SDTO are input into and output from JP11, JP14, JP12, JP13 and JP15.

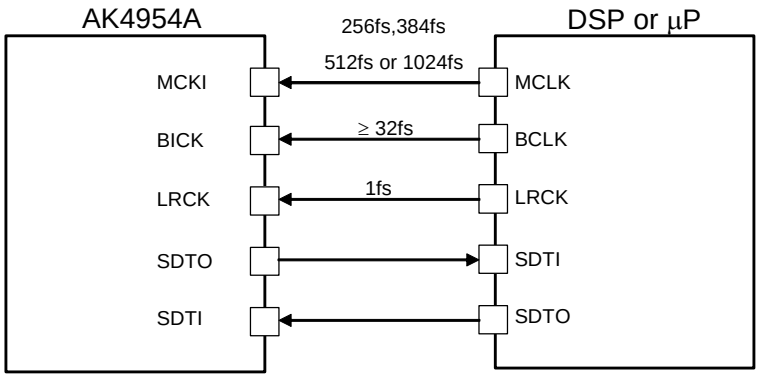



Figure 4. EXT Slave Mode

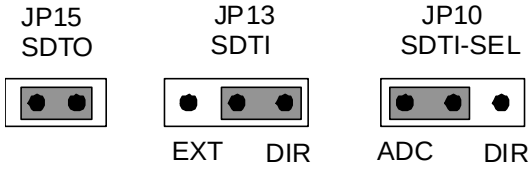
## (4) Evaluation in Loop-back Mode.

### (4-1) Setting in PLL Master Mode

Do not connect anything to PORT1 (DIR), PORT2 (DIT).
Registers of the AK4954A should be set to “PLL Master Mode”.

(4-1-1) In case of supplying MCLK to JP11

The jumper pins should be set as follows.

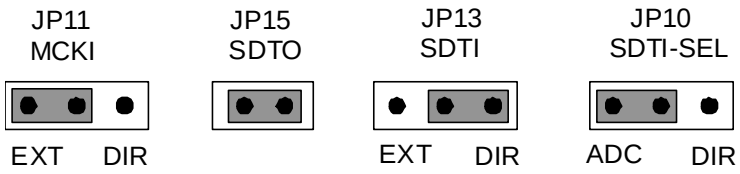


### (4-2) Setting in PLL Slave Mode

Registers of the AK4954A should be set to “PLL Slave Mode” (Reference Clock: BICK).
Do not connect anything to PORT1 (DIR) and PORT2 (DIT).

(4-2-1) In case of supplying BICK and LRCK from the external clock

The jumper pins should be set as follows.



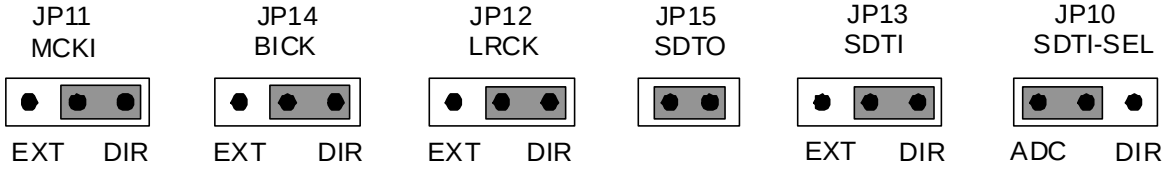

### (4-3) Setting in External Slave Mode

Registers of the AK4954A should be set to “EXT Slave Mode”.
Do not connect anything to PORT1 (DIR), PORT2 (DIT).

(4-3-1) In case of using clocks from AK4118A

Use X1 (11.2896MHz).

The jumper pins should be set as follows.



## ■ DIP Switch Setting

[S1] (SW DIP-4): Mode setting of the AK4118A.

| No. | Name | ON ("H") | OFF ("L") | Default |
|---|---|---|---|---|
| 1 | OCKS1 | AK4118A Master Clock Setting : See Table 4 | | L |
| 2 | DIF0 | AK4118A Audio Format Setting<br>See Table 3 | | L |
| 3 | DIF1 | | | L |
| 4 | DIF2 | | | H |

Table 2. Mode Setting of the AK4118A

| Mode | DIF2 | DIF1 | DIF0 | DAUX | SDTO | LRCK | | BICK | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | I/O | | I/O | |
| 0 | 0 | 0 | 0 | 24bit, Left justified | 16bit, Right justified | H/L | O | 64fs | O | |
| 1 | 0 | 0 | 1 | 24bit, Left justified | 18bit, Right justified | H/L | O | 64fs | O | |
| 2 | 0 | 1 | 0 | 24bit, Left justified | 20bit, Right justified | H/L | O | 64fs | O | |
| 3 | 0 | 1 | 1 | 24bit, Left justified | 24bit, Right justified | H/L | O | 64fs | O | |
| 4 | 1 | 0 | 0 | 24bit, Left justified | 24bit, Left justified | H/L | O | 64fs | O | Default |
| 5 | 1 | 0 | 1 | 24bit, $I^2S$ | 24bit, $I^2S$ | L/H | O | 64fs | O | |
| 6 | 1 | 1 | 0 | 24bit, Left justified | 24bit, Left justified | H/L | I | 64 -128fs | I | |
| 7 | 1 | 1 | 1 | 24bit, $I^2S$ | 24bit, $I^2S$ | L/H | I | 64 -128fs | I | |

Table 3. AK4118A Audio Interface Format Setting

| OCKS1 | MCKO1 | X'tal | |
|---|---|---|---|
| 0 | 256fs | 256fs | Default |
| 1 | 512fs | 512fs | |

Table 4. AK4118A Master Clock Setting

## ■ Toggle SW Function

*Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Power downs AK4954A and AK4118A. Keep "H" during normal operation.

## ■ Control Port

It is possible to control AKD4954A-B via general USB port. Connect cable with the USB connection(PORT3) on the board and PC.

## ■ Analog Input/Output Circuits

(1) Input Circuits

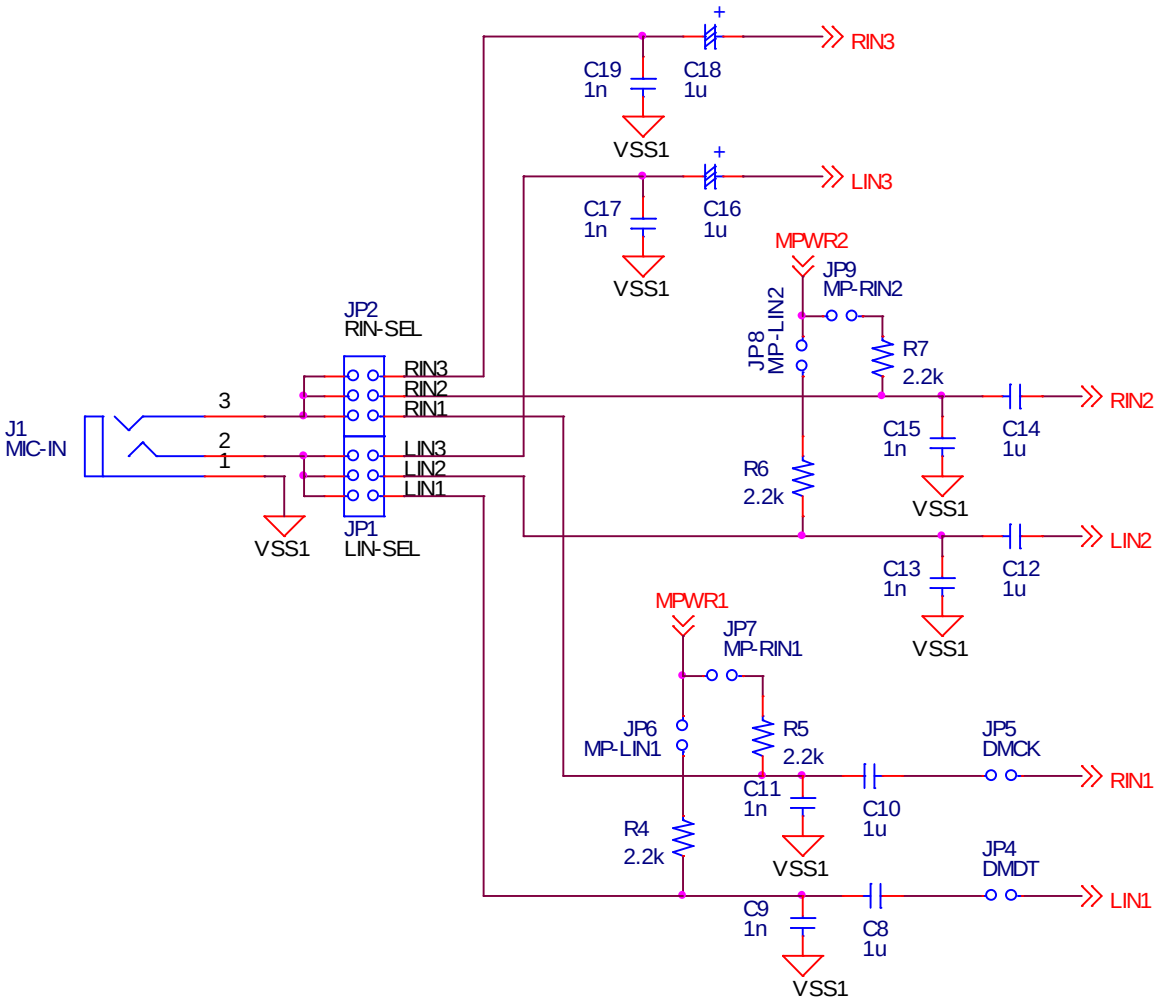
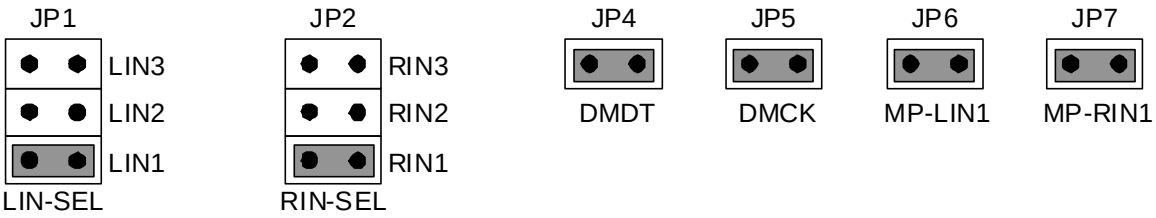



Figure 5. LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 Input Circuits

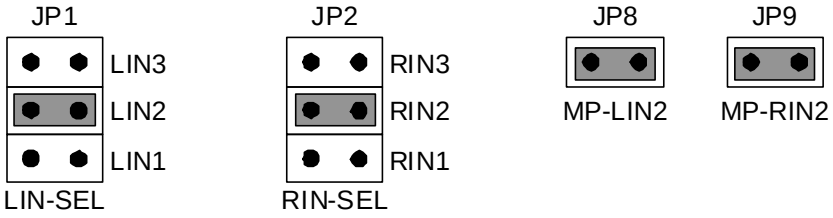
(1-1) LIN1/RIN1Input Circuit <Default>

LIN1 and RIN1are input to J1.
When the Mic Power is not used, JP6 and JP7 should be set to open.



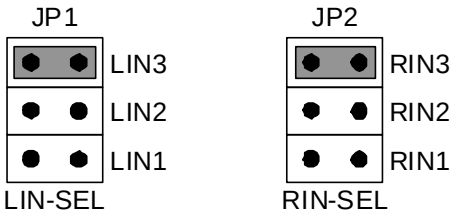
(1-2) LIN2/RIN2 Input Circuit <Default>

LIN2 and RIN2 are input to J2 and J3.
When the Mic Power is not used, JP8 and JP9 should be set to open.



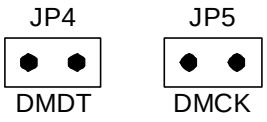

(1-3) LIN3/RIN3 Input Circuit

LIN3 and RIN3 are input to J2 and J3.




(1-4) Digital Mic Input Circuit

DMCK is output from JP5 and DMDT is input to JP4.



(2) Output Circuits

(2-1) HPL/HPR Output Circuit

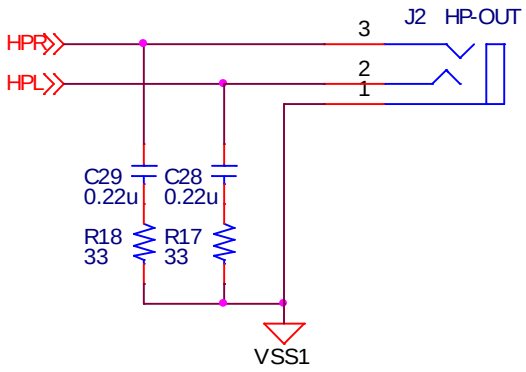



Figure 6. HPL/HPR Output Circuit

HPL and HPR are output from J2

(2-2) SPP/SPN Output Circuit

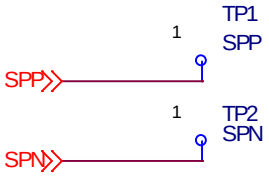
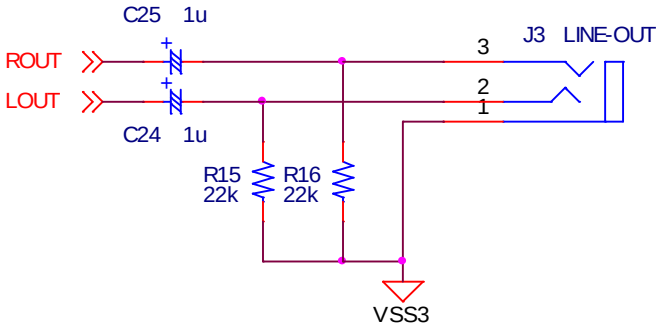



Figure 7. SPP/SPN Output Circuit

SPP and SPN are output from TP1 and TP2.

(2-3) Stereo Line Output Circuit




.Figure 8. LOUT/ROUT Output Circuit

LOUT and ROUT are output from J3.

* AKM assumes no responsibility for the trouble when using the above circuit examples.

# AK4954A Control Software Manual

## ■ Evaluation Board and Control Software Settings

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect cable with the USB connection on the board and PC.
3. The USB I/F board is recognized as HID (Human Interface Device) on PC. It is not necessary to install a new driver.
4. Start up the control program.(Note 1)

Note 1. After power up the evaluation board, put SW1 to "L" to power down the AK4954A and the AK4118A, and return them to "H" to release the power-down state. Then, an initialization must be executed by pressing the Dummy Command button.

5. Begin evaluation by following the procedure below.

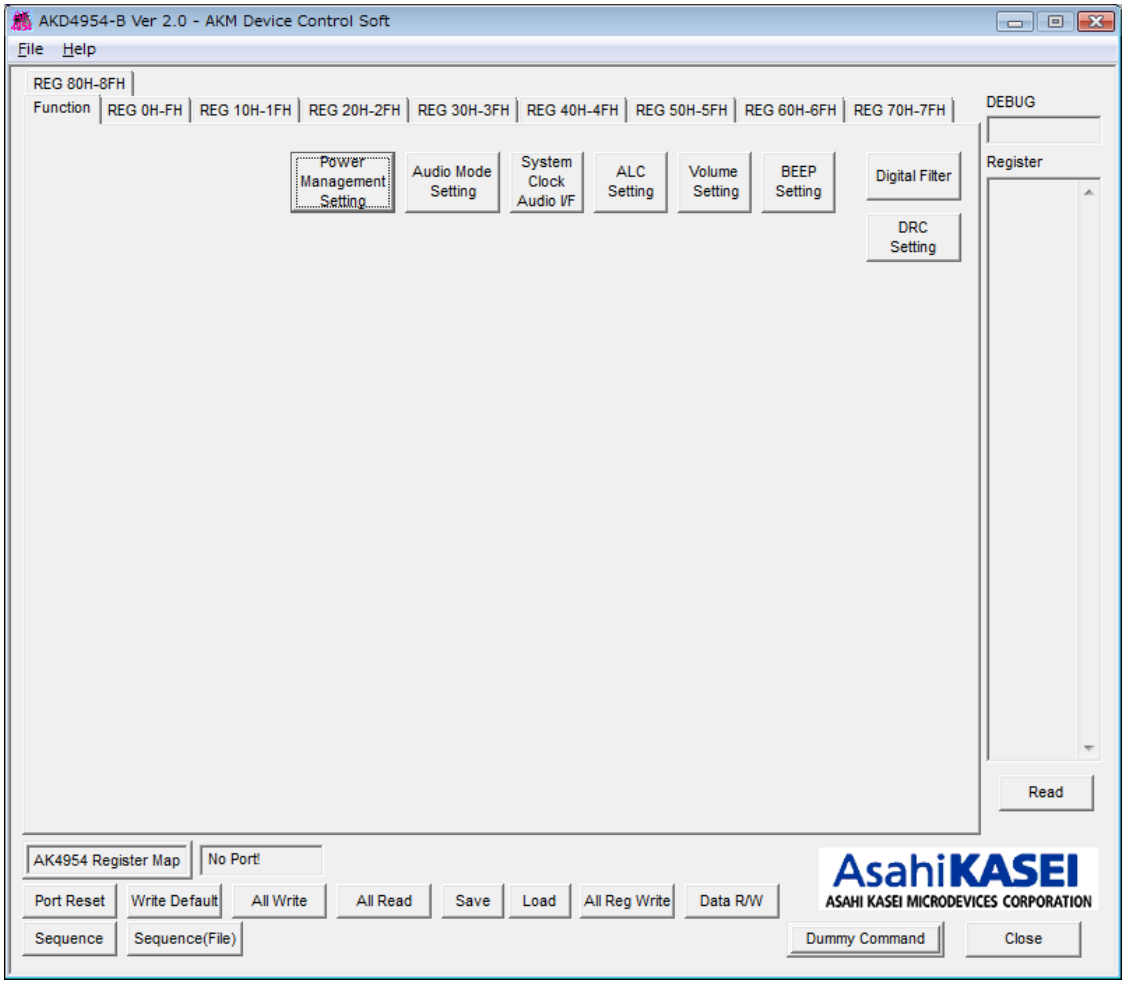



Figure 9. Window of Control Soft

## ■ Operation Overview

Function, register map and testing tool are controlled by this control software. These controls may be selected by the upper tabs.

Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” section for details of each dialog box setting.

1. [Port Reset]: Click this button after the control soft starts up.

2. [Write Default]: Initializes Registers
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executes write command for all registers displayed.

4. [All Read]: Executes read command for all registers displayed.

5. [Save]: Saves current register settings to a file.

6. [Load]: Executes data write from a saved file.

7. [All Req Write]: Opens “All Req Write” dialog box.

8. [Data R/W]: Opens “Data R/W” dialog box

9. [Sequence]: Opens “Sequence” dialog box.

10. [Sequence (File)]: Opens “Sequence(File)” dialog box.

11. [Read]: Reads current register settings and displays on to the register area (on the right of the main window). This is different from [All Read] button as it does not reflect to the register map. It only displays register values in hexadecimal numbers.

12. [Dummy Command]: The dummy command is written (Note 2).

Note 2. After power up the evaluation board, put SW1 to “L” to power down the AK4954A and the AK4118A, and return them to “H” to release the power-down state. Then, an initialization must be executed by pressing the Dummy Command button.

## ■ Tab Functions (Note 3)

### 1. [Function]: Function control

The dialog box setting is open when click the each button
Each operation is executed by [Function] buttons on the left side of the screen. (Refer to the "■ Dialog Box" for details of each dialog box setting.)

Note 3. After power up the evaluation board, put SW1 to "L" to power down the AK4954A and the AK4118A, and return them to "H" to release the power-down state. Then, an initialization must be executed by pressing the Dummy Command button.

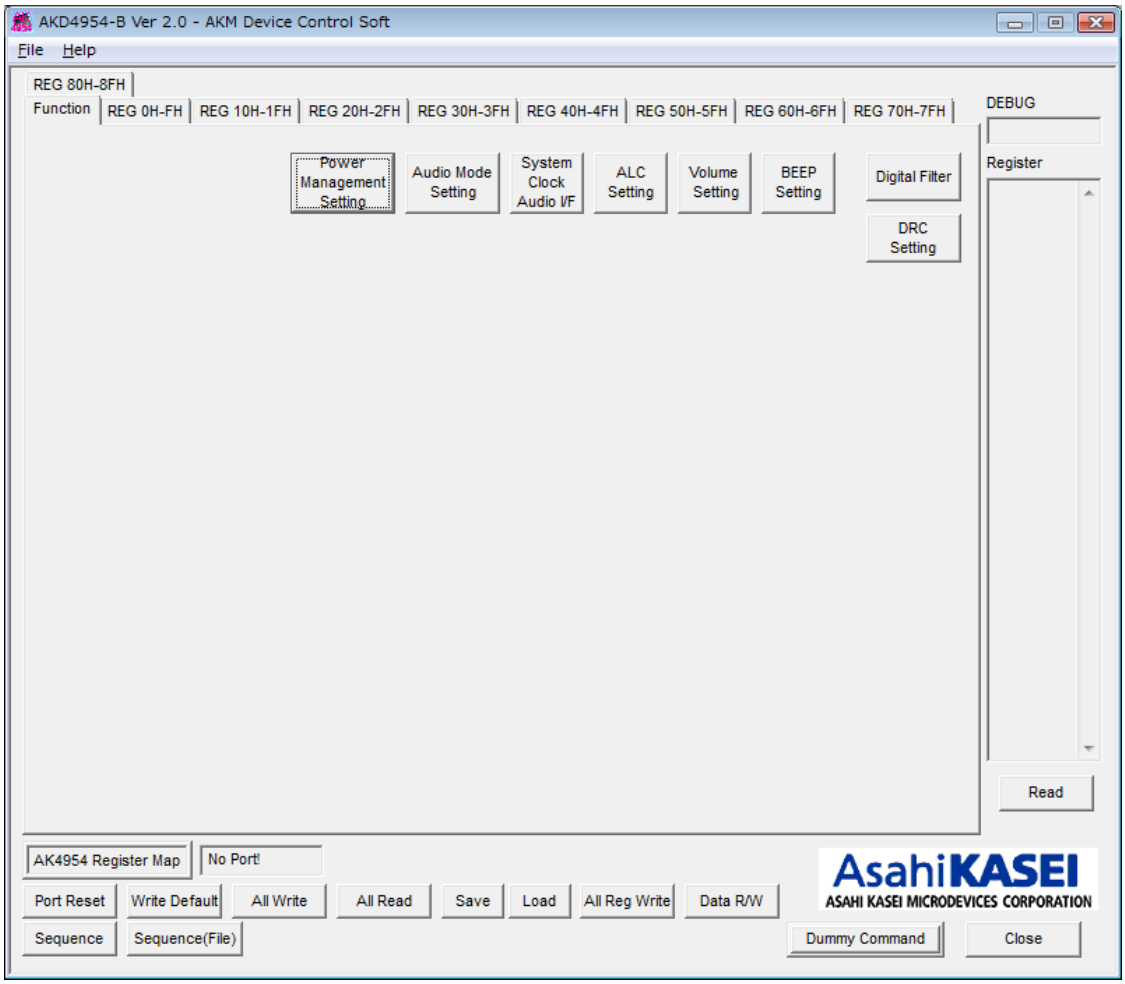



Figure 10. [Function] Window

[Power Management Setting] : Open [Power Management Setting] dialog.
[Audio Mode Setting] : Open [Audio Mode Setting] dialog.
[System Clock Audio I/F] : Open [System Clock Audio I/F] dialog.
[ALC Setting] : Open [ALC Setting] dialog.
[Volume Setting] : Open [Volume Setting] dialog.
[Beep Setting] : Open [Beep Setting] dialog.
[Digital Filter] : Open [Filter Setting] dialog.
[DRC Setting] : Open [DRC Function] dialog.

## 2. [REG]: Register Map

This tab is for a register write and read.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is shown in red (when read-only, the name is shown in dark red).
Button Up indicates “L” or “0” and the bit name is shown in blue (when read-only, the name is shown in gray).

Grayed-out registers are Read-only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

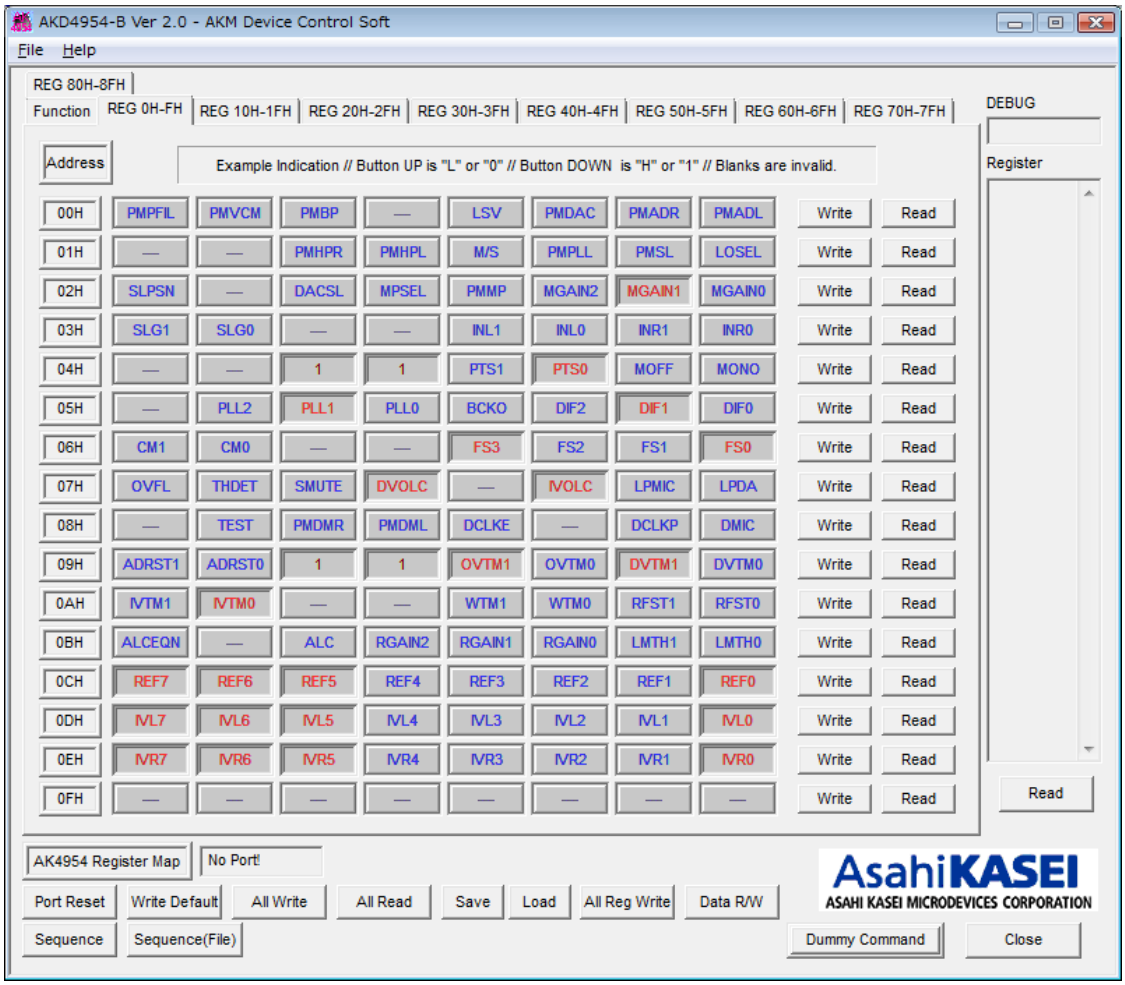



Figure 11. [REG] Window

### 2-1. [Write]: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing tow or more bits on the same address simultaneously. Click the [Write] button for the register pop-up dialog box shown below. When the checkbox next to the register name is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write setting values to the registers, or click [Cancel] to cancel this setting.

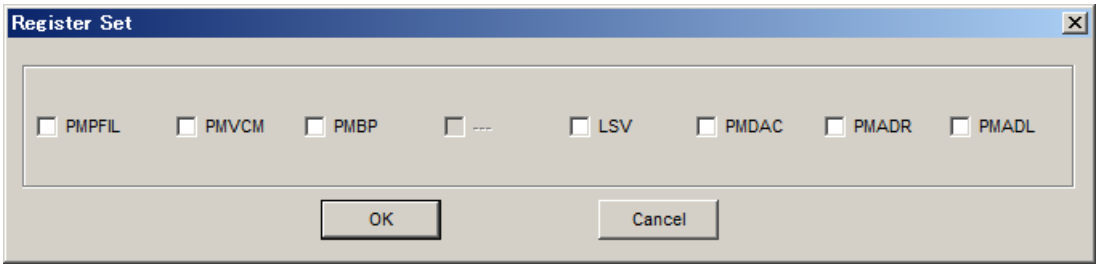



Figure 12. [Register Set] Window

### 2-2. [Read]: Data Read

Click the [Read] button located on the right of the each corresponding address to execute a register read.
The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.
Button Down indicates “1” and the bit name is shown in red (when read-only, the name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read-only, the name is shown in gray).
Please be aware that button statuses will be changed by a Read command.

## ■ Dialog Box

### 1. [All Req Write]: All Reg Write dialog box

Click the [All Reg Write] button in the main window to open register setting file window shown below. Register setting files saved by the [SAVE] button may be applied.

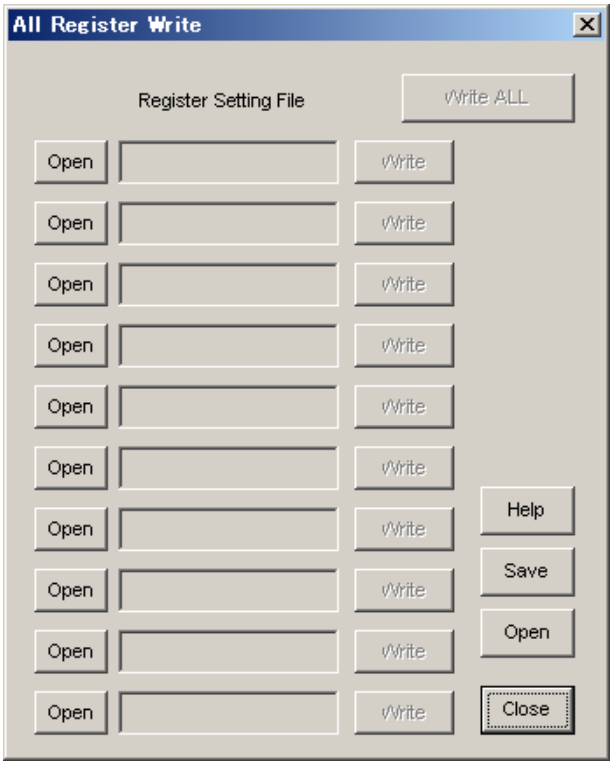



Figure 13. [All Reg Write] Window

[Open (left)] : Selects a register setting file (*.akr).
[Write] : Executes register write with selected setting file.
[Write All] : Executes register write with all selected setting files.
Selected files are executed in descending order.

[Help] : Opens a help window.
[Save] : Saves a register setting file assignment. File name is “*.mar”.
[Open (right)]: Opens a saved register setting file assignment “*. mar”.
[Close] : Closes the dialog box and finish process.

### ~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

## 2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data is written to the specified address.

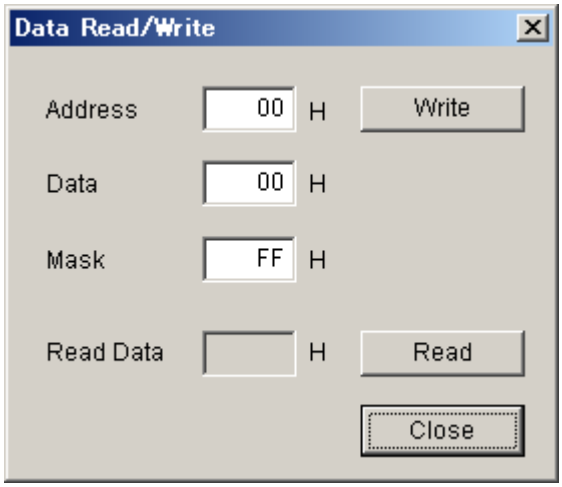



Figure 14. [Data R/W] Window

[Address] Box : Input data write address in hexadecimal numbers.
[Data] Box : Input write data in hexadecimal numbers.
[Mask] Box : Input masks data in hexadecimal numbers.
This value "ANDed" with the write data becomes the input data.
[Write] : Writes the data generated from Data and Mask value is written to the address specified in "Address" box (Note 4).
[Read] : Reads data from the address specified in "Address" box (Note 4).
The result will be shown in the Read Data Box in hexadecimal numbers.
[Close] : Closes the dialog box and finishes process.
Data write will not be executed unless the [Write] button is clicked.

Note 4. The register map will be updated after executing the [Write] or [Read] command.

### 3. [Sequence]: Sequence Dialog Box

Click the [Sequence] button to open register sequence setting dialog box.
Register sequence may be set in this dialog box.

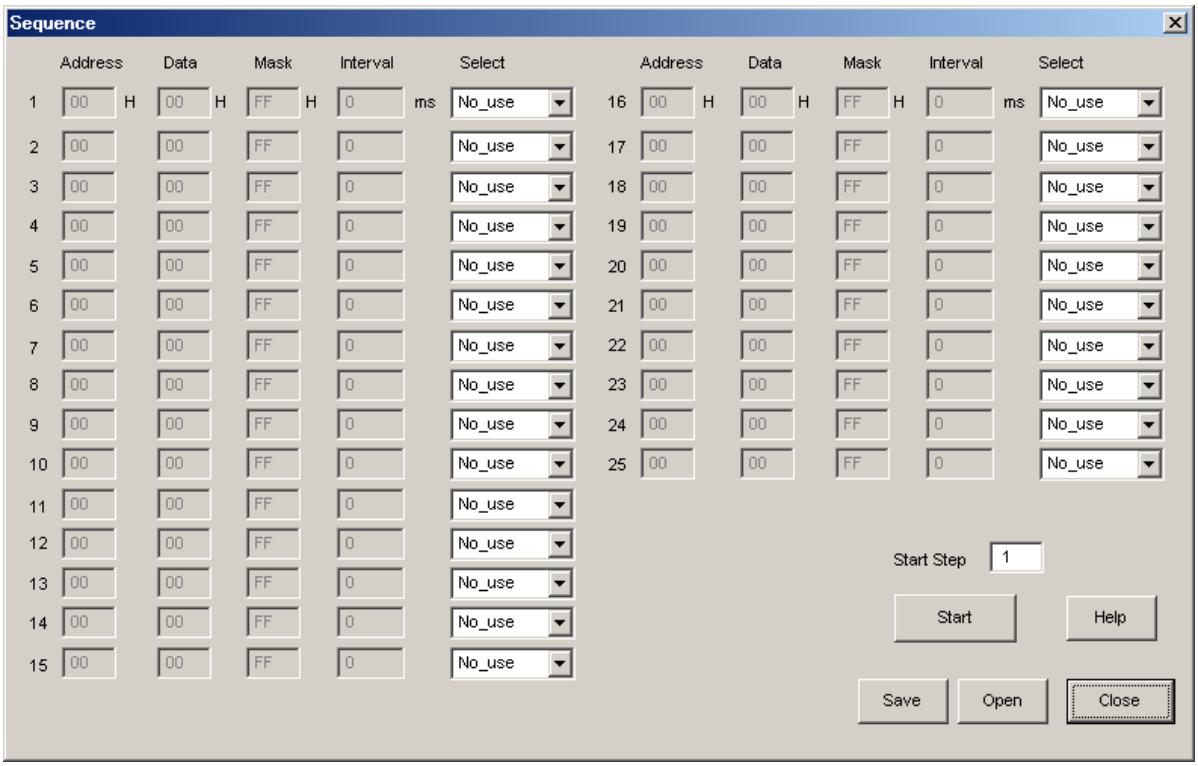



Figure 15. [Sequence] Window

### ~ Sequence Setting ~

Set register sequence according to the following process bellow.

1. Select a command
   Use [Select] pull-down box to choose commands.
   Corresponding boxes will be valid.

   < Select Pull-down menu >
   - No_use : Not using this address
   - Register : Register write
   - Reg(Mask) : Register write (Masked)
   - Interval : Takes an interval
   - Stop : Pauses the sequence
   - End : Ends the sequence

2. Input sequence
   [Address] : Data address
   [Data] : Write data
   [Mask] : Mask
   The value in the [Data] box is ANDed with the value in the [Mask] box. This data becomes the actual input data.
   When Mask = 0x00, current setting is hold.
   When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
   When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
   Upper 4bit is hold to current setting.
   [Interval] : Interval time

   Valid boxes for each process command are shown bellow.

   · No_use : None
   · Register : [Address], [Data], [Interval]
   · Reg(Mask) : [Address], [Data], [Mask], [Interval]
   · Interval : [Interval]
   · Stop : None
   · End : None

### ~ Control Buttons~

Functions of Control Buttons are shown bellow.

[Start] Button : Executes the sequence
[Help] Button : Opens a help window
[Save] Button : Saves sequence settings as a file. The file name is “*.aks”.
[Open] Button: Opens a sequence setting file “*.aks”.
[Close] Button: Closes the dialog box and finishes the process.

### ~ Stop of the sequence~

When “Stop” is selected in the sequence, the process is paused. It starts again when the [Start] button is clicked Restart step number is shown in the “Start Step” box. When executing the process until the end of sequence, the “Start Step” value will return to “1”.

The sequence can be started from any step by writing a step number to the “Start Step” box.
Write “1” to the “Start Step” box and click [Start] button, when restarting the process from the beginning.

### 4. [Sequence(File)]: Sequence Setting File Dialog Box

Click the [Sequence(File)] button to open sequence setting file dialog box shown below.
Files saved in the “Sequence setting dialog” can be applied in this dialog.

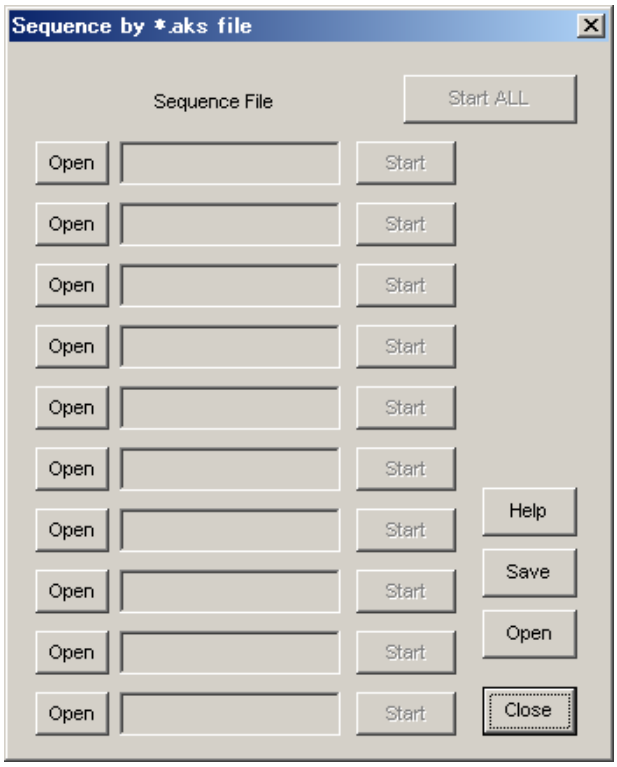



Figure 16. [Sequence(File)] Window

[Open (left)] : Select a sequence setting file (*.aks).
[Start] : Executes the sequence by the setting of selected file.
[Start All] : Executing all sequence settings.
Selected files are executed in descending order.
[Help] : Opens a help window.
[Save] : Saves a sequence setting file assignment. File name is “*.mas”.
[Open(right)] : Select a saved sequence setting file assignment “*. mas”.
[Close] : Closes the dialog box and finishes the process.

### ~ Operating Suggestions ~

1. Files saved by the [Save] button and opened by the [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” is selected in the sequence, the process will be paused and the message box shown below pops up. Click “OK” to continue the process.


Figure 17. Window of [Sequence Pause]

## 5. [Power Management Setting]: Power Management Setting Dialog Box

Click [Power Management Setting] button in the function tab to open the power management setting dialog box shown in Figure 18.
Refer to the datasheet for register settings of the AK4954A.

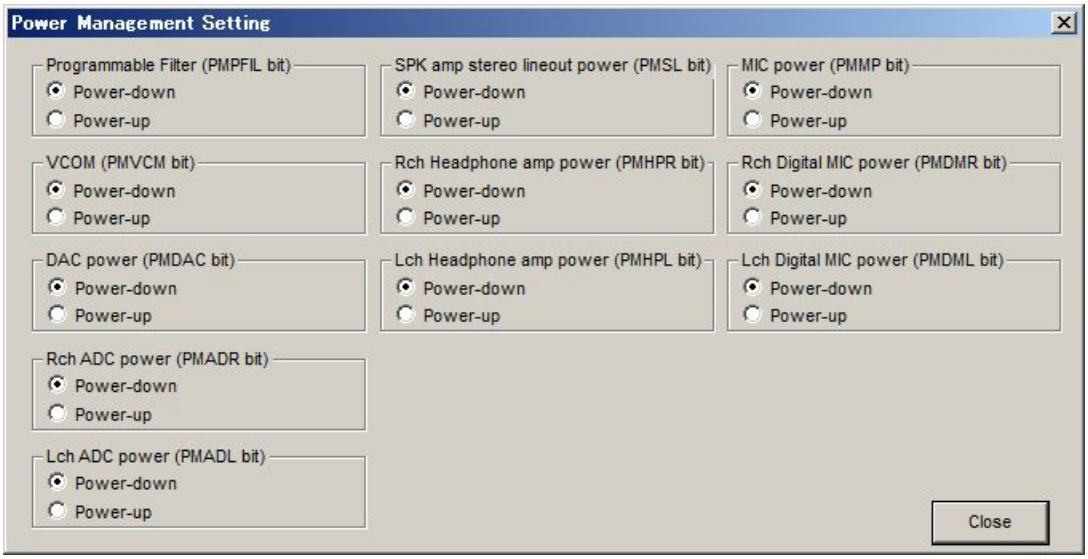



Figure 18. [Power Management Setting] Window

## 6. [Audio Mode Setting]: Audio Mode Setting Dialog Box

Click the [Audio Mode Setting] button in the function tab to open the audio mode setting dialog box shown in Figure 19.
Refer to the datasheet for register settings of the AK4954A.

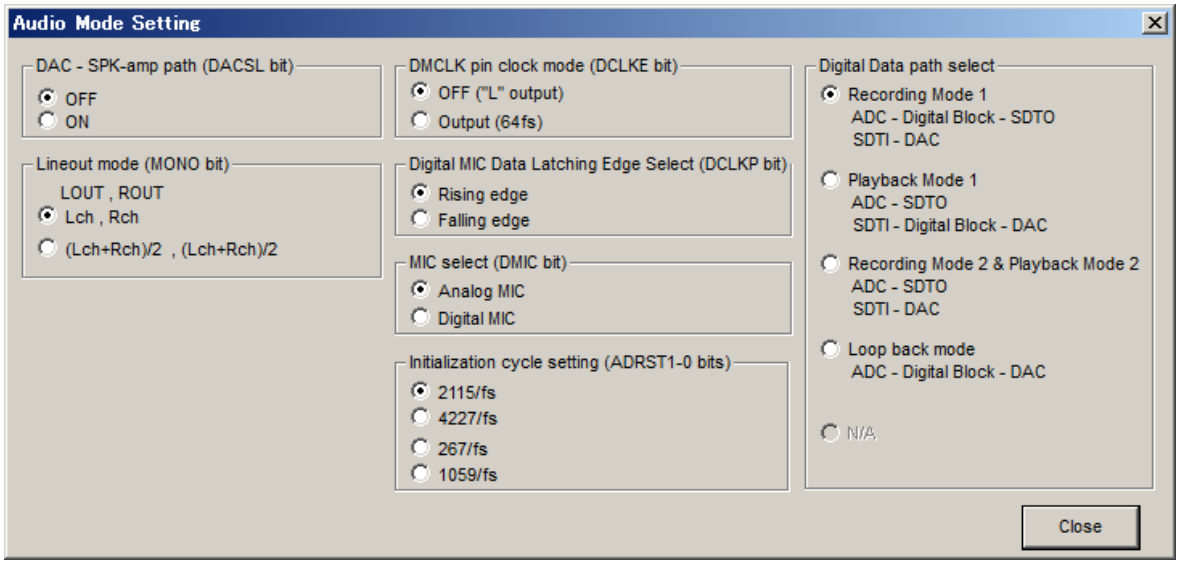



Figure 19. [Audio Mode Setting] Window

## 7. [System Clock Audio I/F]: System Clock Audio I/F Dialog Box

Click the [System Clock Audio I/F] button in the function tab to open the System Clock Audio I/F dialog box shown in Figure 20. Refer to the datasheet for register settings of the AK4954A.

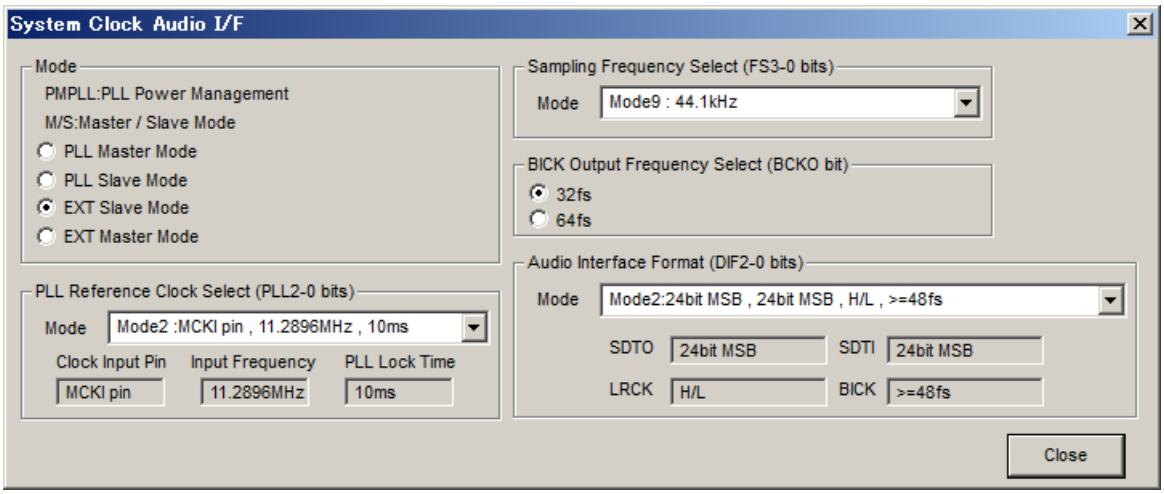



Figure 20. [System Clock Audio I/F] Window

## 8. [ALC Setting]: ALC Setting Dialog Box

Click the [ALC Setting] button in the function tab to open the ALC setting dialog box shown in Figure 21. Refer to the datasheet for register settings of the AK4954A.

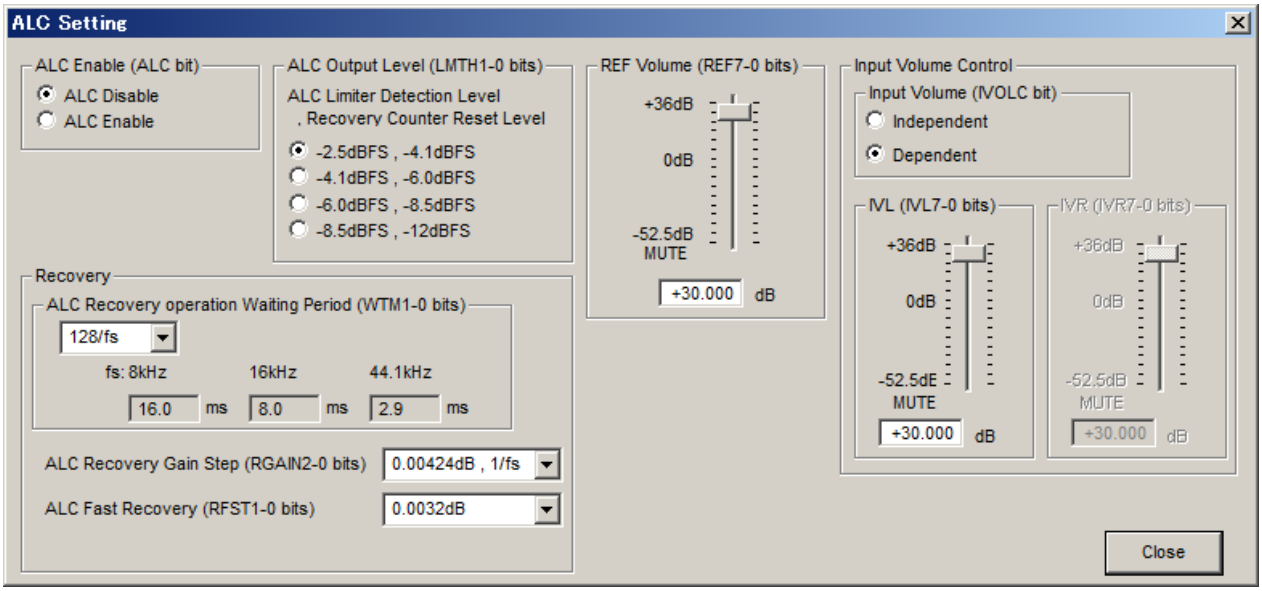



Figure 21. [ALC Setting] Window

### Volume Control by Slider Menu

The volume can also be changed by writing a value in a dialog box. The slide bar is moved to the value that is written in the dialog box. Use the mouse or arrow keys on the keyboard for fine adjustments.

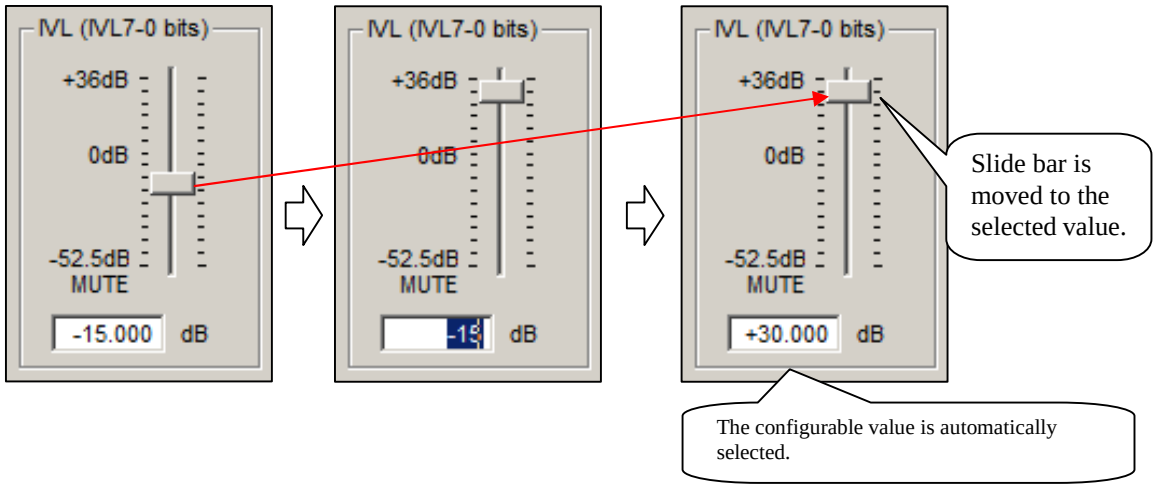



Figure 22. Volume Slider

## 9. [Volume Setting]: Volume Setting Dialog Box

Click the [Volume Setting] button in the function tab to open the volume setting dialog box shown in Figure 23. Refer to the datasheet for register settings of the AK4954A.

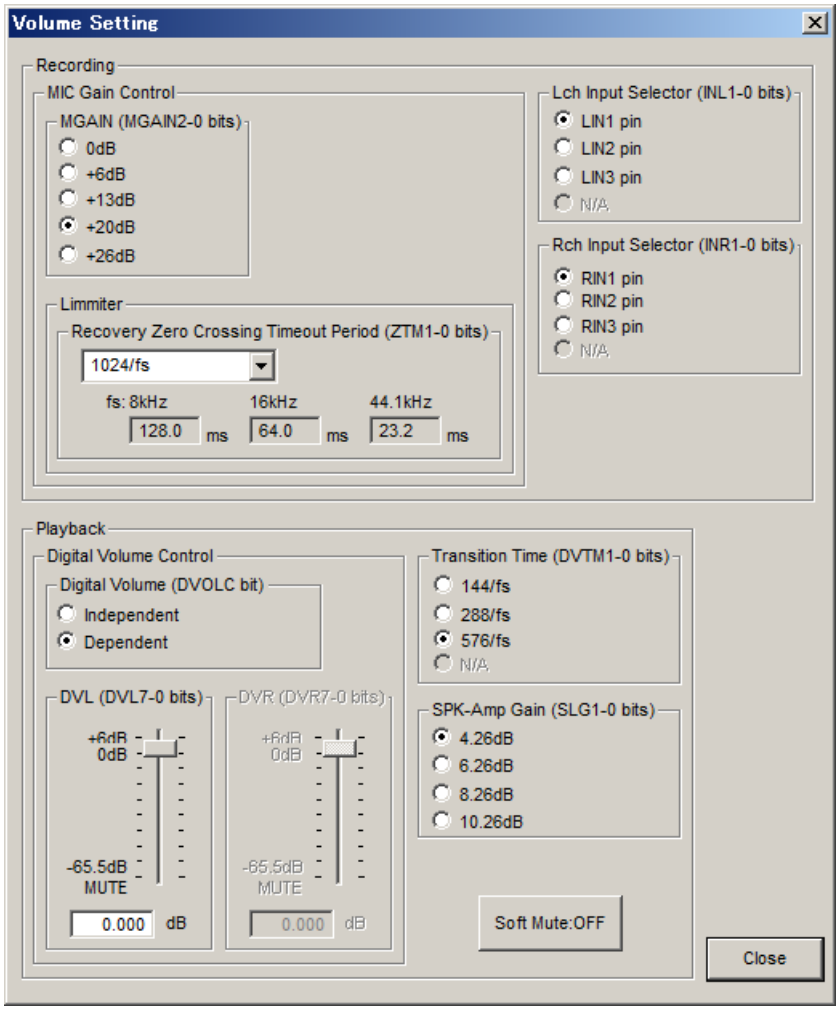



Figure 23. [Volume Setting] Window

## 10. [BEEP Setting]: BEEP Setting Dialog Box

Click the [BEEP Setting] button in the function tab to open is the Beep setting dialog box shown in Figure 24. Refer to the datasheet for register settings of the AK4954A.

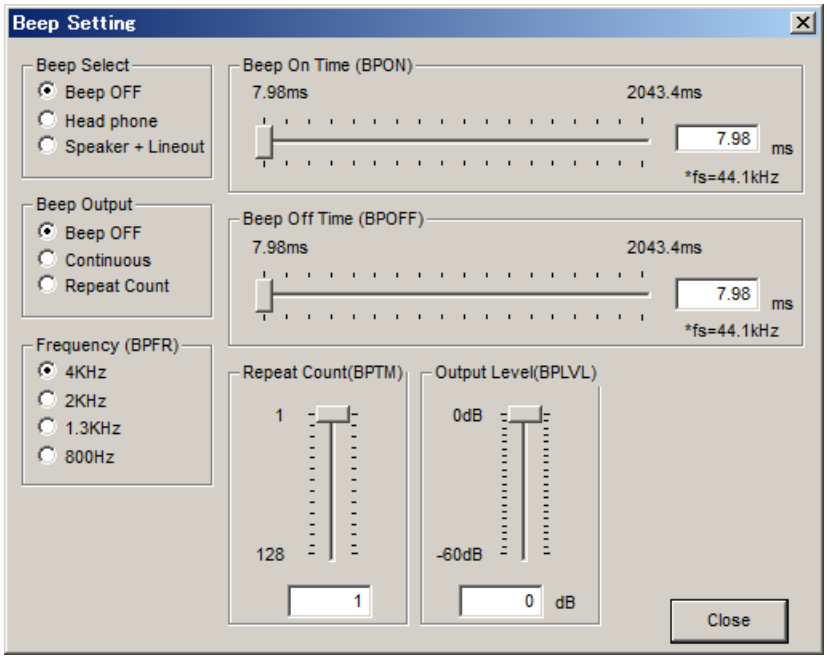



Figure 24. [BEEP Setting] Window

## 11. [Digital Filter]: Filter Setting Dialog Box

Click the [Digital Filter] button in the function tab to open the filter setting dialog box shown in Figure 25. Refer to the datasheet for register settings of the AK4954A.

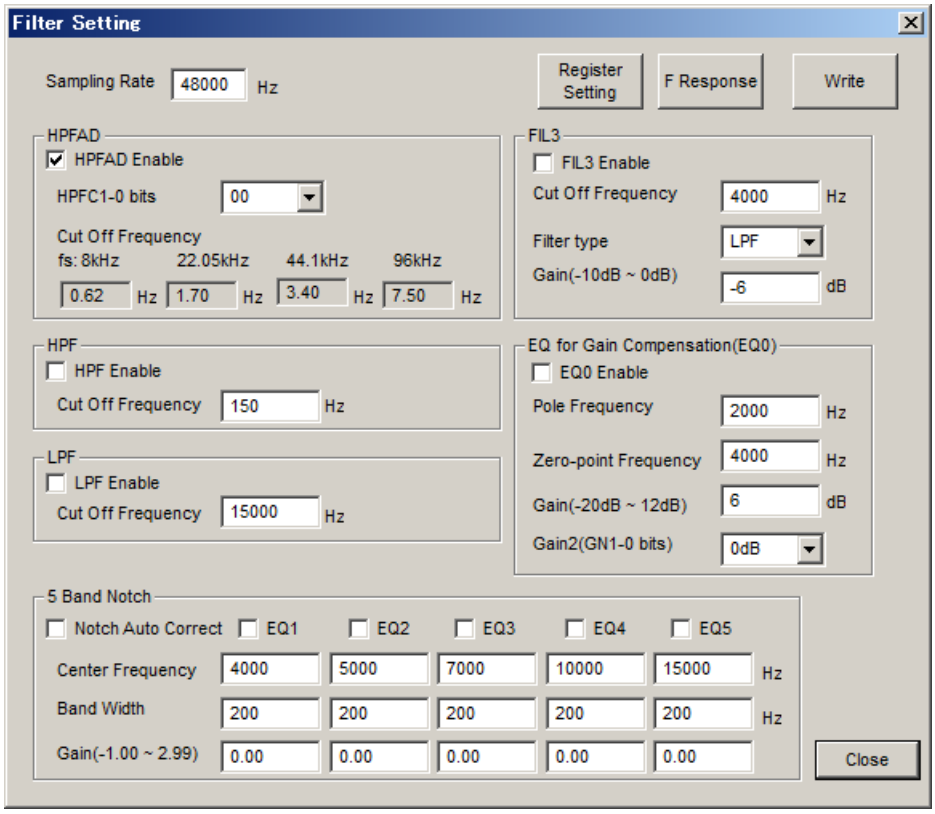



Figure 25. [Filter Setting] Window

[Register Setting] : Opens “Register Setting for Filter” dialog box.
[F Response] : Opens the filter characteristic dialog.
Executes all filter calculation, but filter coefficients are not written.
[Write] : Executes all filter calculation, and filter coefficients are written.
[Close] : Closes the dialog box and ends process.

### 11-1. Parameter Setting

(1) Please set a parameter of each Filter.

| Parameter | Function | Setting Range |
|---|---|---|
| Sampling Rate | Sampling frequency (fs) | 7350Hz ≤ fs ≤ 96000Hz |
| **HPF** | | |
| Cut Off Frequency | High pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| **LPF** | | |
| Cut Off Frequency | Low pass filter cut off frequency | fs/20 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| **FIL3** | | |
| Cut Off Frequency | FIL3 cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| Filter type | The selection of filter type | LPF or HPF |
| Gain | Gain | -10dB ≤ Gain < 0dB |
| **EQ0** | | |
| Pole Frequency | EQ0 Pole Frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| Zero-point Frequency | EQ0 Zero-point Frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| Gain | Gain | -20dB ≤ Gain < +12dB |
| Gain2 | Gain2 | 0 / +12 / +24dB |
| **5 Band Equalizer** | | |
| EQ1-5 Center Frequency | EQ1-5 Center Frequency | 0Hz ≤ Center Frequency < (0.497 * fs) |
| EQ1-5 Band Width | EQ1-5 Band Width (Note 5) | 1Hz ≤ Band Width < (0.497 * fs) |
| EQ1-5 Gain | EQ1-5 Gain (Note 6) | -1≤ Gain < 3 |

Table 5. Parameter Setting of [Filter Setting]

Note 5. A gain difference is a bandwidth of 3dB from center frequency.
Note 6. When a gain is “-1”, EQ becomes a notch filter.

(2) “LPF Enable”, “HPF Enable”, “HPFAD Enable”, “FIL3 Enable”, “EQ0 Enable”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5” Please set ON/OFF of Filter by a check box.
When the check box next to the filter name is checked, the filter will become ON. When “Notch Filter Auto Correction” is checked, automatic correction of the center frequency of the notch filter is performed.

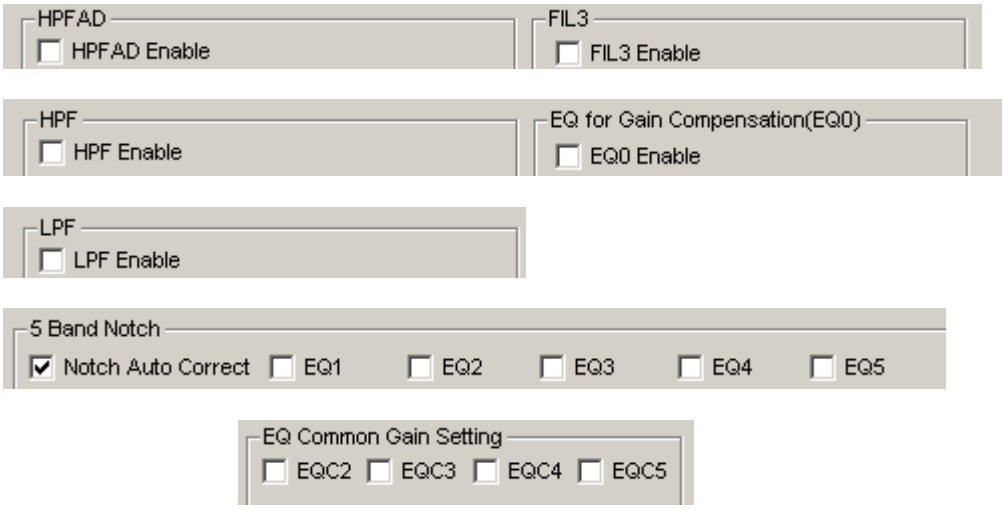



Figure 26. Filter ON/OFF Setting Check Box

## 11-2. [Register Setting]: Register Setting for Filter Dialog Box

Click the [Register Setting] button in the filter setting window to open the register setting dialog box shown below. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

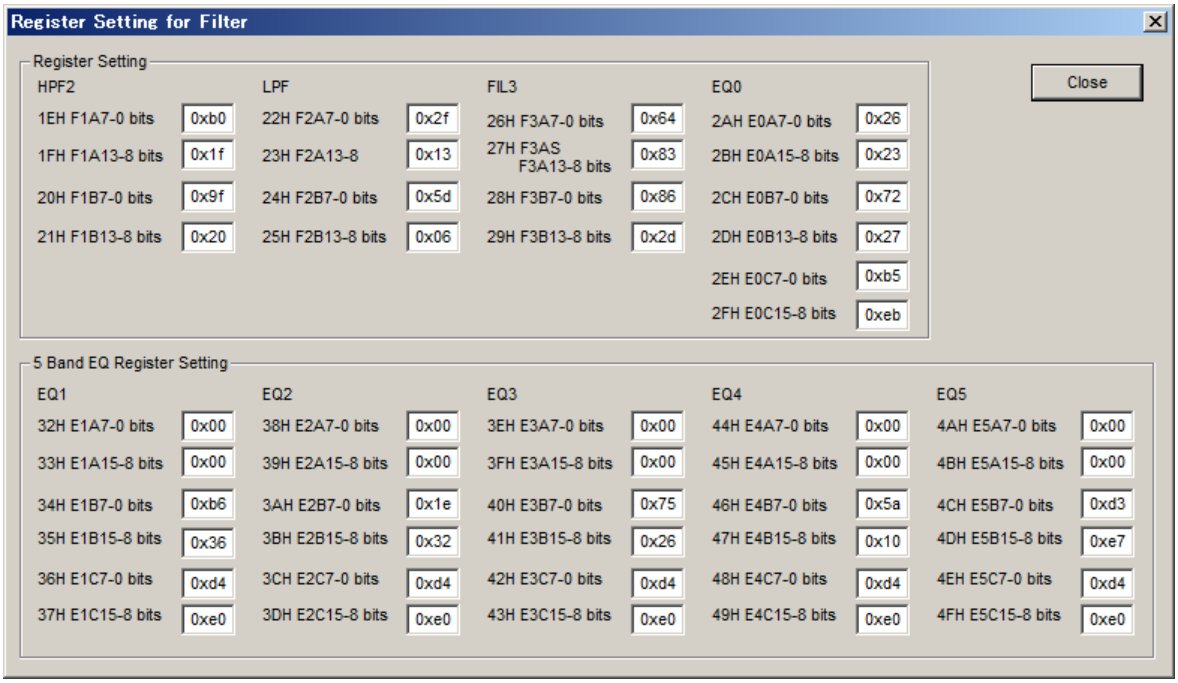



Figure 27. [Register Setting for Filter] Window

Followings are the cases when register set values are updated.
(1) When [Register Setting] button is pushed.
(2) When [Frequency Response] button is pushed.
(3) When [UpDate] button on a frequency characteristic indication window is pushed.
(4) When “Notch Filter Auto Correction” is ON/OFF.

### 11-3. [F Response]: Filter Plot Dialog Box

Click the [F Response] button in the filter setting window to open the filter plot dialog box shown below. Change Frequency Range, and indication of a frequency characteristic is updated when push a [UpDate] button.

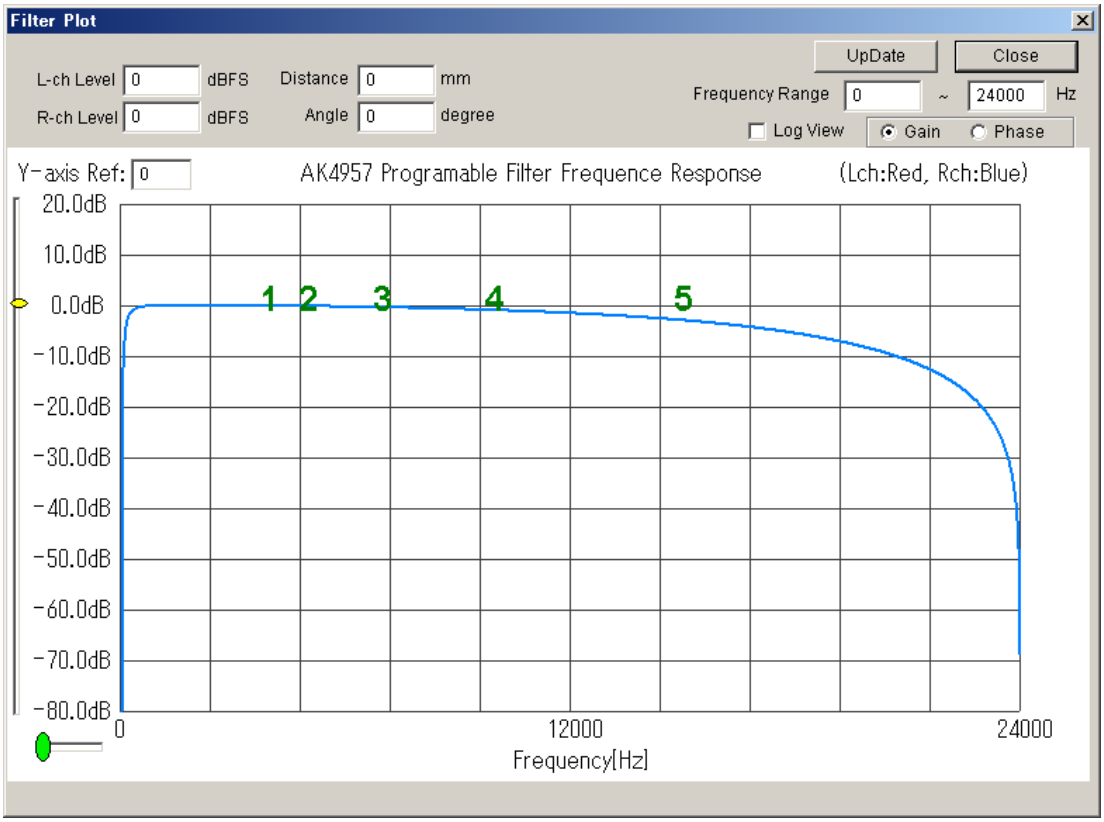



Figure 28. [F Response] Window

[Frequency Range] : The width of the frequency display is specified.
[Update] : Redraws the filter characteristics.
[Gain/Phase] : "Gain/Phase" display Switch.
[Log View] : "Linear/Log" display Switch.
[Close] : Closes the dialog box and ends process.

**~ Adjustment of vertical range ~**

[Y-axis Ref] : Set the center value of Y-axis.
[Vertical slider] : Moves center reference of the Y-axis.
[Horizontal slider] : Adjust scale of the X-axis.
(Left: shrinking, Right: expanding)

### 11-4. 5-BandEQ operation in Filter Plot screen

When EQ(1~5) is turned on, a green number is displayed on the Filter Plot dialog box.
This number shows the setting of the center frequency and the gain of each EQ.
The displayed number can be moved by dragging, and filter characteristics are set on this screen.
The center frequency and the gain setting are changed by left click dragging.
The setting of the bandwidth is changed by right click dragging.

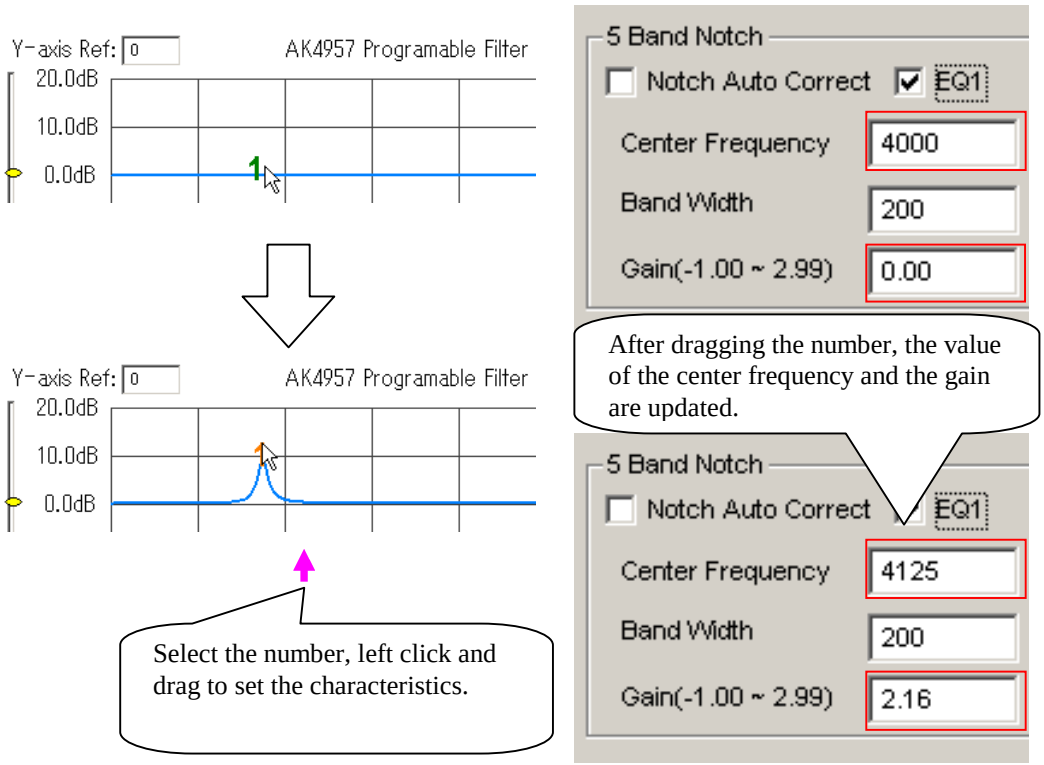



Figure 29. Filter Setting (Left-clicking operation)

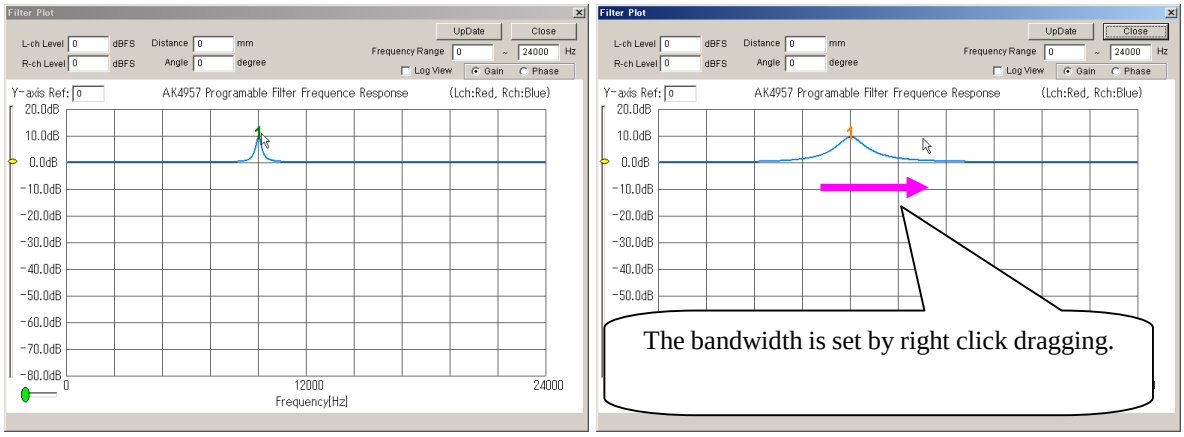



Figure 30. Filter Setting (Right-clicking operation)

### 11-5. Simulation of Fil3 Filter

Setting of Stereo-MIC
[L-ch Level]/[R-ch Level] : Input the level of the MIC input.
[Distance] : Set the distance between the sound source and the MIC.
[Angle] : Set the angle between the sound source and the MIC.

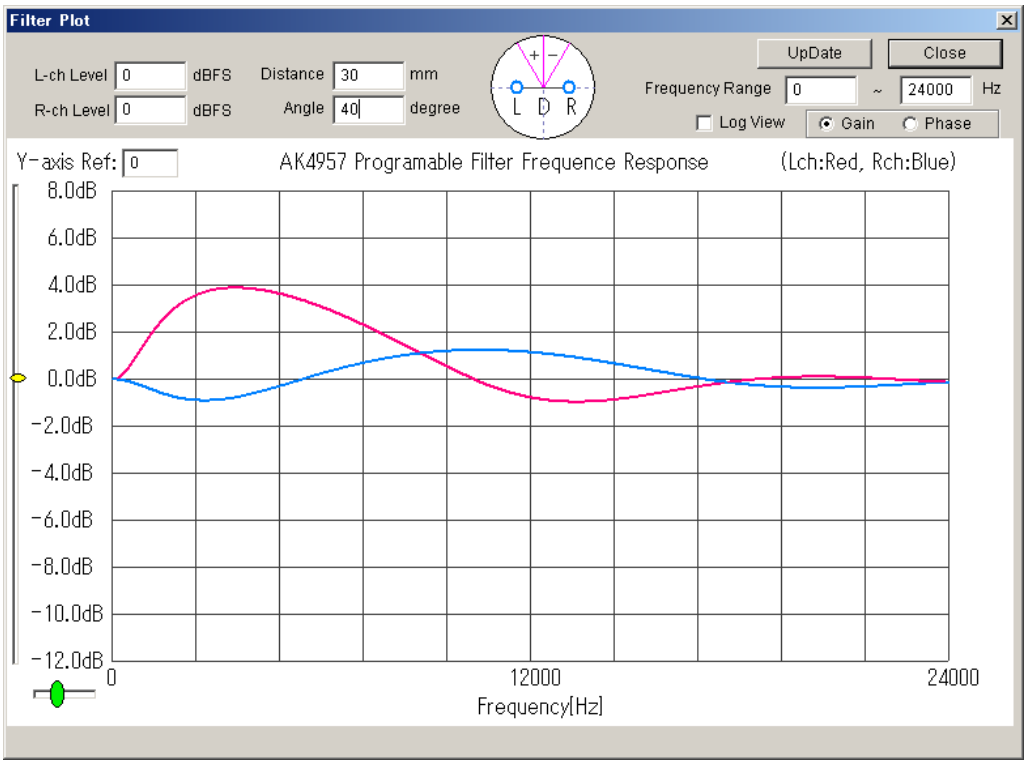
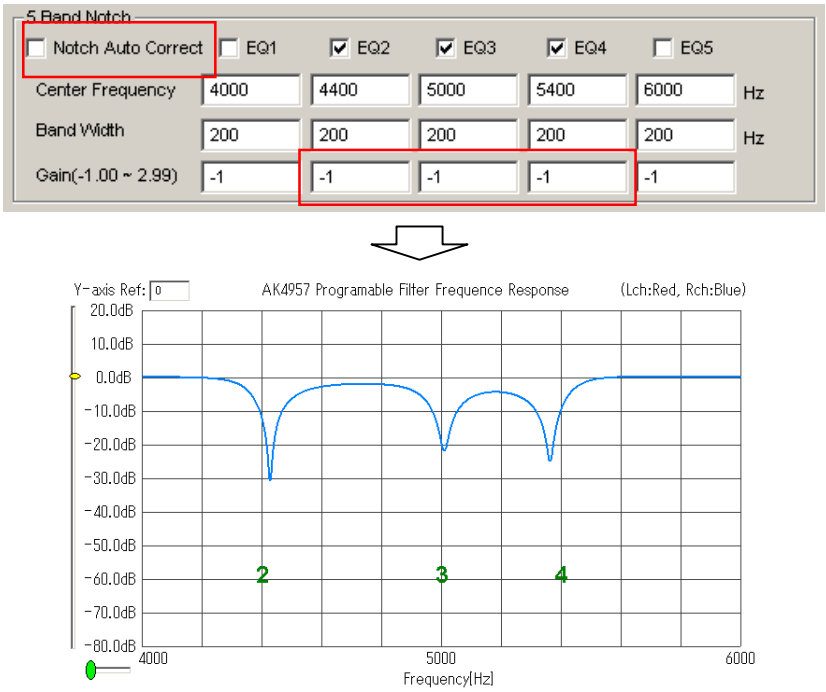



Figure 31. Simulation of Fil3 Filter

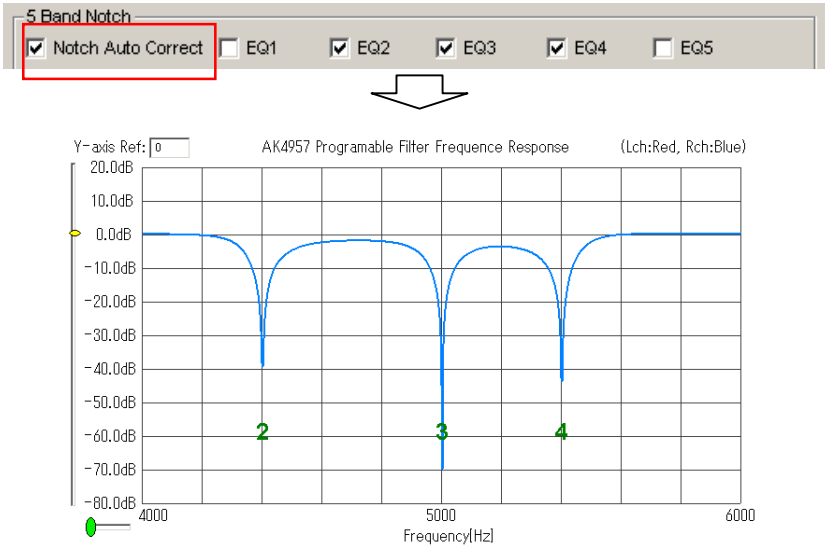
### 11-6. “Notch Auto Correct” Function

If the gain of 5-Band EQ is set to “-1”, Equalizer becomes a notch filter.
If the center frequency of two or more notch filters are adjacent, each center frequency will shift slightly (Figure 32).
Check the “Notch Auto Correct” check box to correct notch filter center frequency automatically (Figure 33).
The automatic correction of center frequency is only effective for the equalizer that the gain is set to “-1” (Note 7).

Note 7. There is a possibility that the automatic correction is not applied appropriately if the width of the center frequency is smaller than that of the bandwidth setting.




Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Bandwidth : 200Hz(EQ2~4)
Figure 32. “Notch Auto Correct” function is “OFF”




Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Bandwidth : 200Hz(EQ2~4)
Figure 33. “Notch Auto Correct” function is “ON”

## 12. [DRC Setting]: [DRC Function] Dialog Box

Click the [DRC Setting] button in the function tab to open the DRC function dialog box shown in Figure 34. Refer to the datasheet for register settings of the AK4954A.

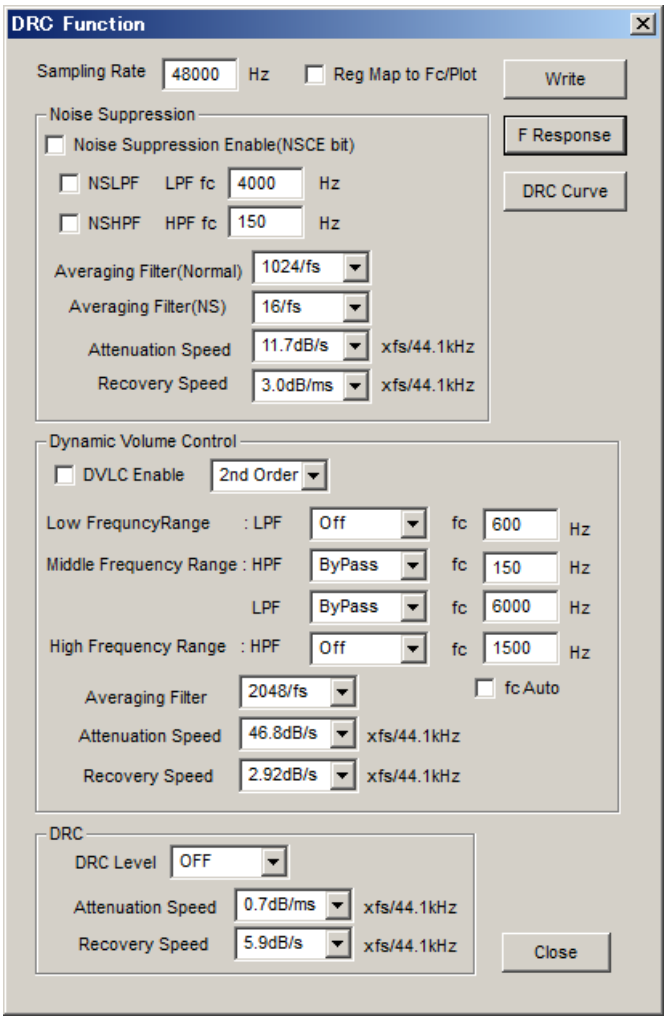



Figure 34. [DRC Setting] Window

[Write] : Executes all filter calculations, and coefficients are written.
[F Response] : Opens the filter characteristic dialog.
Executes all filter calculations, but filter coefficients are not written.
[DRC Curve] : Opens the DRC Curve dialog.
[Close] : Closes the dialog box and ends process.

## 12-1. Parameter Setting

(1) Set a parameter of each Filter and Gain.

| Parameter | Function | Setting Range |
|---|---|---|
| Sampling Rate | Sampling frequency (fs) | 7350Hz ≤ fs ≤ 96000Hz |
| **Noise Suppression** | | |
| LPF | Low pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| HPF | High pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| **Dynamic Volume Control** | | |
| Low Frequency Range | | |
| LPF | Low pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| | | |
| Middle Frequency Range | | |
| LPF | Low pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| HPF | High pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| | | |
| High Frequency Range | | |
| HPF | High pass filter cut off frequency | fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs) |
| | | |

Table 6. Parameter Setting of [DRC Function]

(2) When the checkbox next to each filter name is checked, the filter will be enabled. When “DVLC Enable” button is checked, the filters of Low/Middle/High Range are enabled according to setting of pull-down menu. When “fc Auto” checkbox is checked, the frequency responses of low frequency and high frequency ranges become flat automatically.


Figure 35. Filter ON/OFF setting button

## 12-2. Frequency Response

Click the [F Response] button in the DRC setting window to display frequency characteristics.

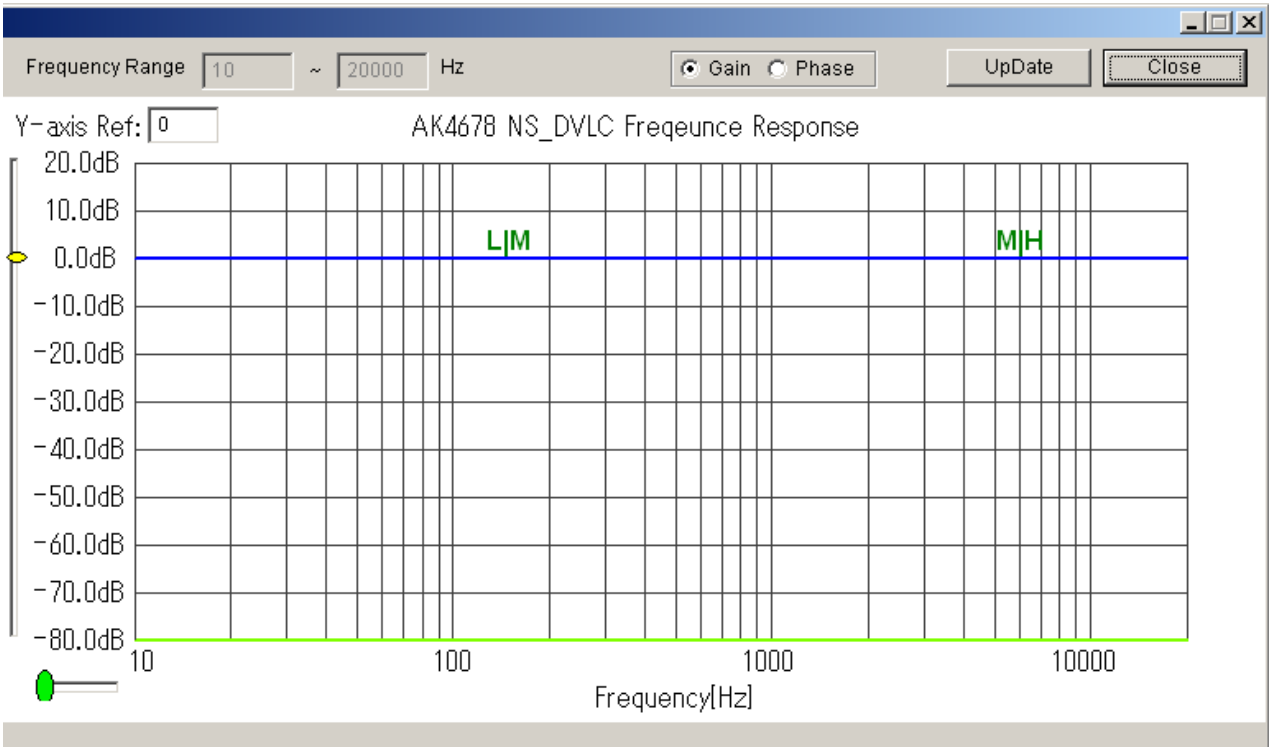



Figure 36. A frequency characteristic indication result

[Frequency Range] : The width of the frequency display is specified.
[Update] : Redraws the filter characteristics.
[Gain/Phase] : “Gain/Phase” display Switch.
[Close] : Closes the dialog box and ends process.

## 12-3. Filter Setting

The filter setting can be executed by checking the “NSLPF”, “NSHPF” or “DVLC Enable” checkbox in the [DRC function] dialog box.

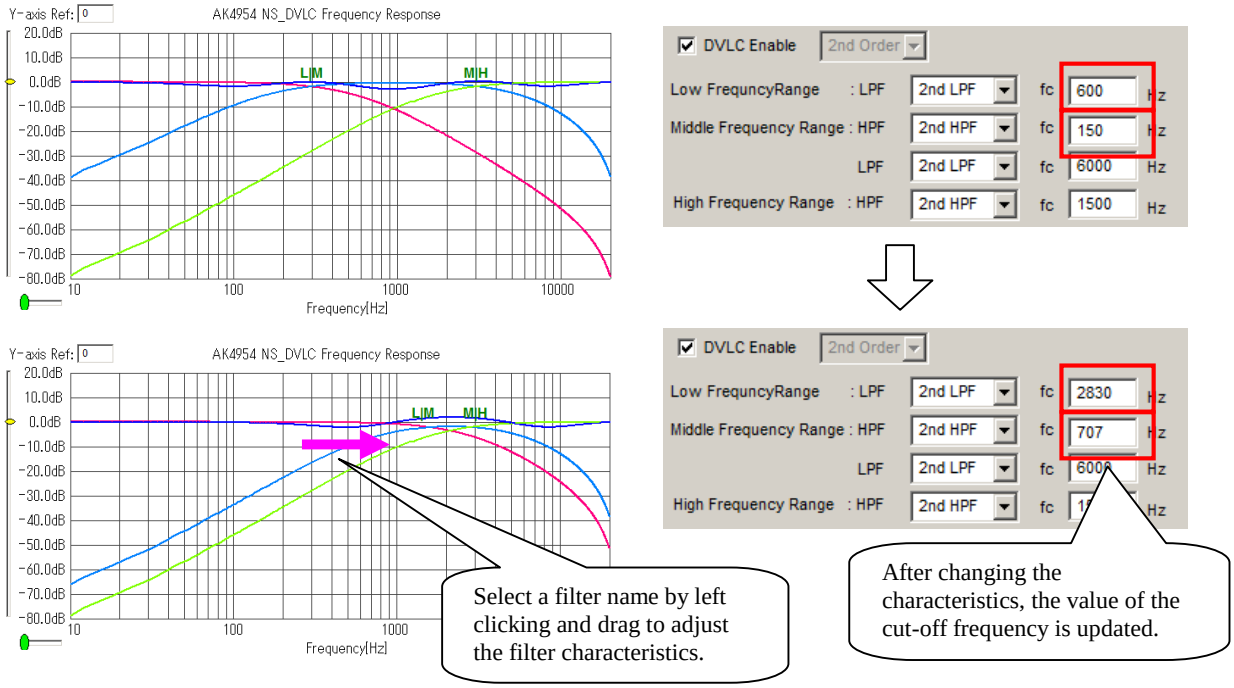



Figure 37. Filter Setting (Left-clicking operation)

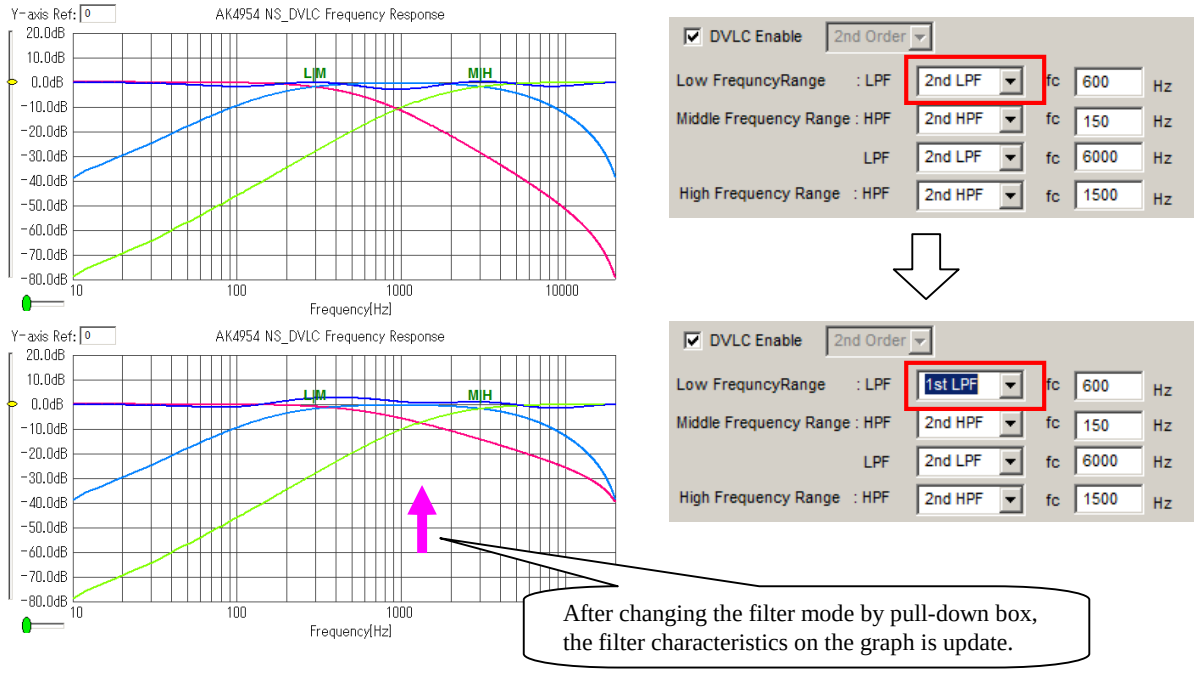



Figure 38. Filter Setting (Filter Selecting)

## 12-4. Noise Suppression

Click the [DRC curve] button in the DRC setting window to open the DRC curve window. Click the “NS” radio button to adjust the noise suppression setting.

Noise Suppression Threshold Low Level and Reference Value can be adjusted by left-click dragging.

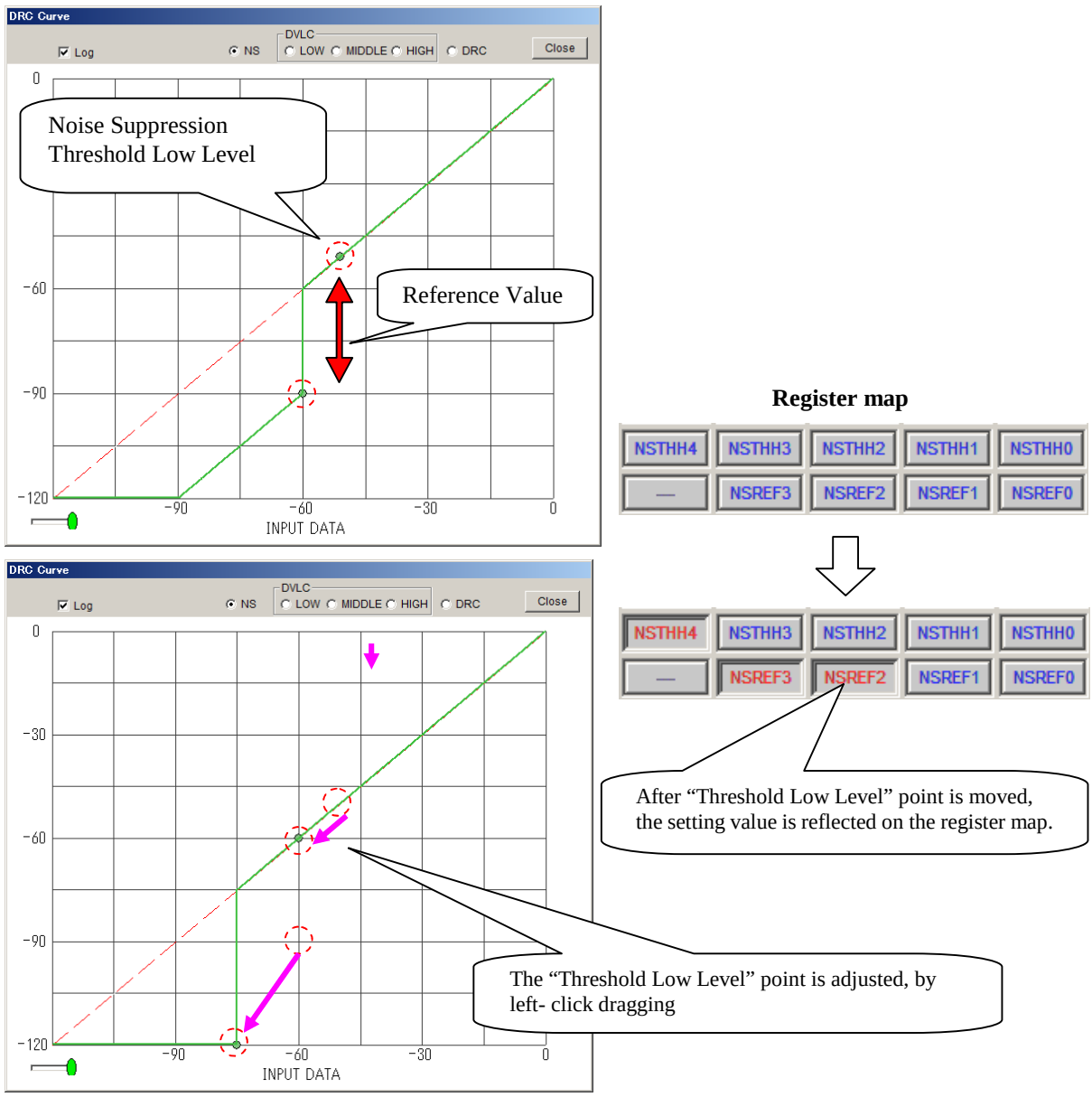



Figure 39. Noise Suppression Setting

## 12-5. Dynamic Volume Control

Dynamic Volume is displayed when “LOW”, ”MIDDLE” or “HIGH” radio button in “DVLC” is checked. Then, a register set point is also updated.

Dynamic Volume Control Points can be adjusted by left-click dragging.

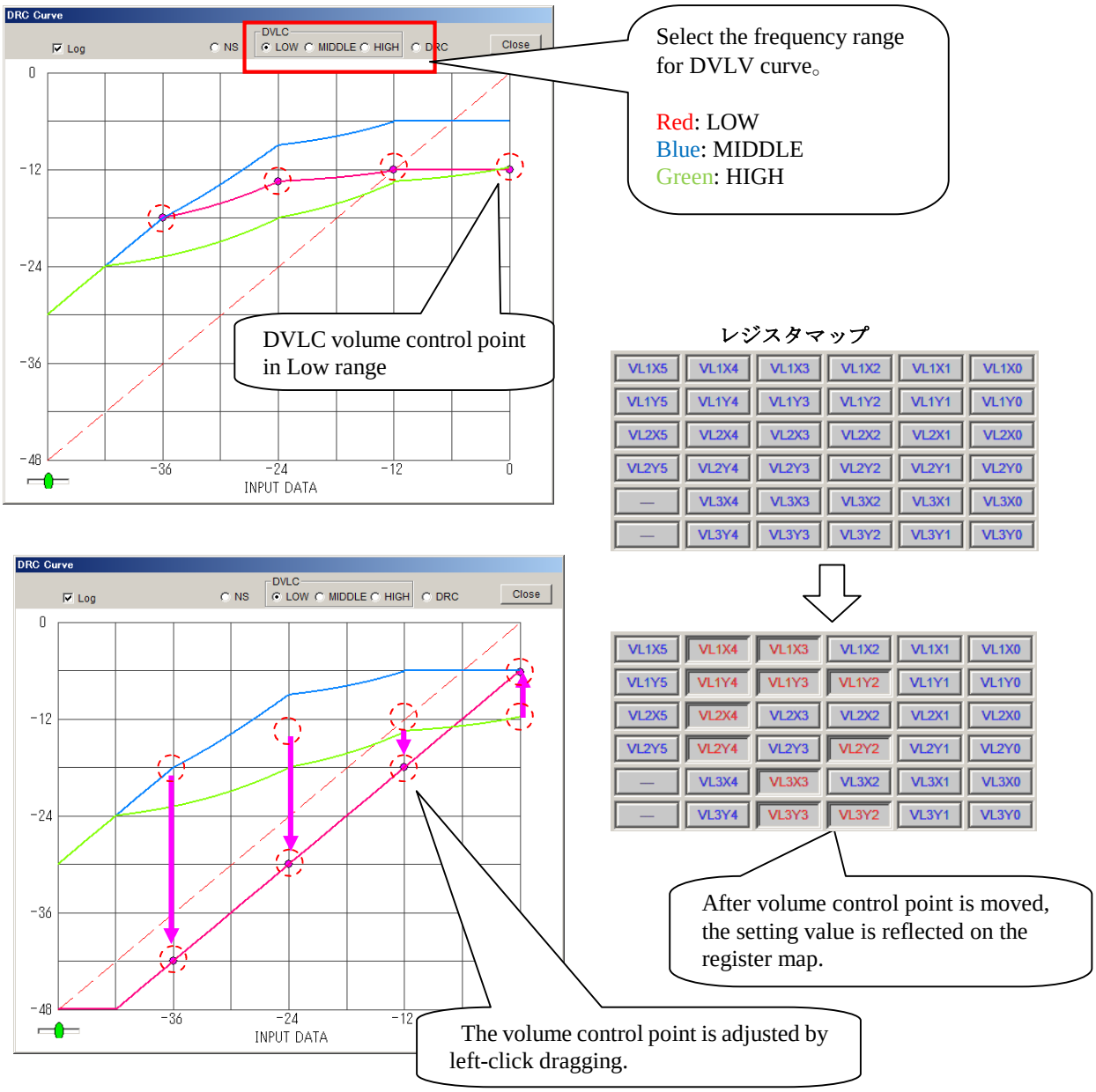



Figure 40. DVLC Curve Setting

## 12-6. Dynamic Range Control

Dynamic Range Control is displayed when “DRC” radio button is checked. Then, a register set point is also updated.

Dynamic Range Compression Level can be adjusted by left-click dragging.

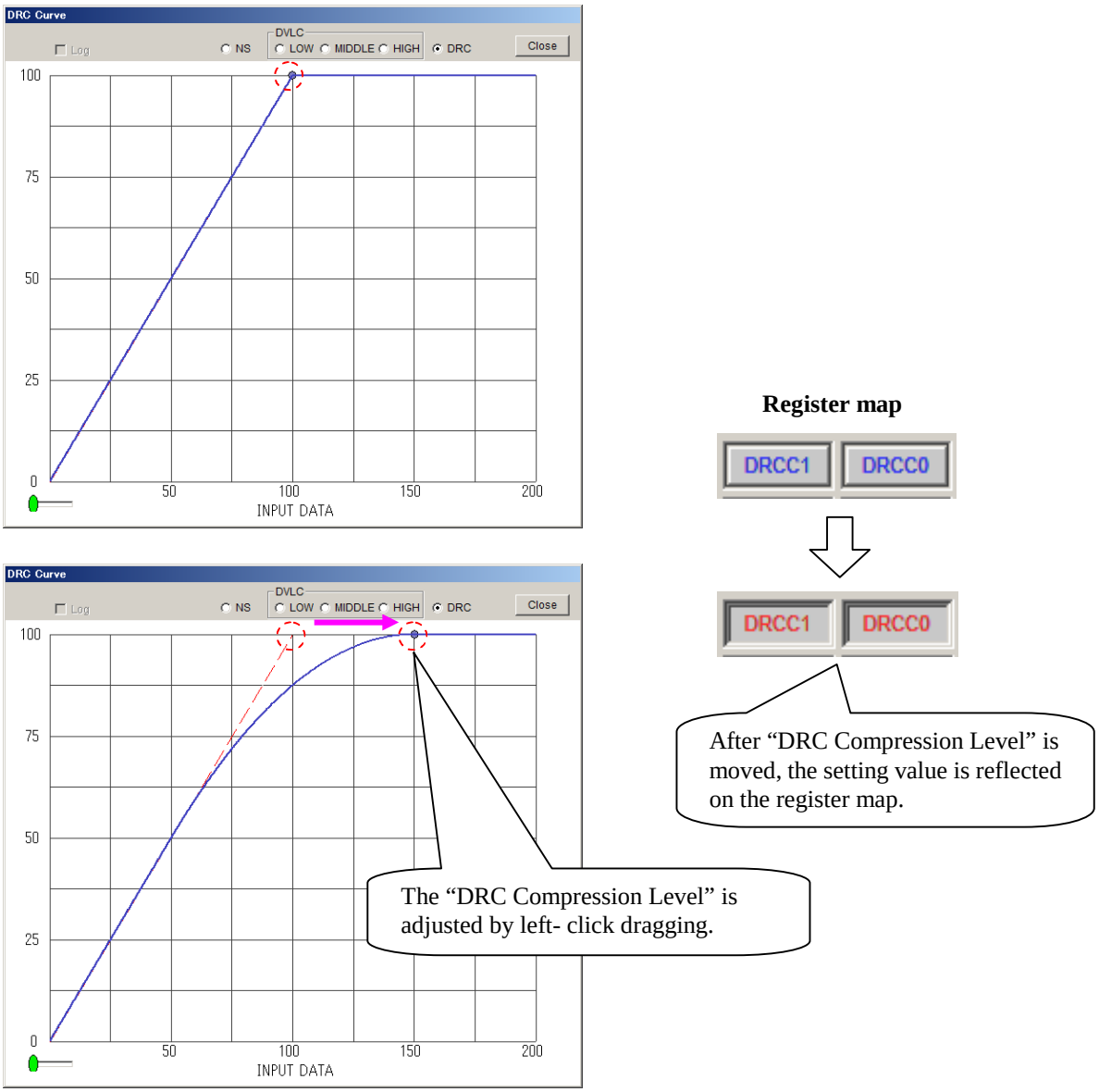



Figure 41. Dynamic Range Control Setting

## MEASUREMENT RESULTS

### [Measurement condition]

- Measurement unit : Audio Precision, System two Cascade
- MCKI : 256fs (11.2896MHz, 24.576MHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz
- Bit : 24bit
- Measurement Mode : EXT Slave Mode
- Power Supply : AVDD = SVDD = TVDD = 3.3V, DVDD = 1.8V
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz (fs=44.1kHz), 20 ~ 40kHz (fs=96kHz)
- Temperature : Room

### [Measurement Results]

1. ADC

| | | Result | | Unit |
|---|---|---|---|---|
| | | Lch | Rch | |
| ADC: LIN1/RIN1 → ADC → IVOL, IVOL=0dB, ALC=OFF | | | | |
| MGAIN = +20dB | | | | |
| S/(N+D) (-1dBFS) | fs=44.1kHz, BW=20kHz | 89.2 | 88.9 | dB |
| | fs=96kHz, BW=40kHz | 84.9 | 85.2 | dB |
| DR | (-60dBFS, A-Weighted) | 97.0 | 96.7 | dB |
| S/N | (A-weighted) | 97.1 | 96.8 | dB |
| MGAIN = 0dB | | | | |
| S/(N+D) (-1dBFS) | fs=44.1kHz, BW=20kHz | 88.2 | 89.0 | dB |
| | fs=96kHz, BW=40kHz | 81.5 | 82.2 | dB |
| DR | (-60dBFS, A-Weighted) | 100.9 | 101.0 | dB |
| S/N | (A-weighted) | 101.0 | 101.1 | dB |

2. DAC

| | | Result | | Unit |
|---|---|---|---|---|
| | | Lch | Rch | |
| Headphone-Amp: DAC → HPL/HPR, IVOL=DVOL=0dB, RL=16Ω | | | | |
| S/(N+D) | fs=44.1kHz, BW=20kHz | 69.9 | 68.9 | dB |
| | fs=96kHz, BW=40kHz | 69.8 | 68.7 | dB |
| S/N | (A-weighted) | 100.7 | 100.6 | dB |
| Speaker-Amp: DAC → SPP/SPN, IVOL=DVOL=0dB, SPKG=+6.26dB, $R_L$=8Ω | | | | |
| fs=44.1kHz, BW=20kHz | | | | |
| S/(N+D) | (-0.5dBFS) | 76.1 | | dB |
| Output Noise Level | (A-Weighted) | -96.3 | | dBV |
| Stereo Line Output: DAC → LOUT/ROUT, IVOL=DVOL=0dB, RL=20kΩ | | | | |
| fs=44.1kHz, BW=20kHz | | | | |
| S/(N+D) | | 85.6 | 85.4 | dB |
| S/N | (A-weighted) | 89.1 | 89.1 | dB |

**[Plot]**

**1. ADC (LIN1/RIN1 → ADC) (+20dB)**
**[fs=44.1kHz]**

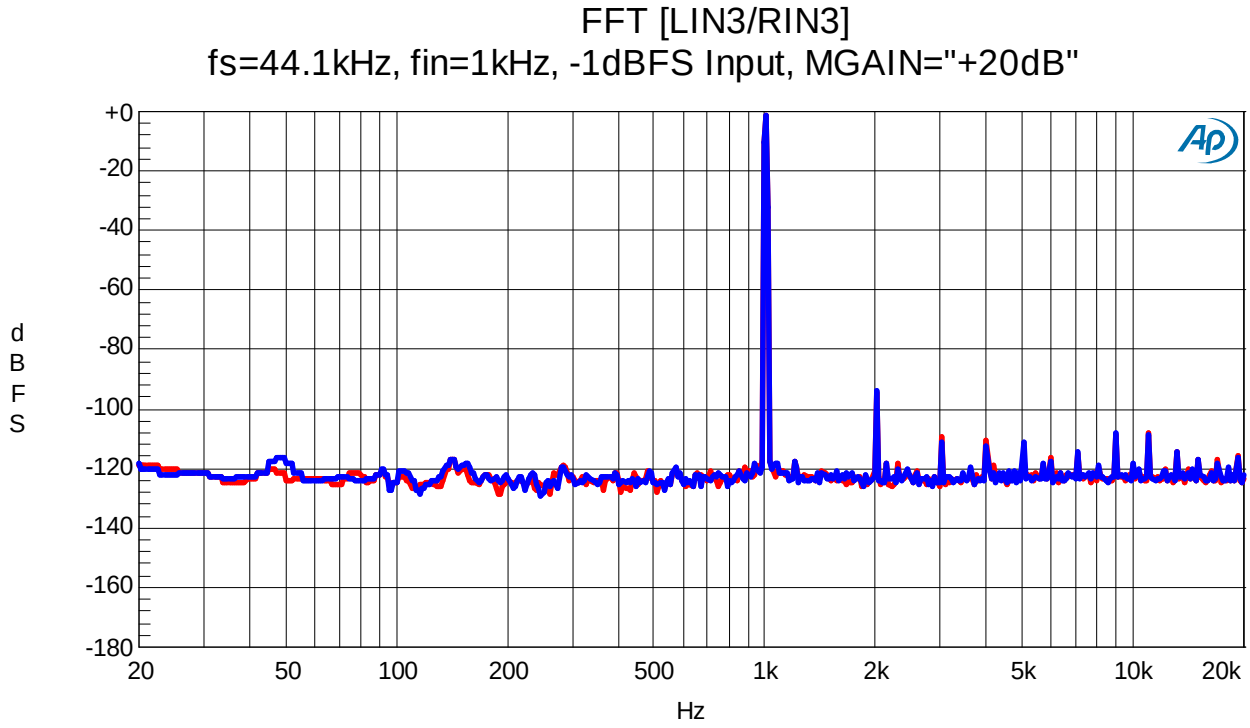



Figure 42. FFT (Input level= -1dBFS)

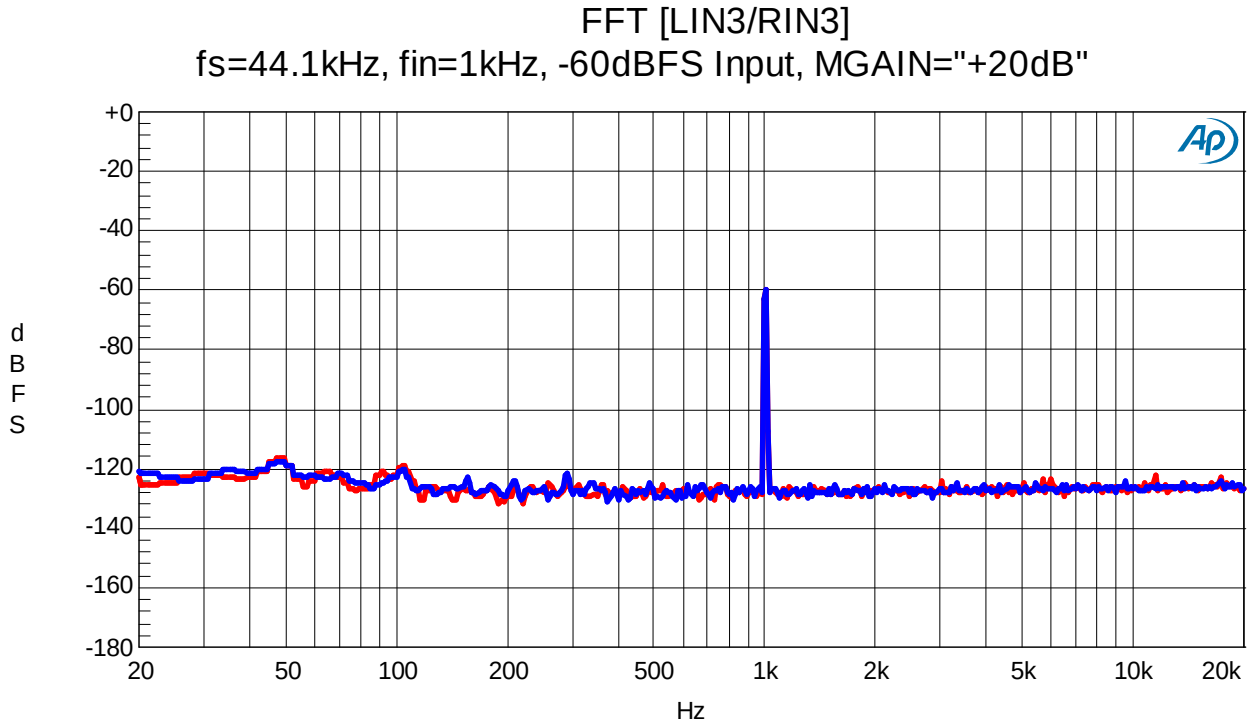



Figure 43. FFT (Input level= -60dBFS)

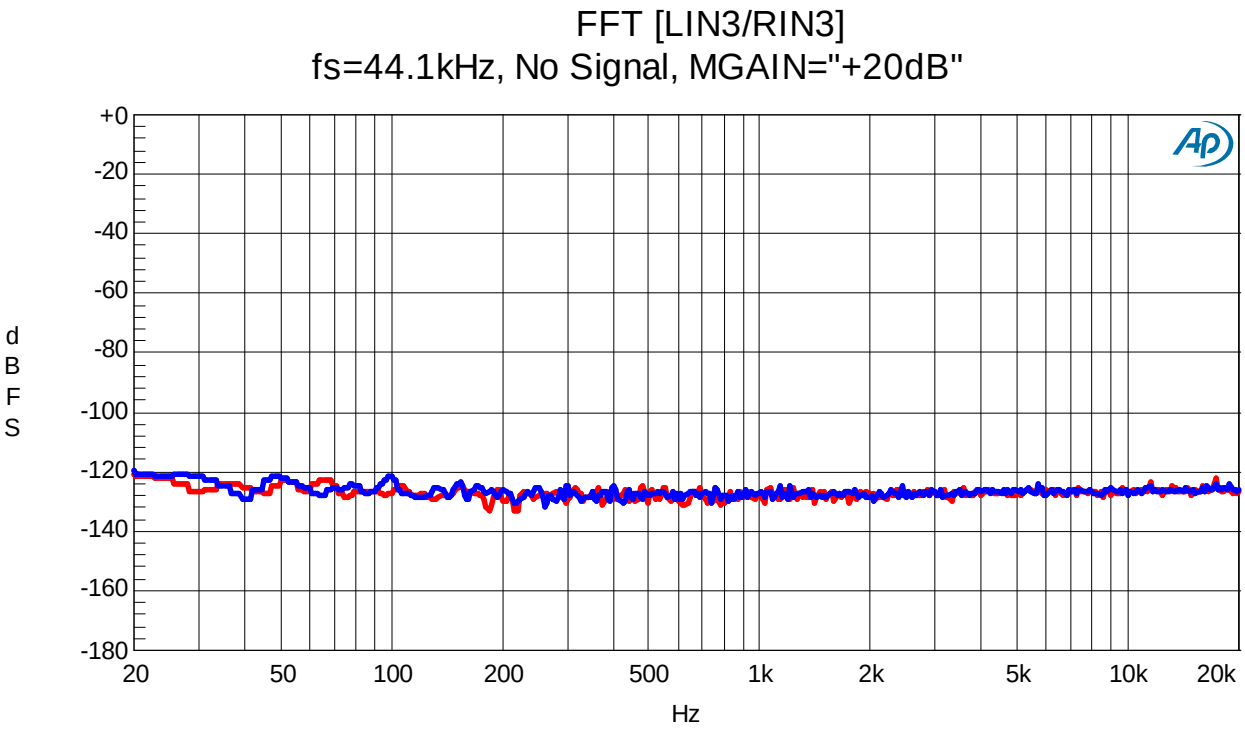



Figure 44. FFT (No signal)

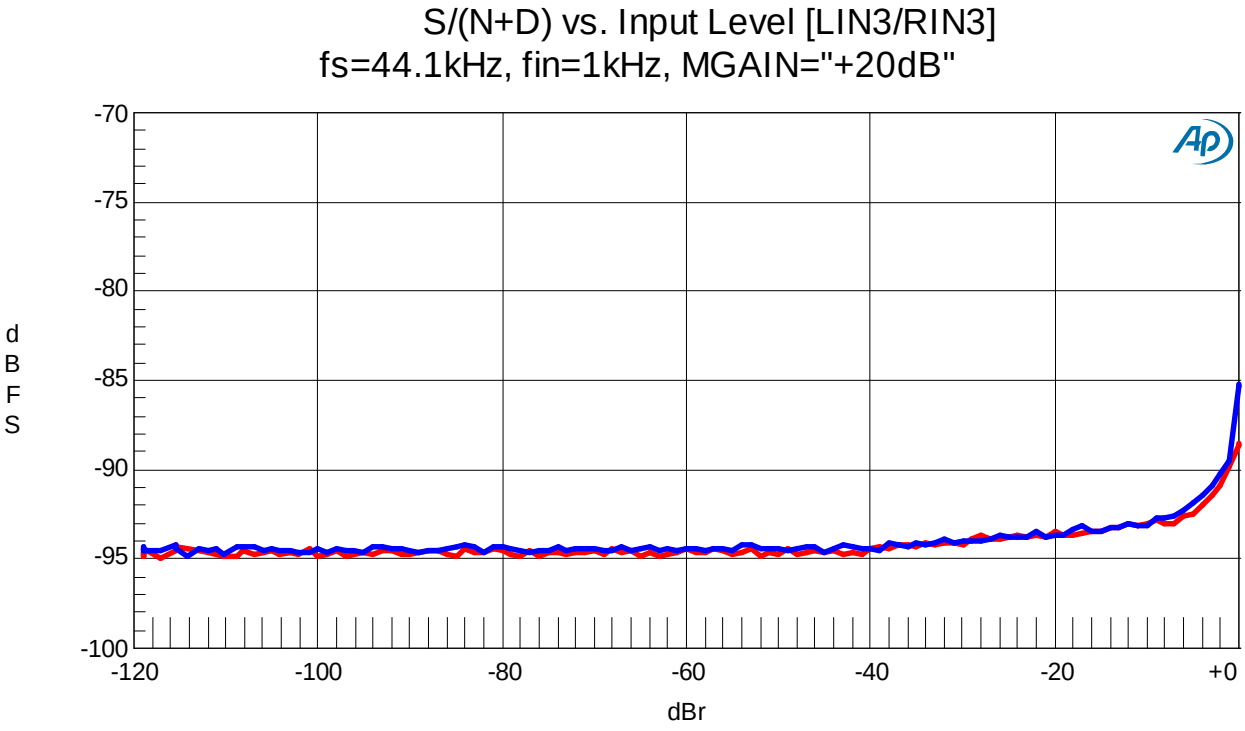



Figure 45. THD+N vs. Input Level

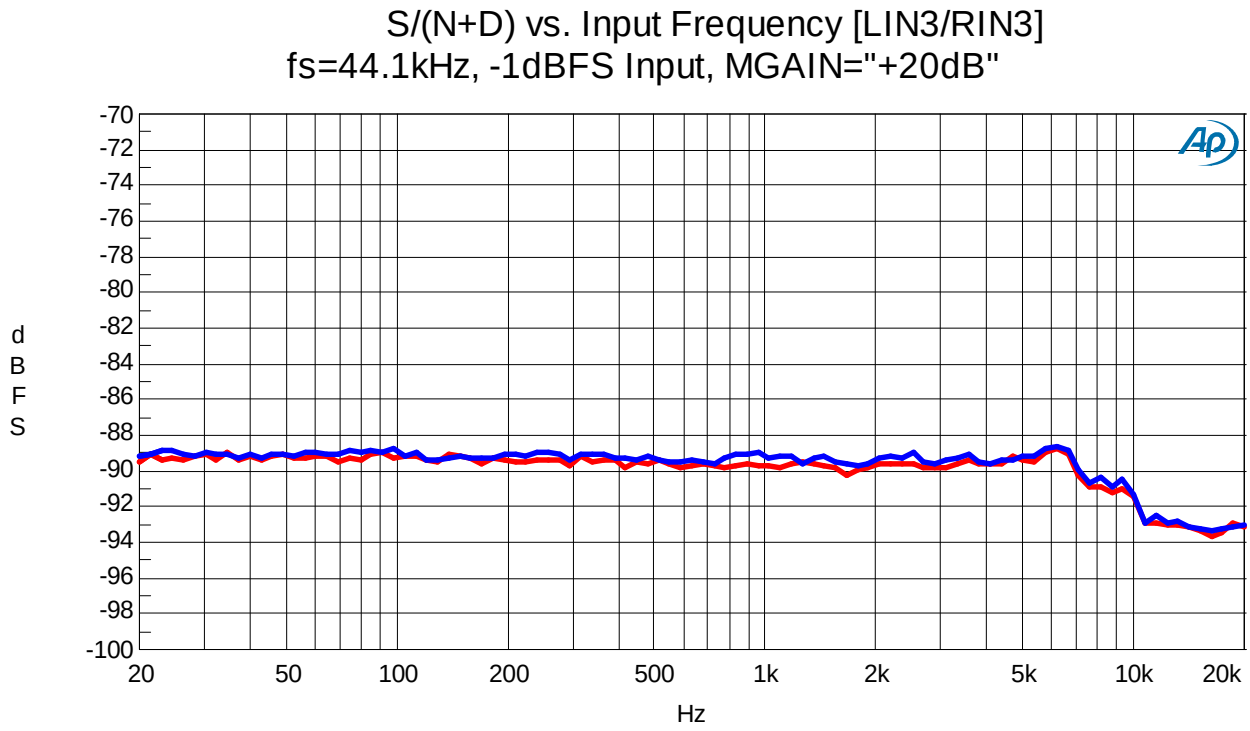



Figure 37. THD+N vs. Input Frequency

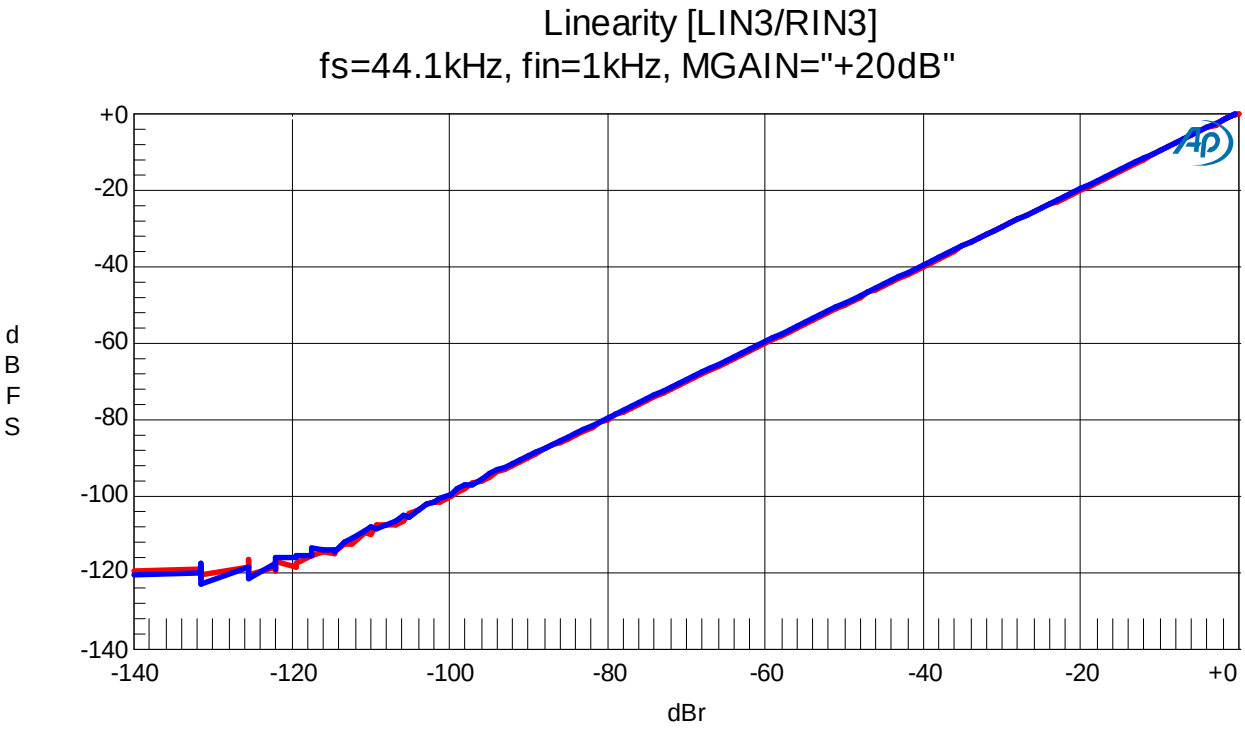



Figure 47. Linearity

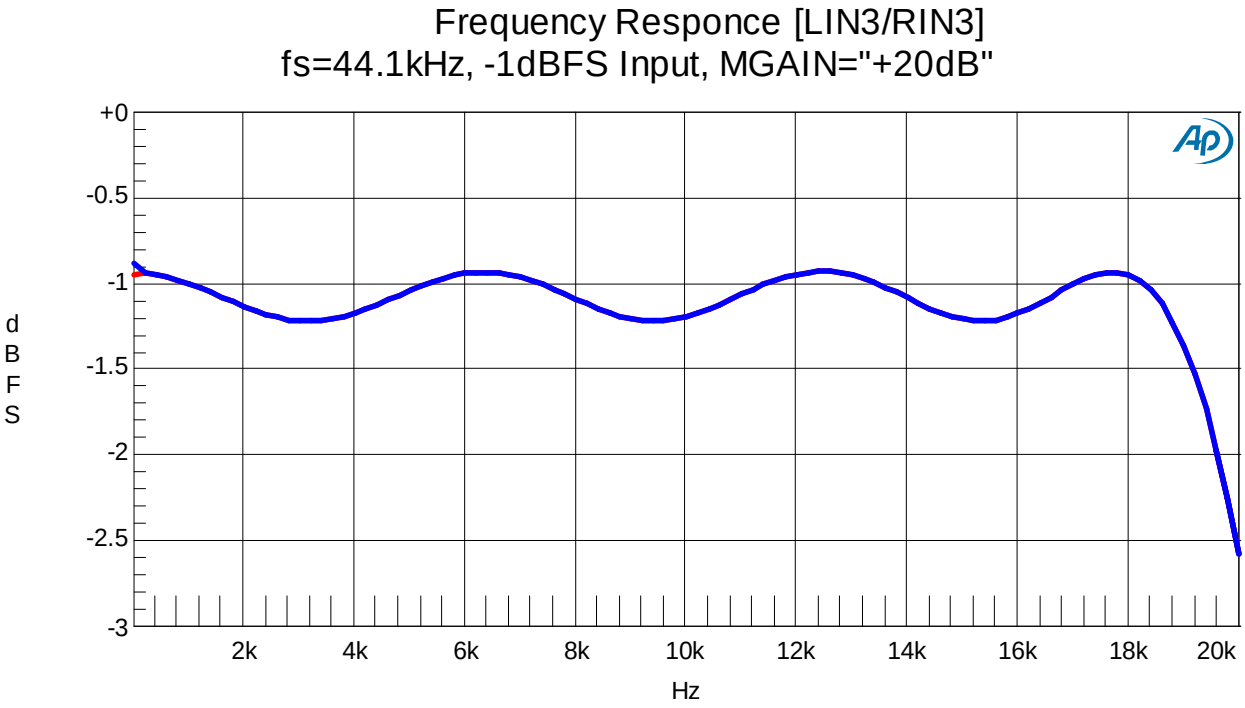



Figure 48. Frequency Response

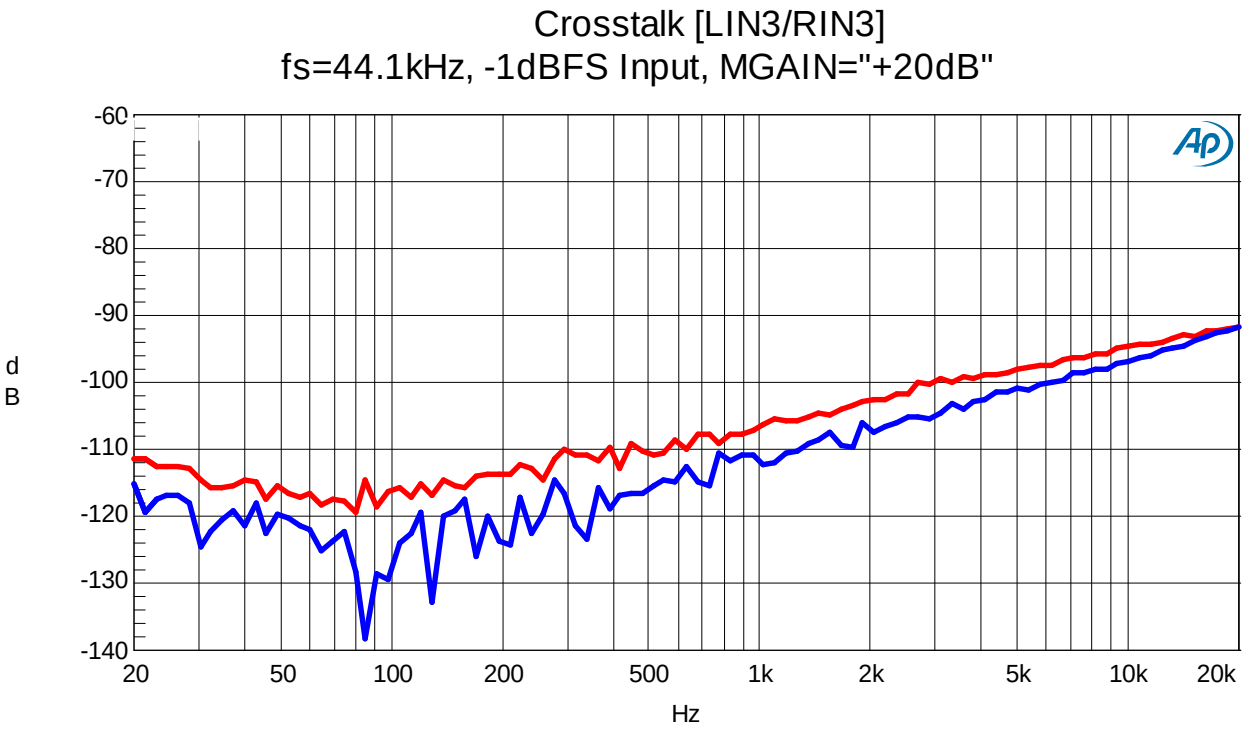



Figure 49. Crosstalk

**2. ADC (LIN1/RIN1 → ADC) (+20dB)**
**[fs=96kHz]**

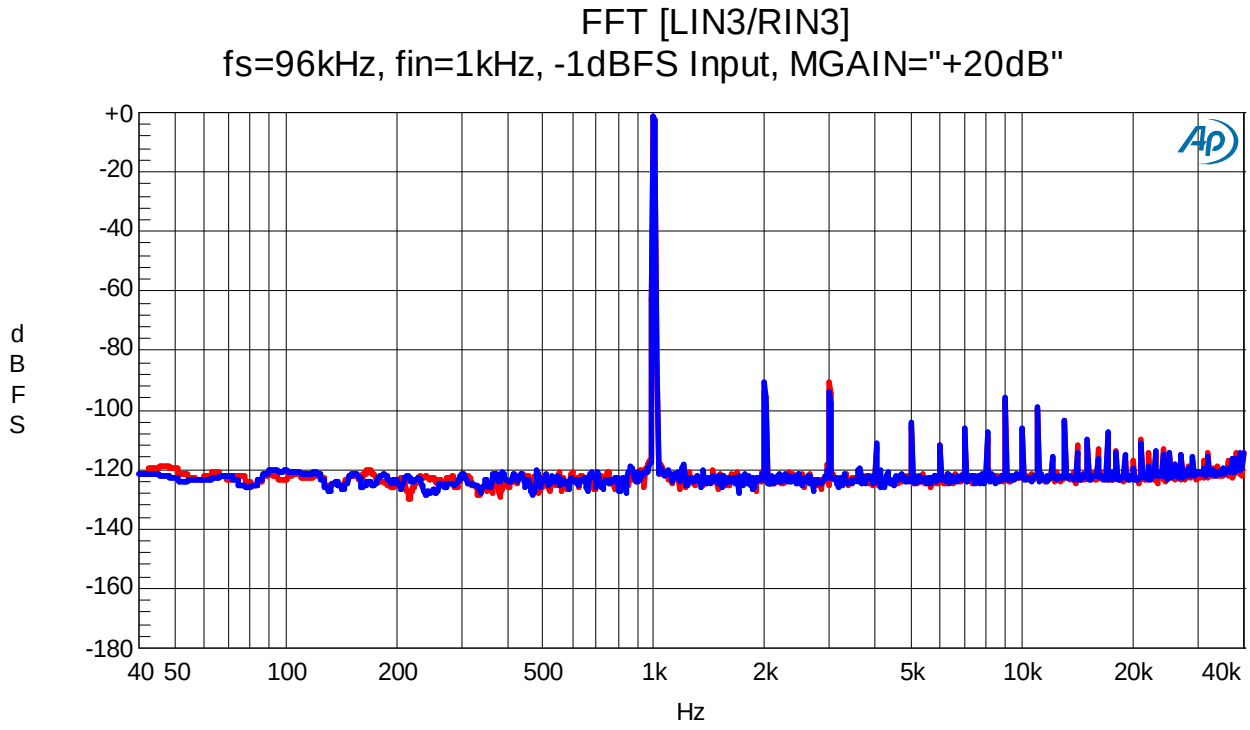



Figure 50. FFT (Input level= -1dBFS)

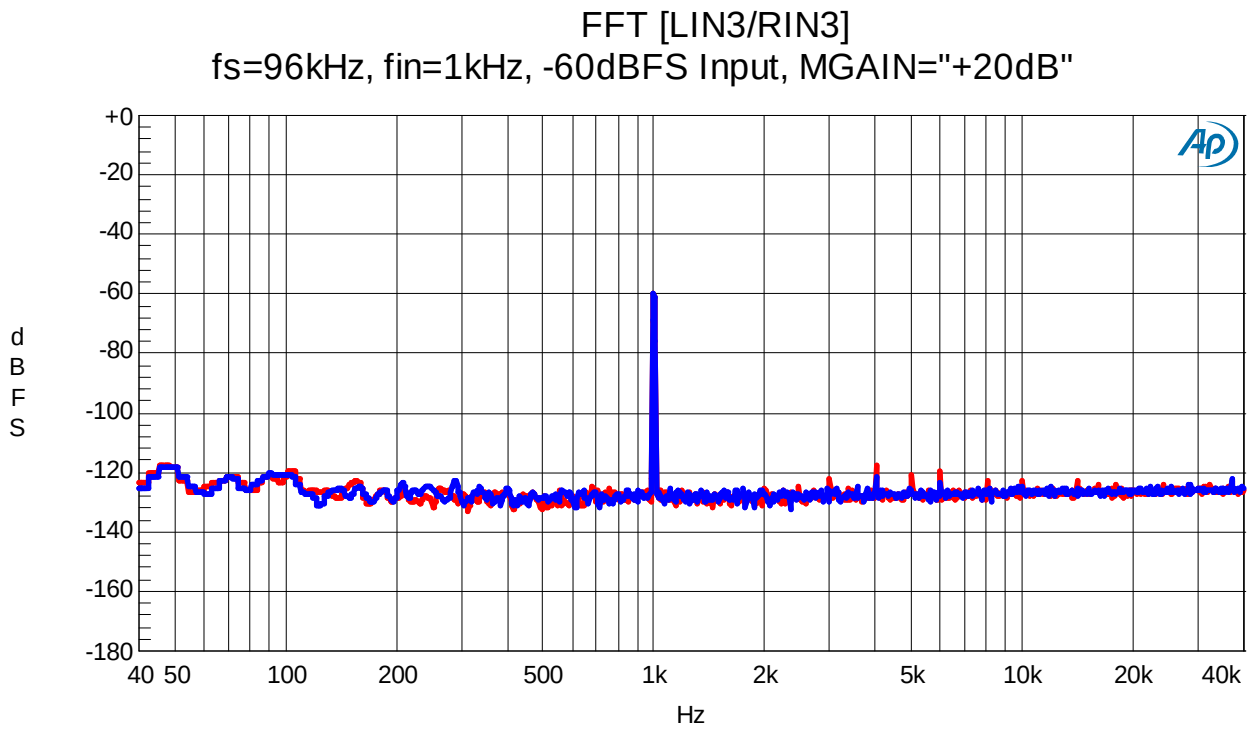



Figure 51. FFT (Input level= -60dBFS)

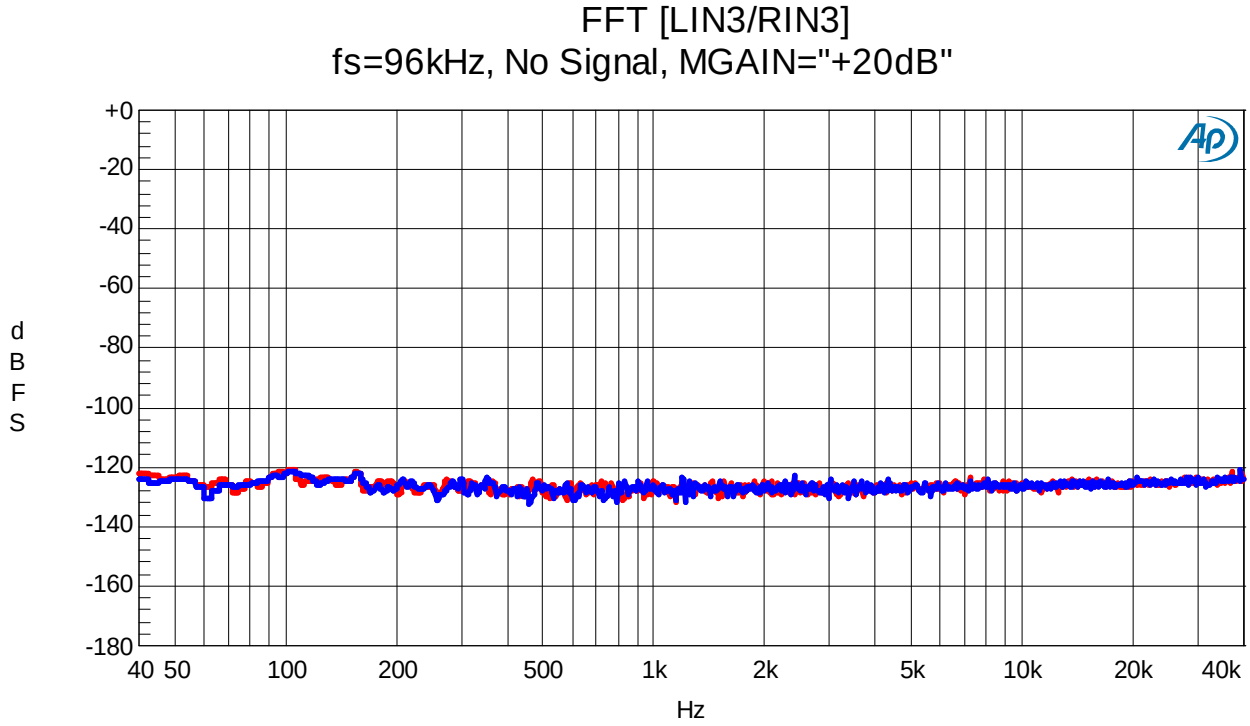



Figure 52. FFT (No signal)

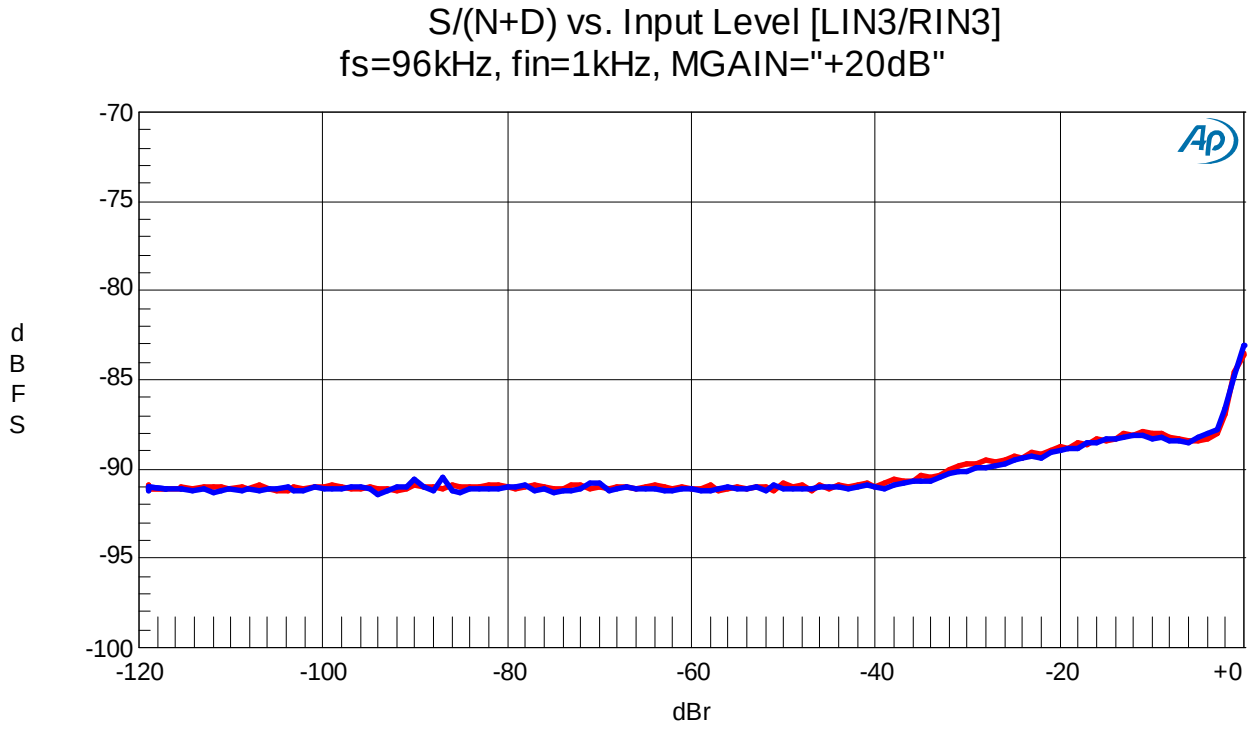



Figure 53. THD+N vs. Input Level

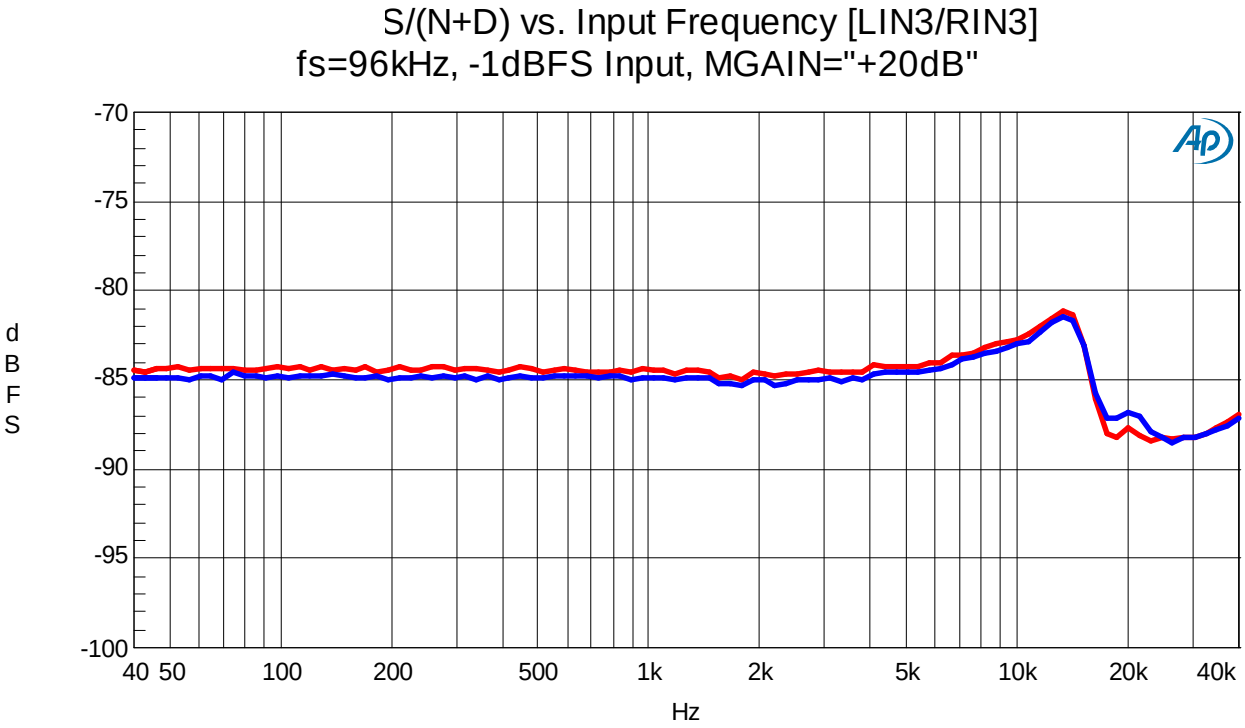



Figure 54. THD+N vs. Input Frequency

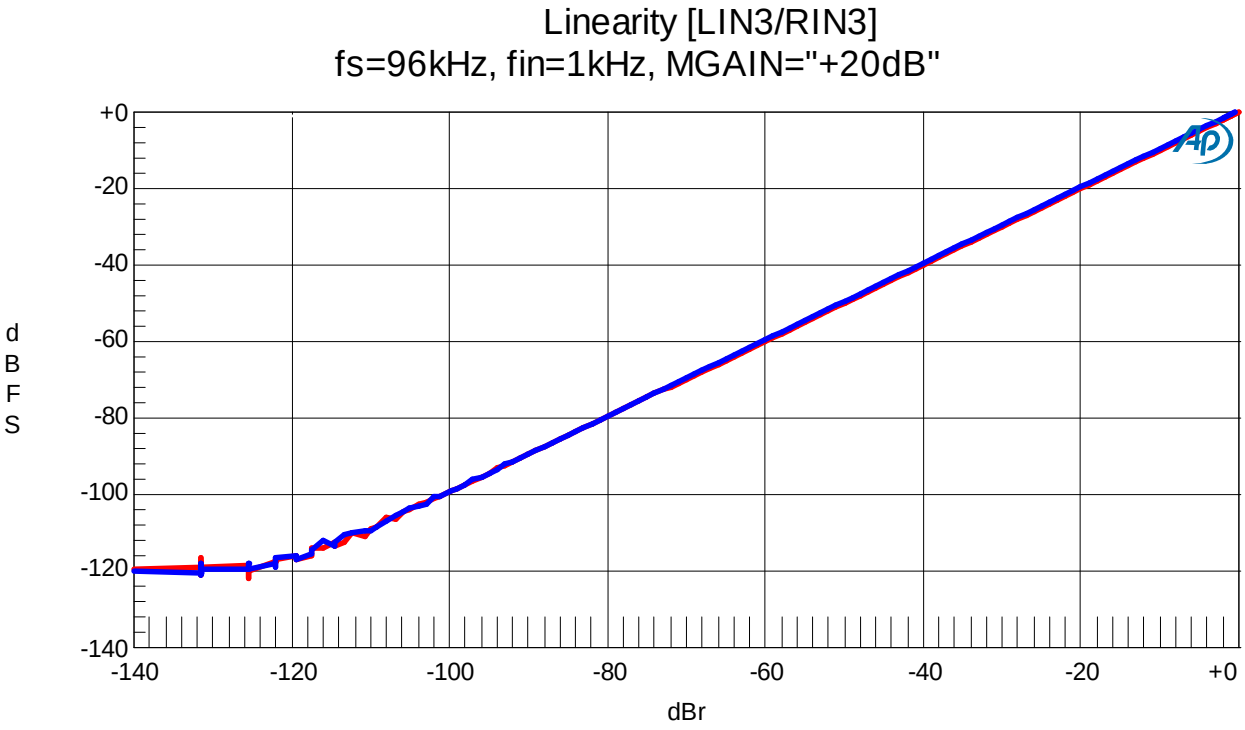



Figure 55. Linearity

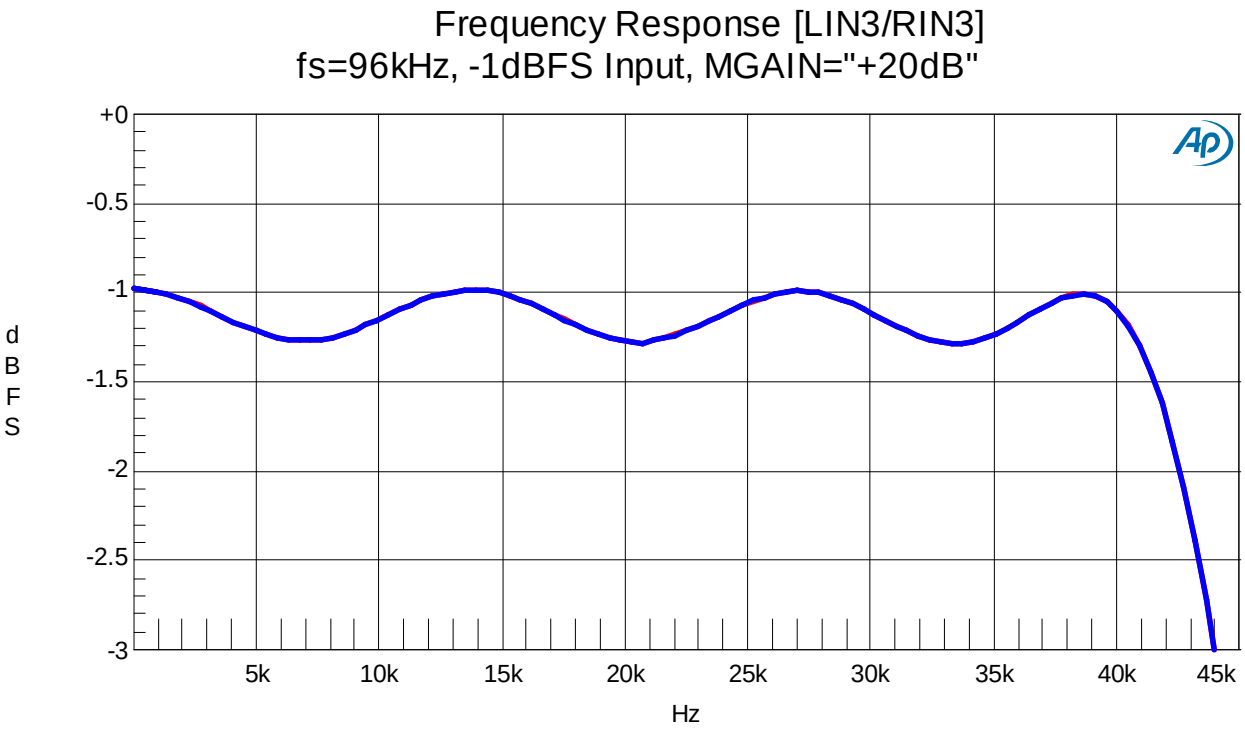



Figure 56. Frequency Response

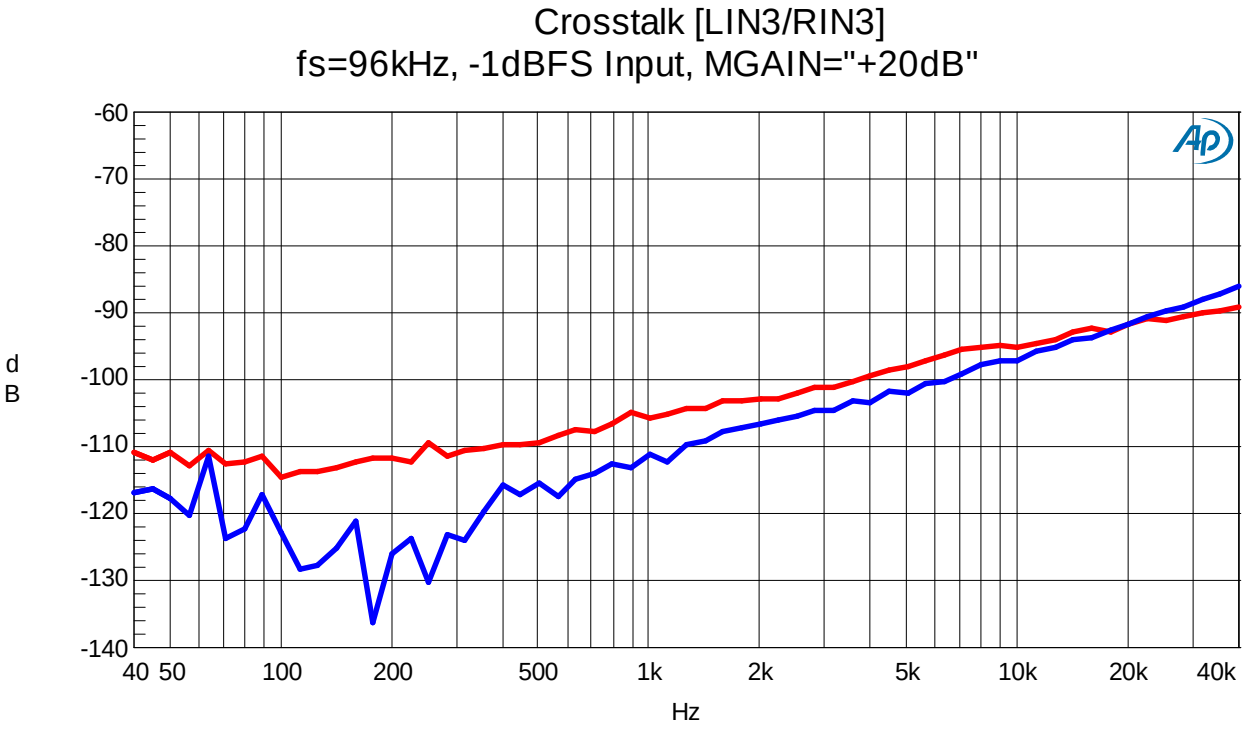



Figure 57. Crosstalk

**3. DAC (DAC→ HPL/HPR)**
**[fs=44.1kHz]**

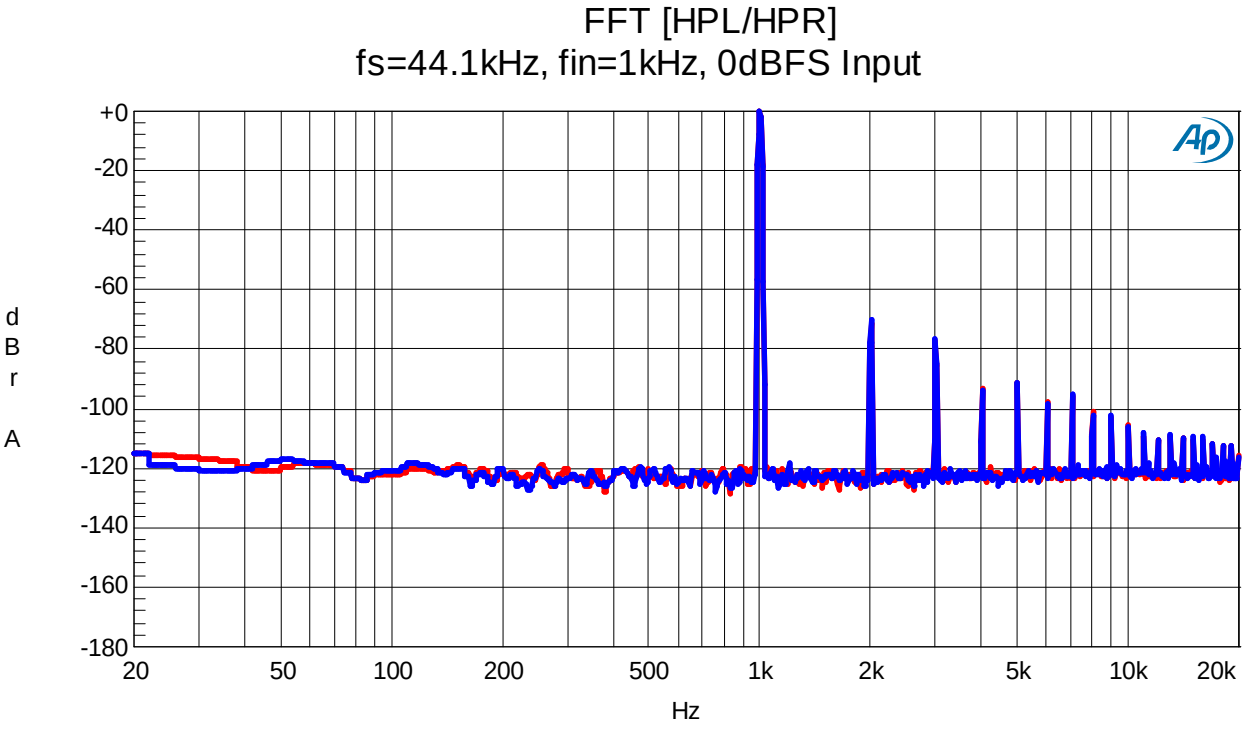



Figure 58. FFT (Input level= 0dBFS)

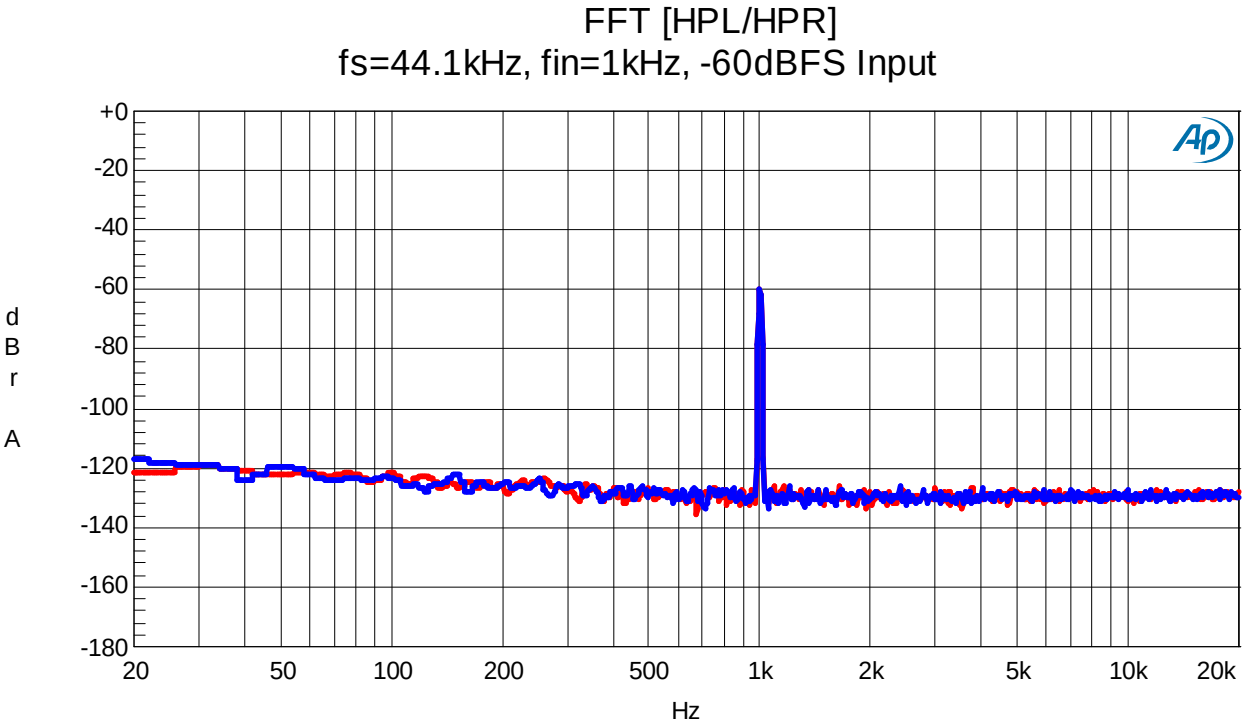



Figure 59. FFT (Input level= -60dBFS)

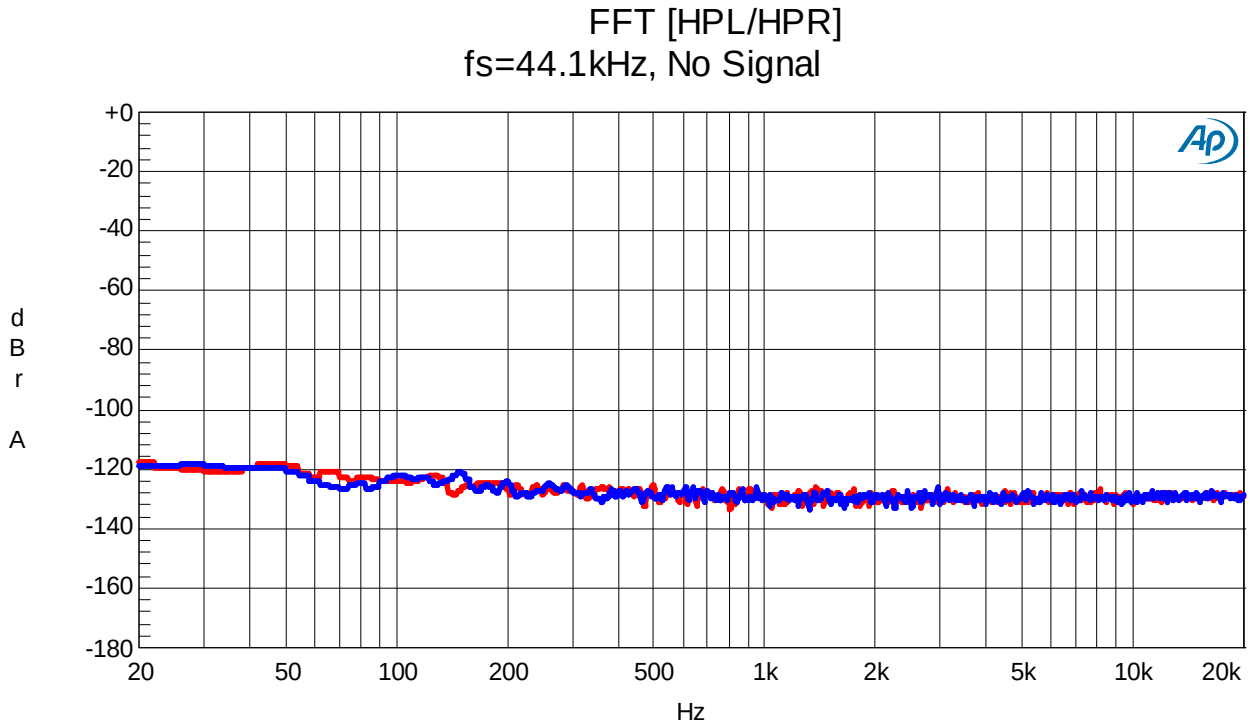



Figure 60. FFT (No signal)

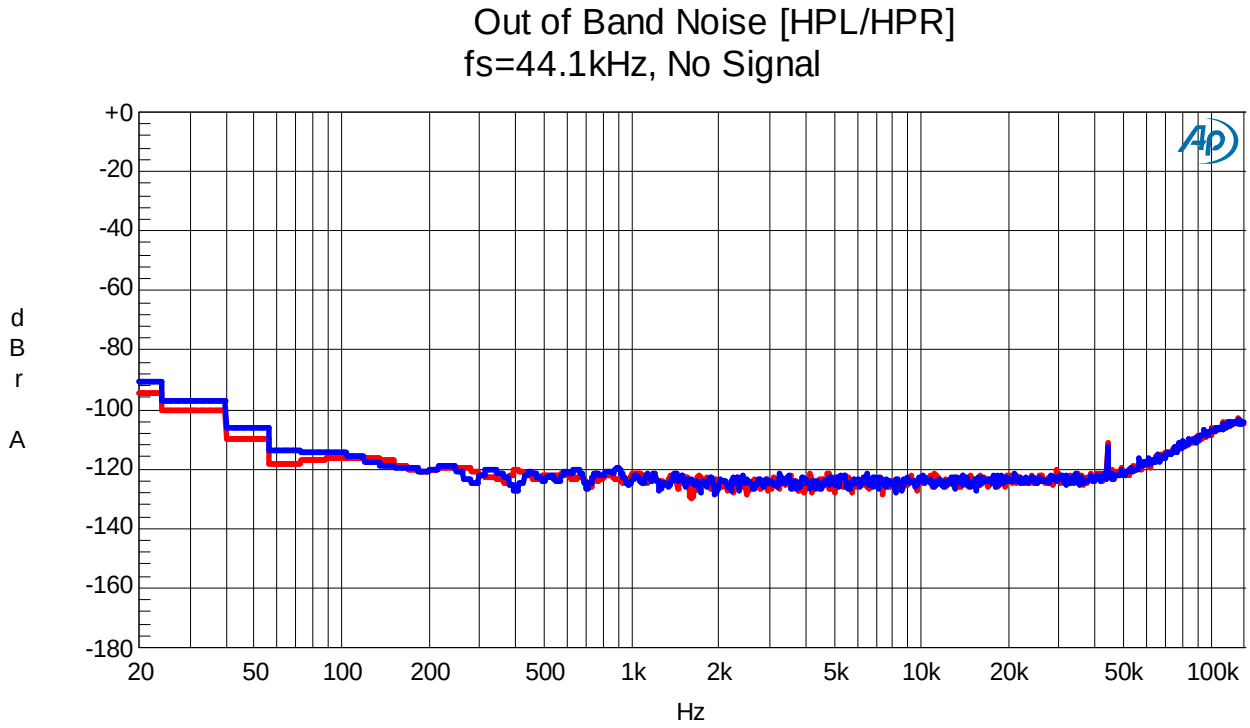



Figure 61. FFT (Out-of-band Noise)

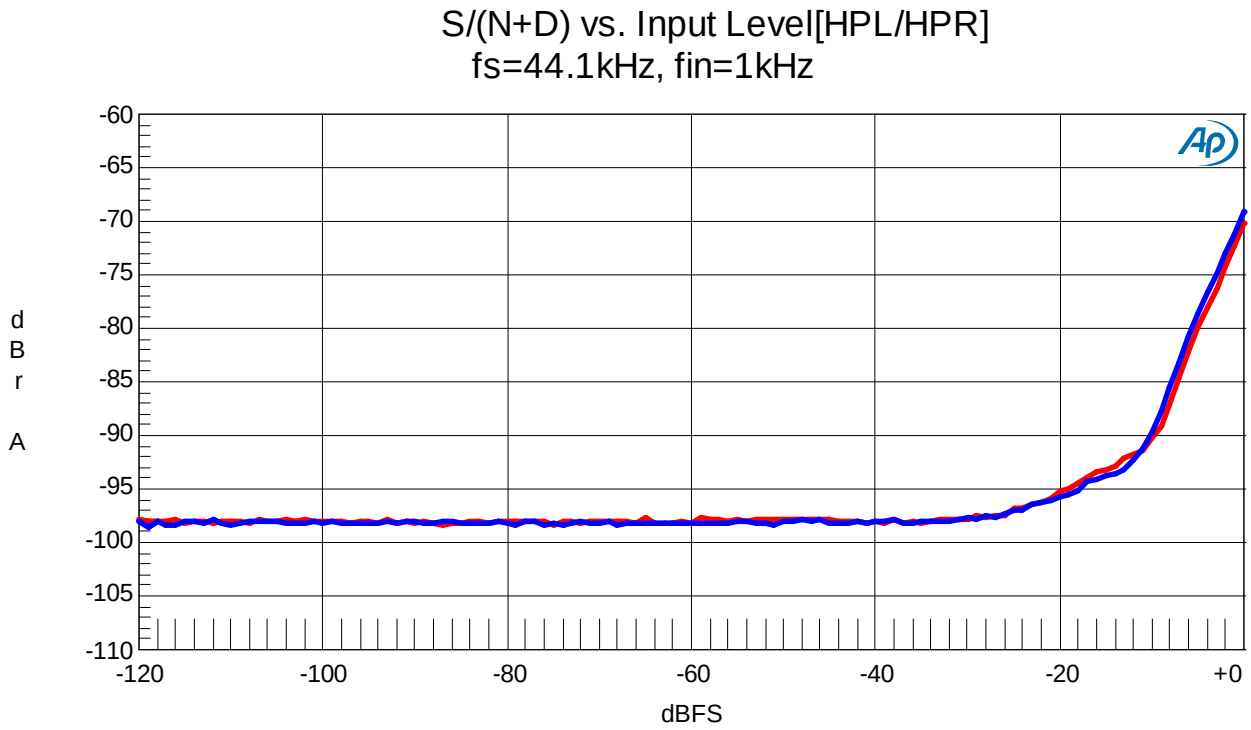



Figure 62. THD+N vs. Input Level

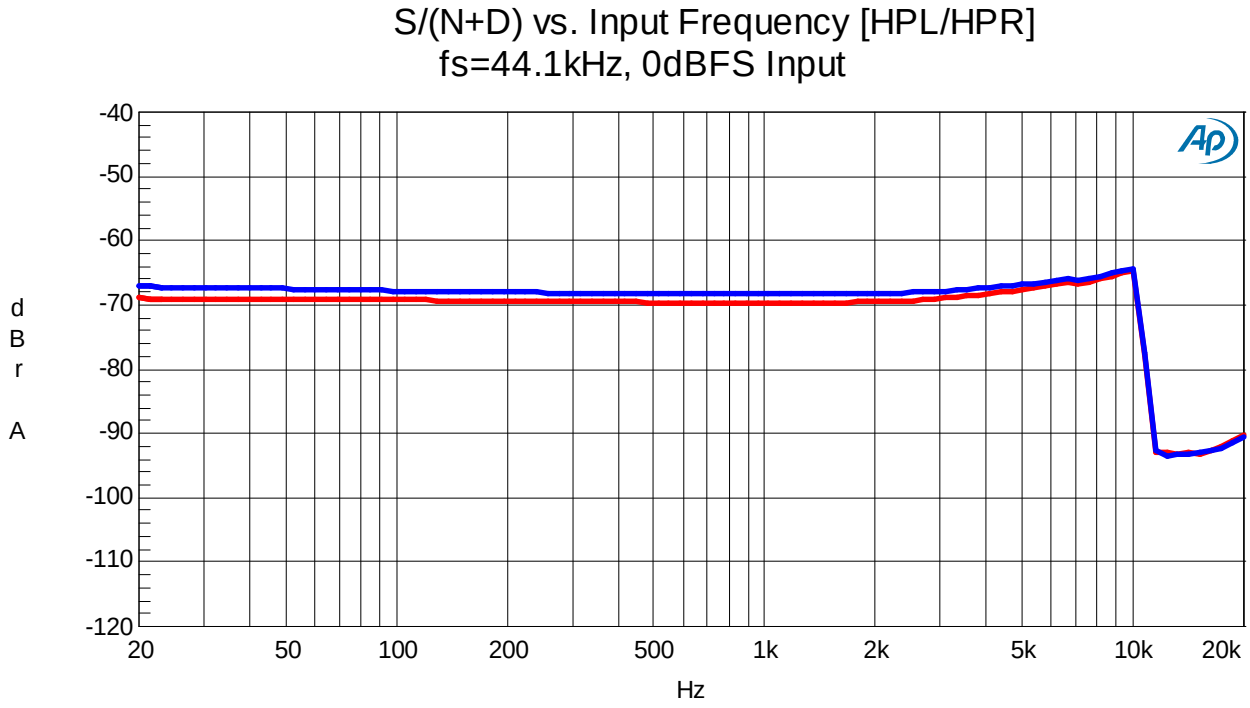



Figure 63. THD+N vs. Input Frequency

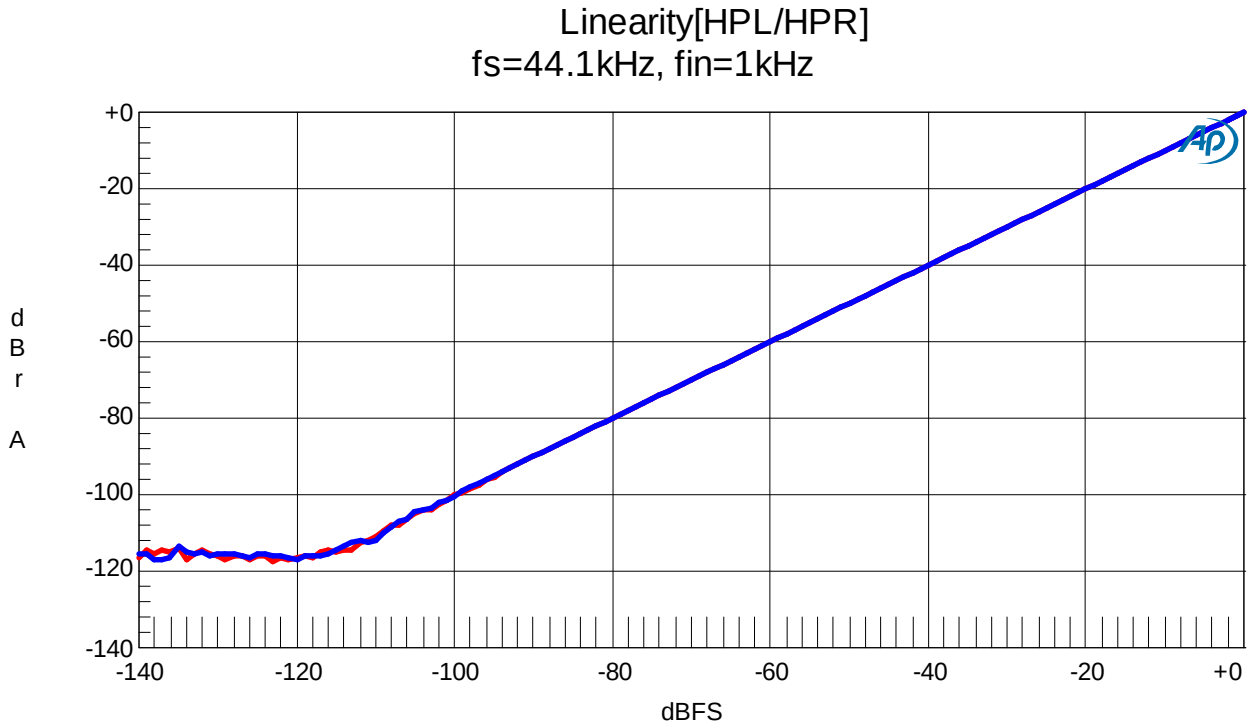



Figure 64. Linearity

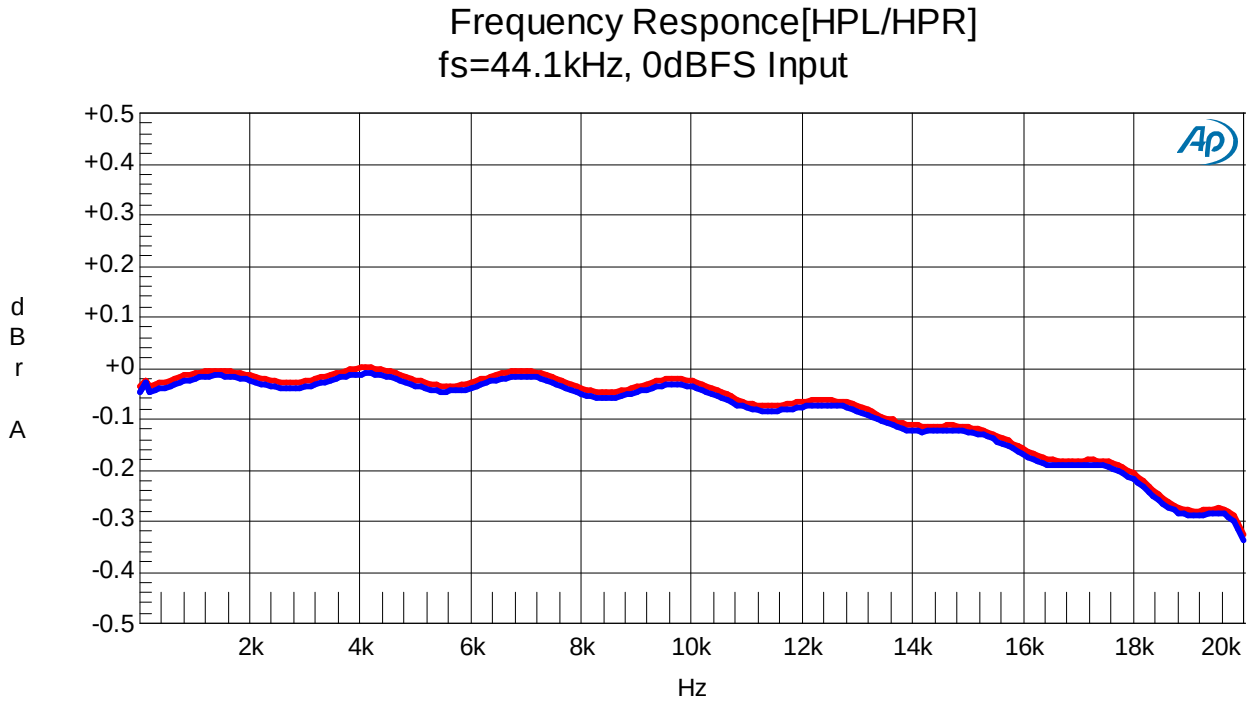



Figure 65. Frequency Response

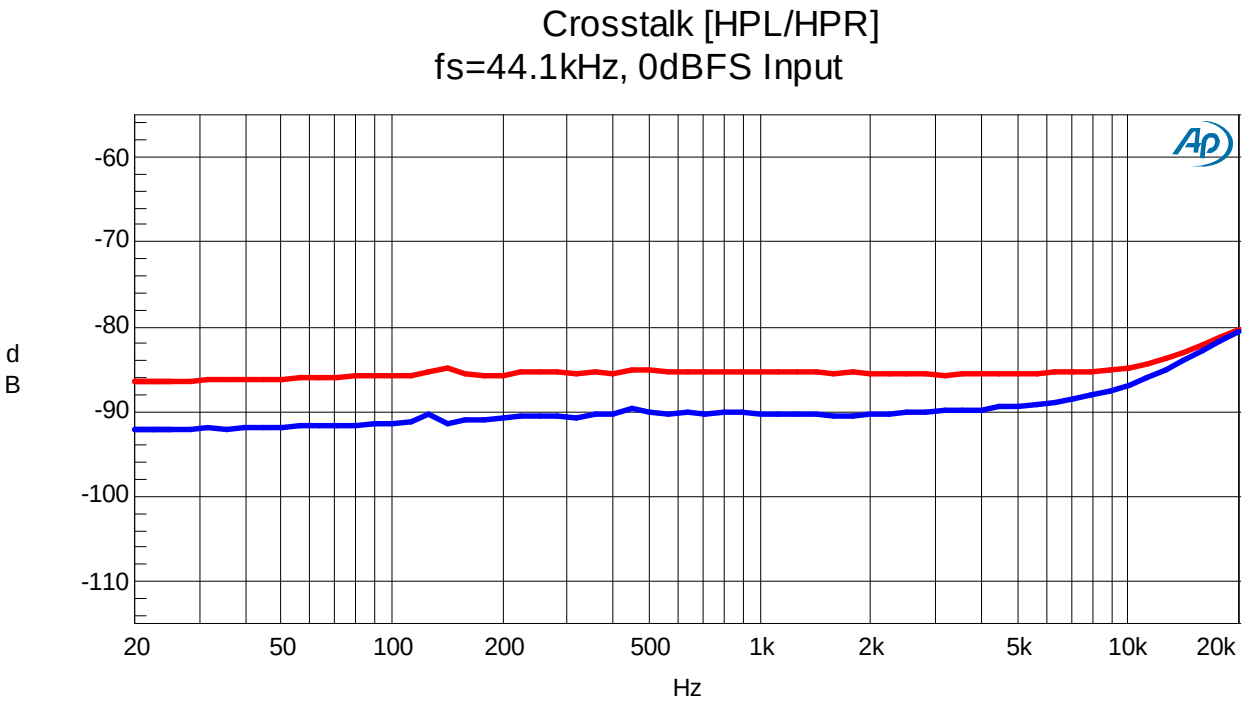



Figure 66. Crosstalk

**4. DAC (DAC→ HPL/HPR)**
**[fs=96kHz]**

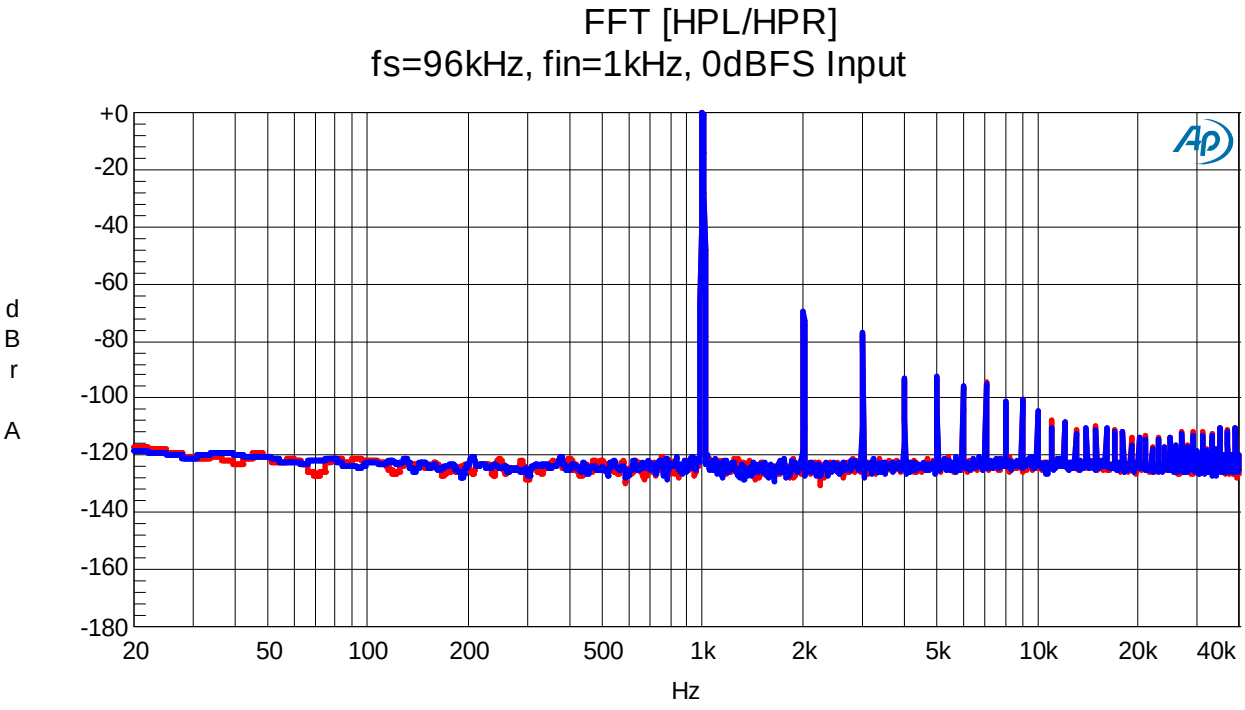



Figure 67. FFT (Input level= 0dBFS)

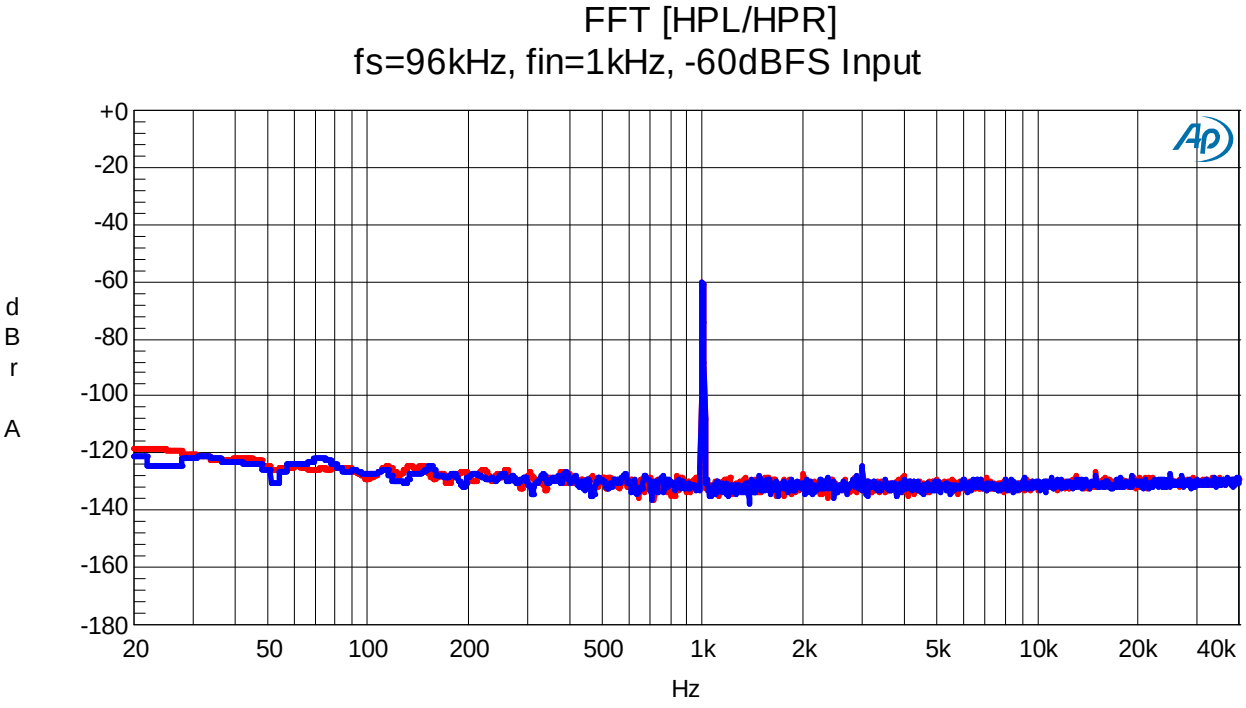



Figure 68. FFT (Input level= -60dBFS)

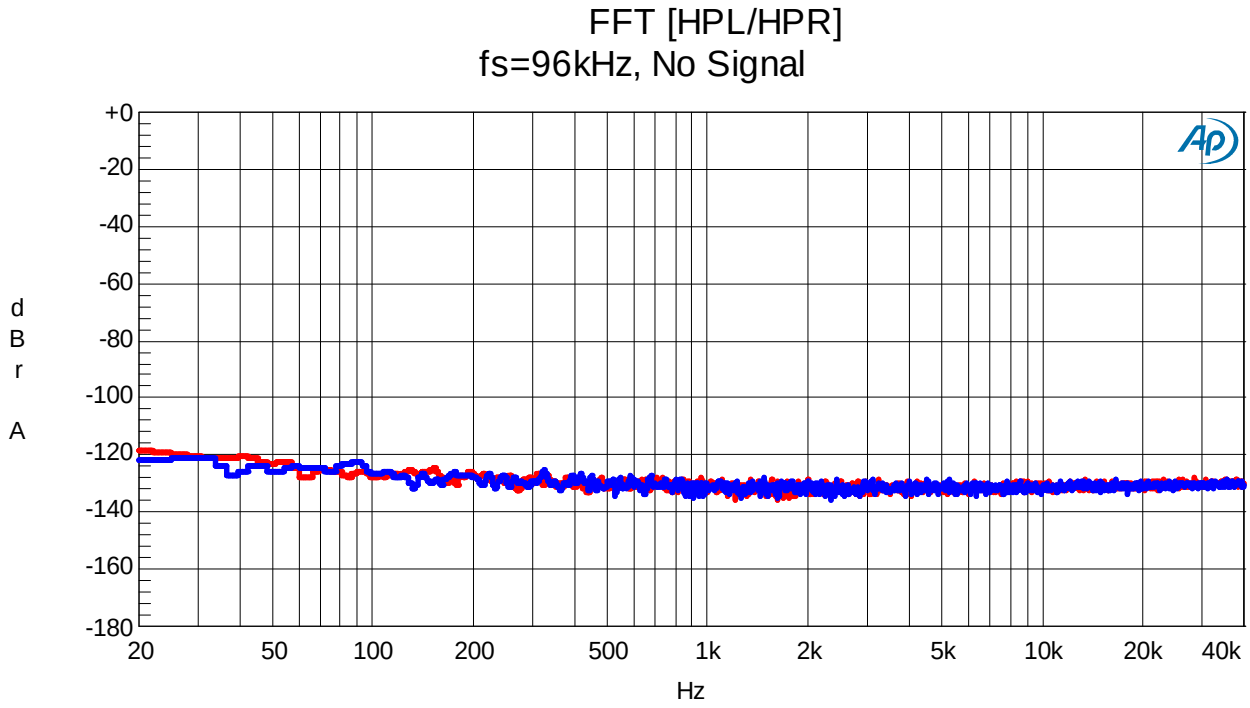



Figure 69. FFT (No signal)

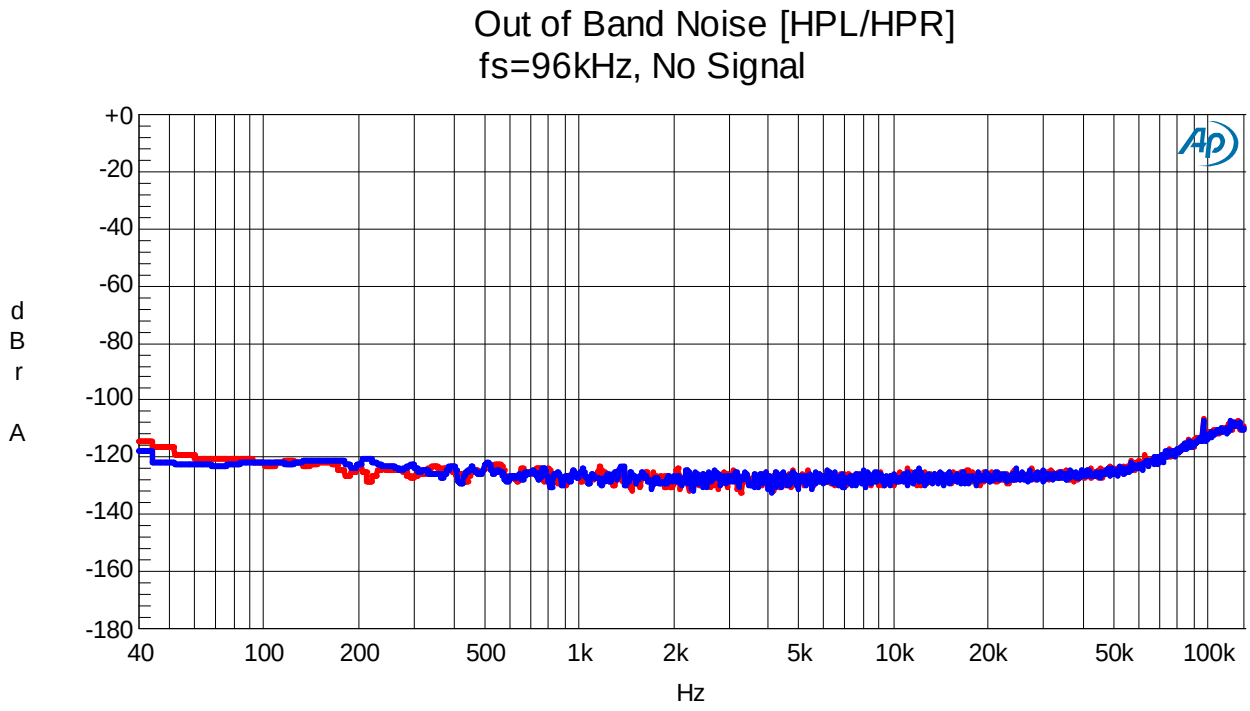



Figure 70. FFT (Out-of-band Noise)

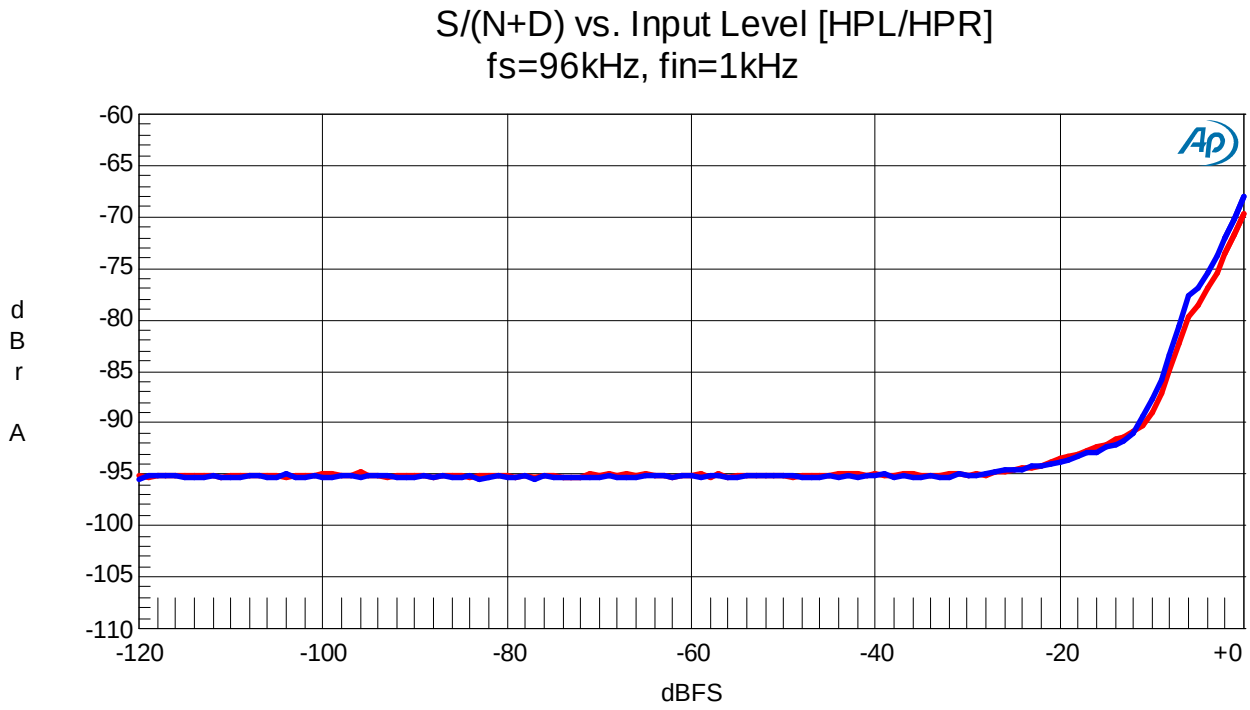



Figure 71. THD+N vs. Input Level

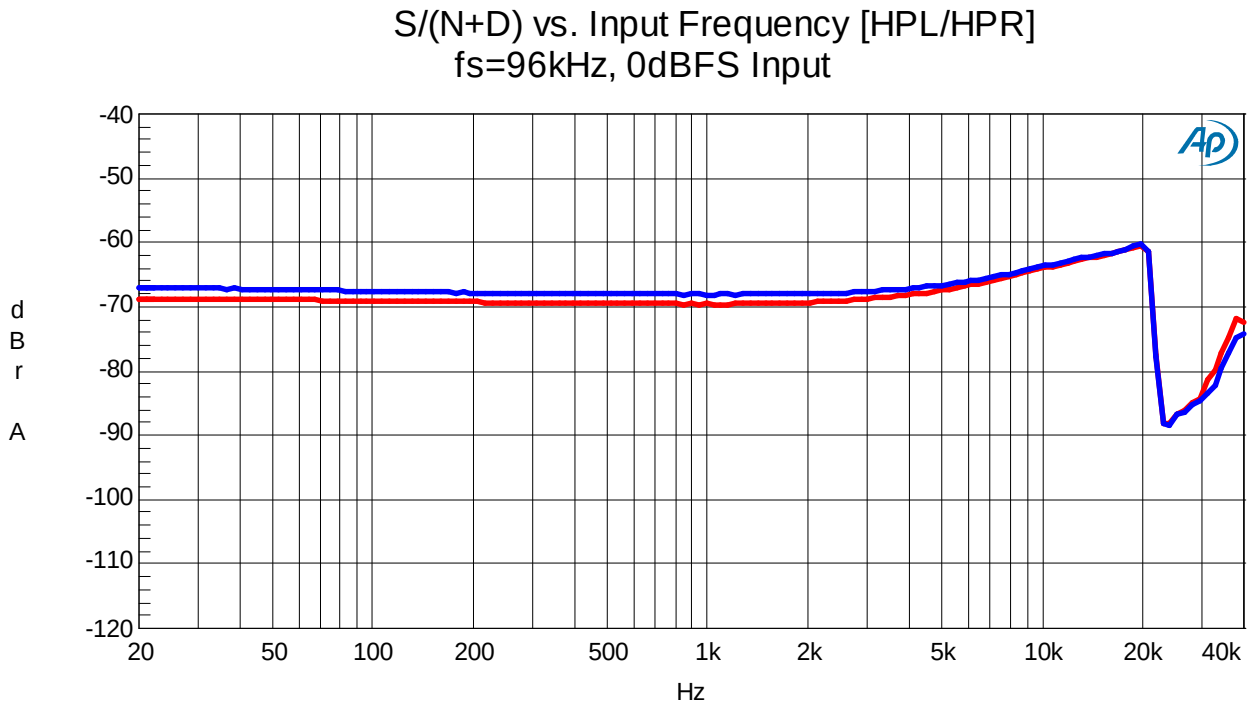



Figure 72. THD+N vs. Input Frequency

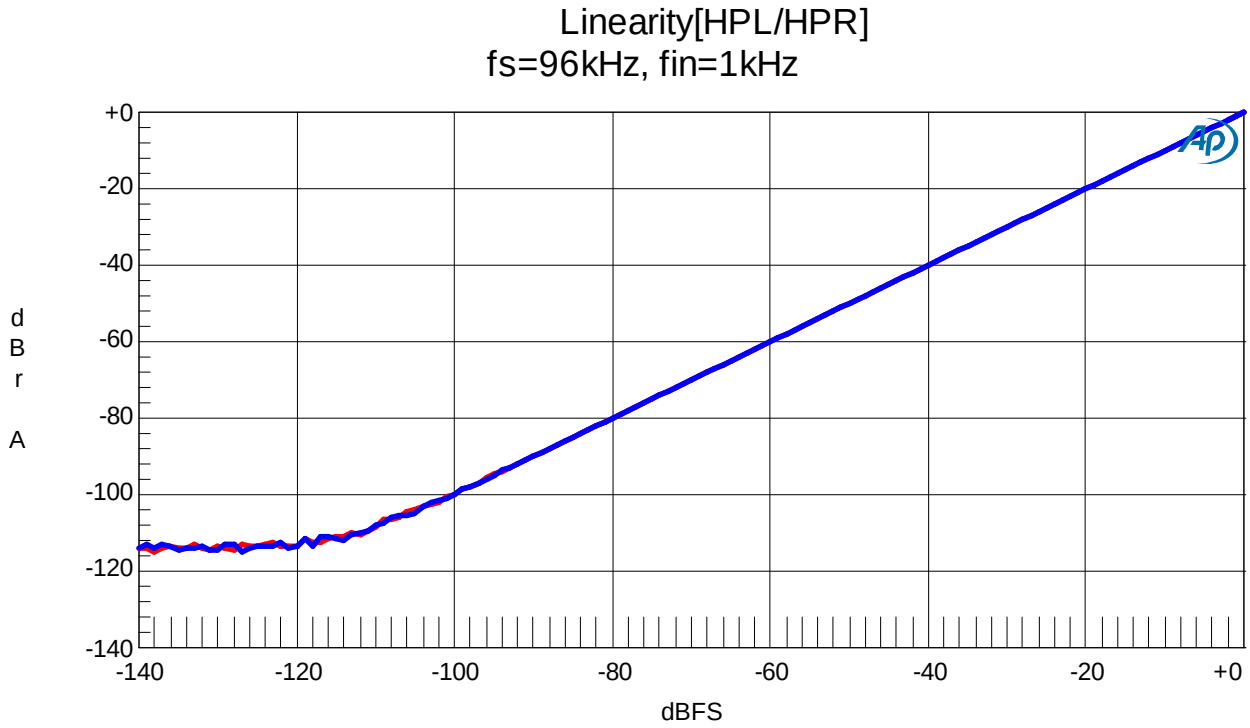



Figure 73. Linearity

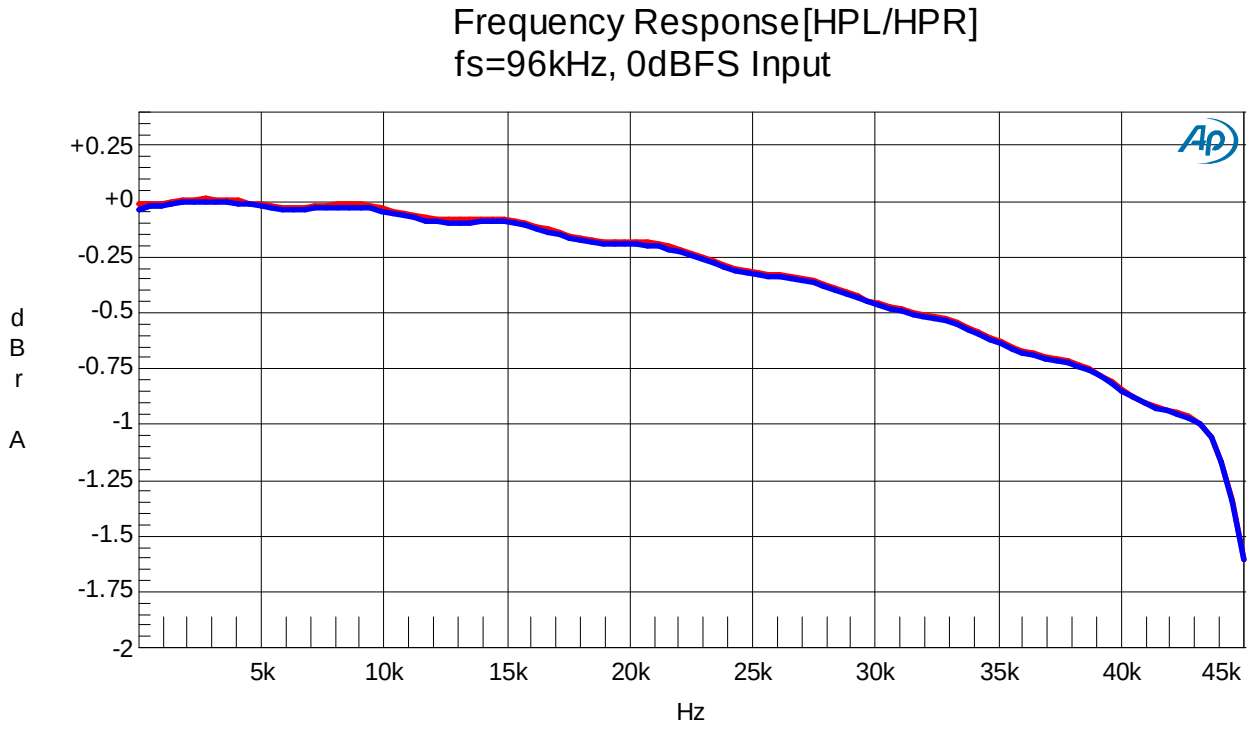



Figure 74. Frequency Response

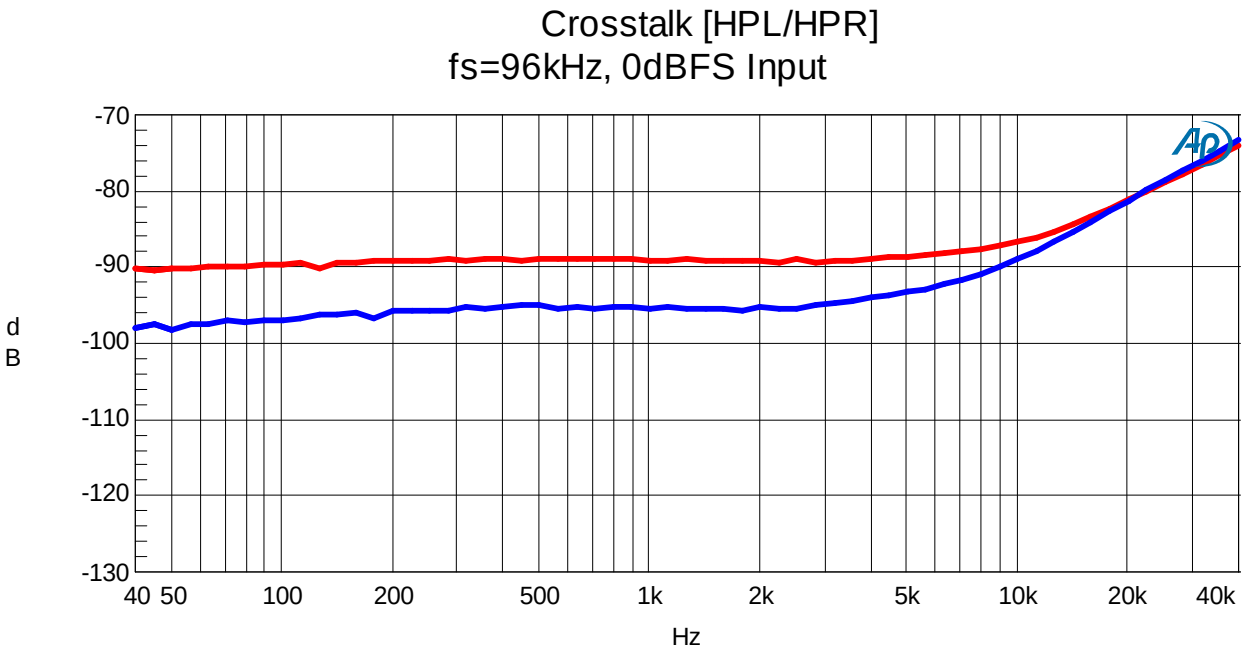



Figure 75. Crosstalk

**5. DAC (DAC→ SPK)**
**[fs=44.1kHz]**

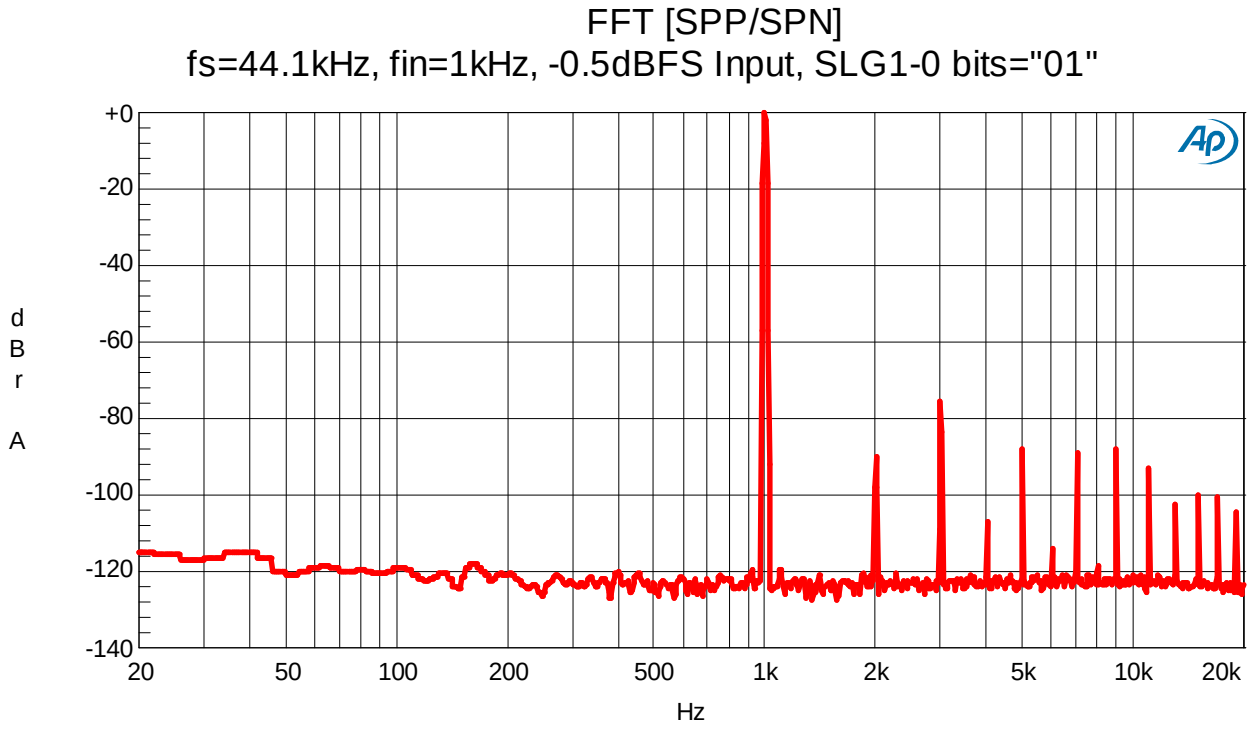



Figure 76. FFT (Input level= -0.5dBFS)

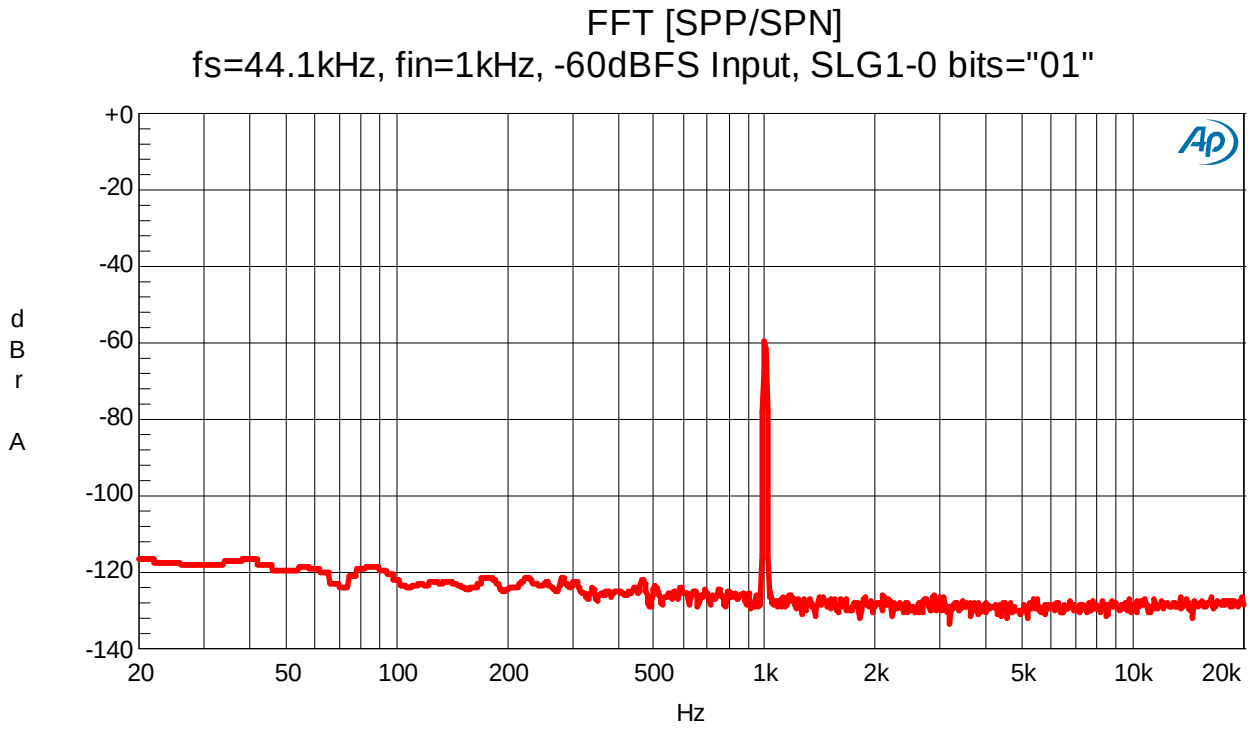



Figure 77. FFT (Input level= -60dBFS)

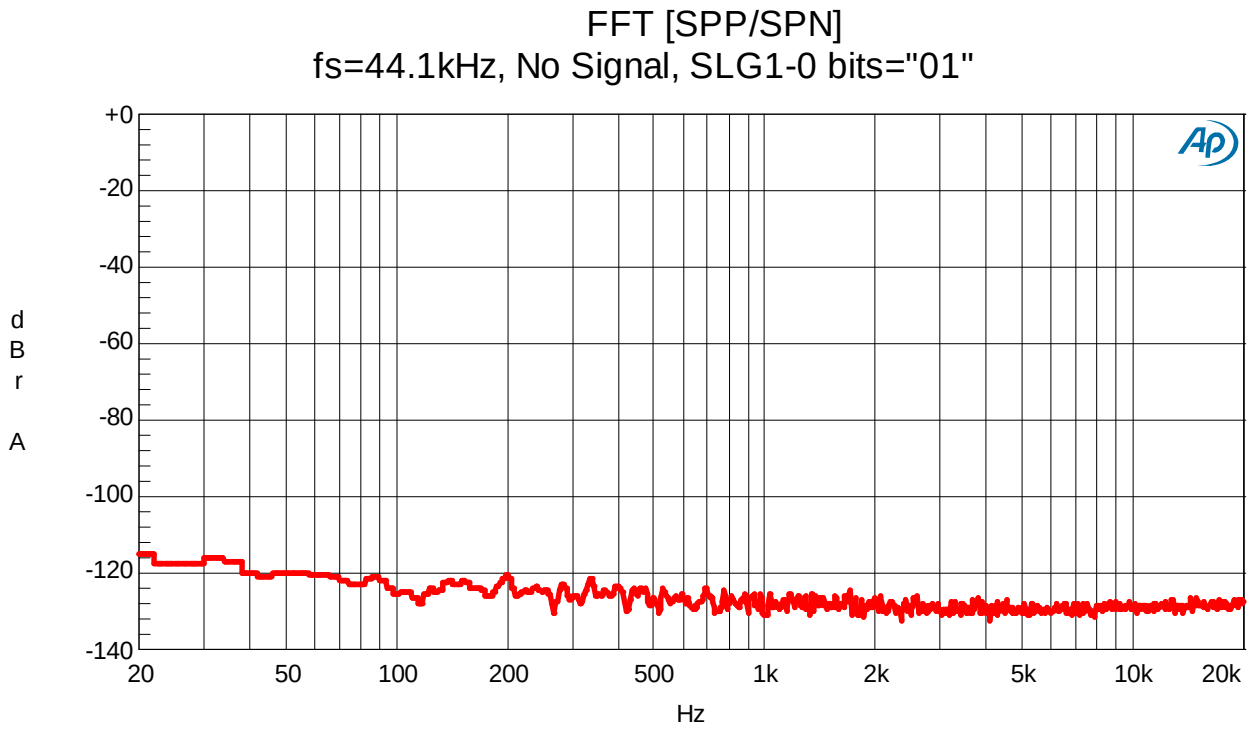



Figure 78. FFT (No Signal)

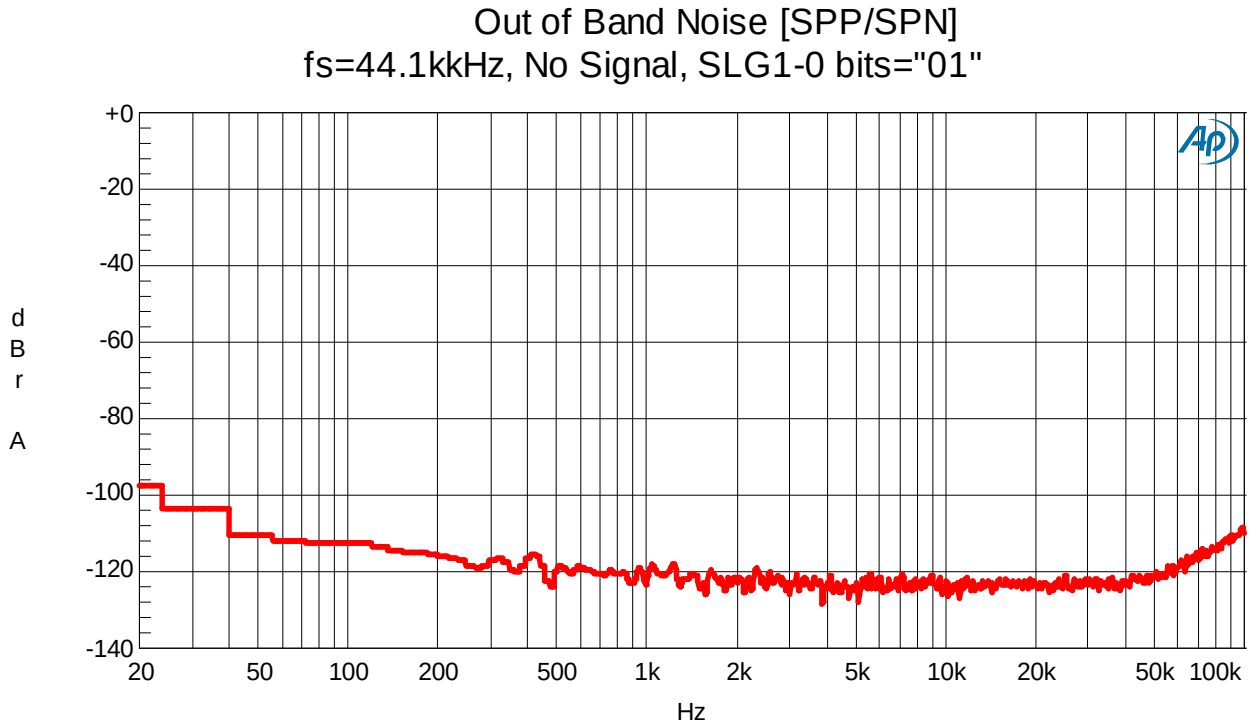



Figure 79. FFT (No Signal)

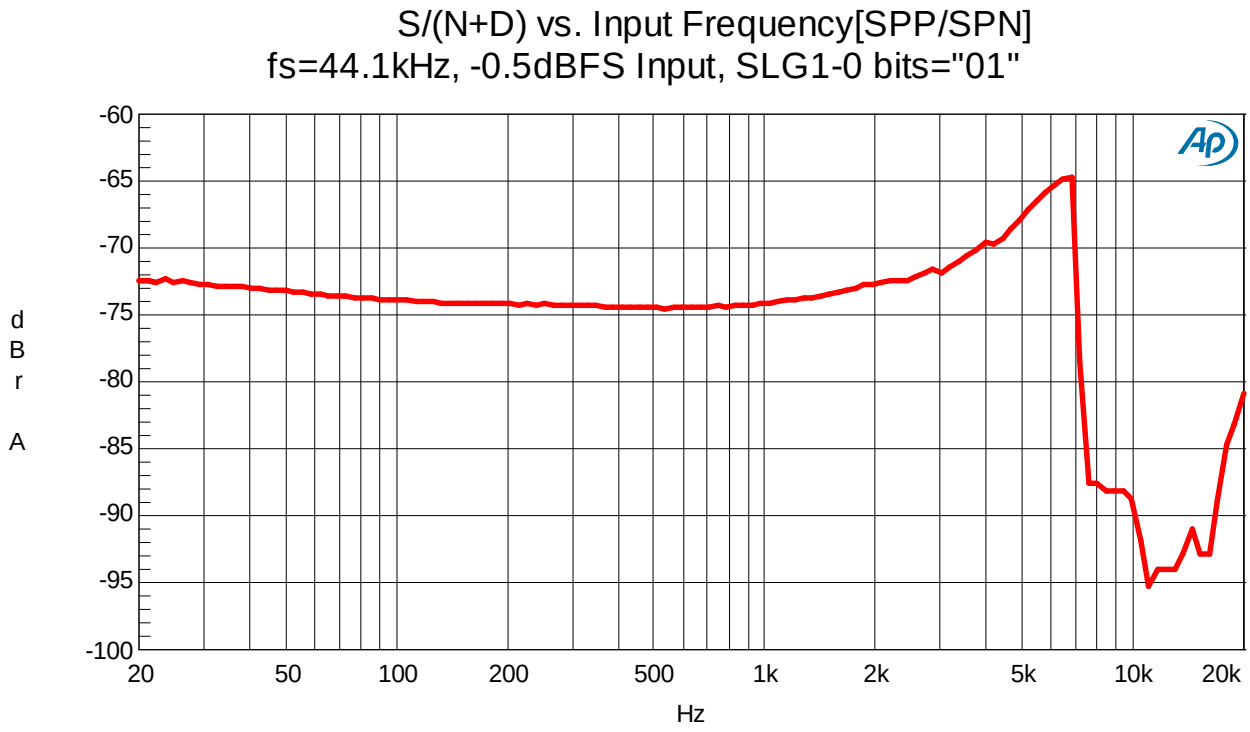



Figure 80. THD+N vs. Input Frequency

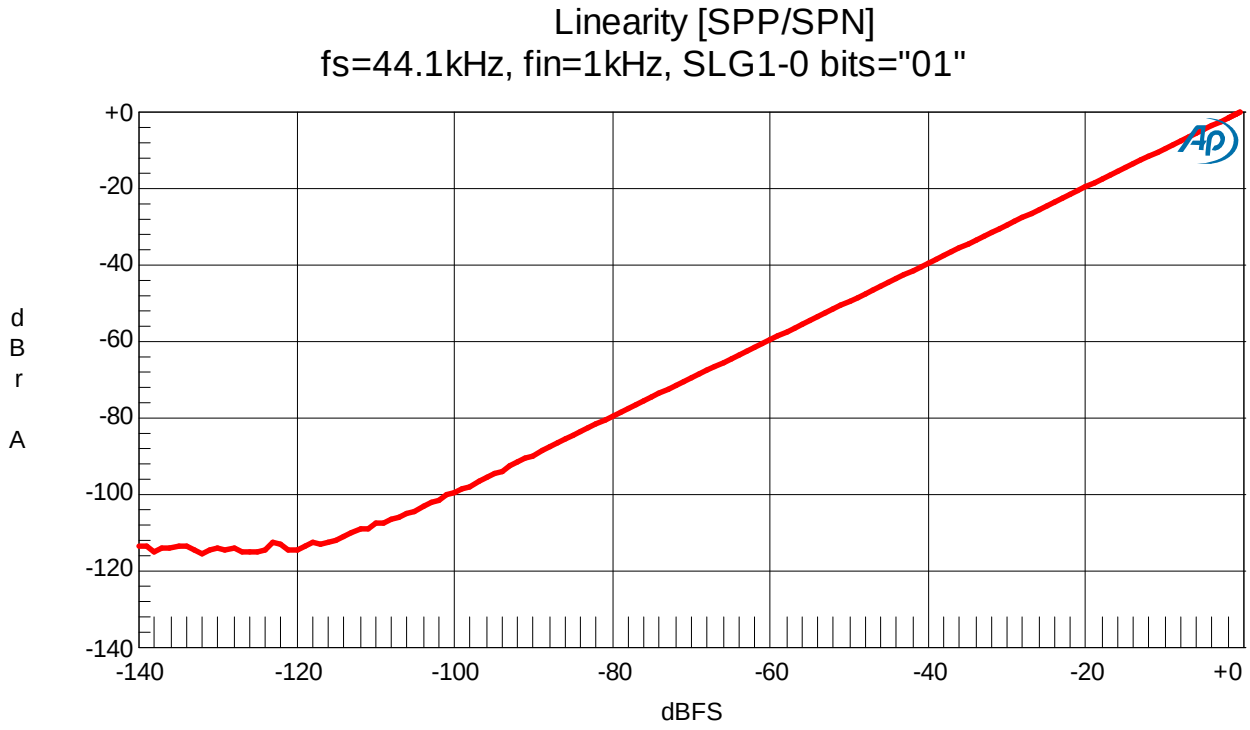



Figure 81. Linearity

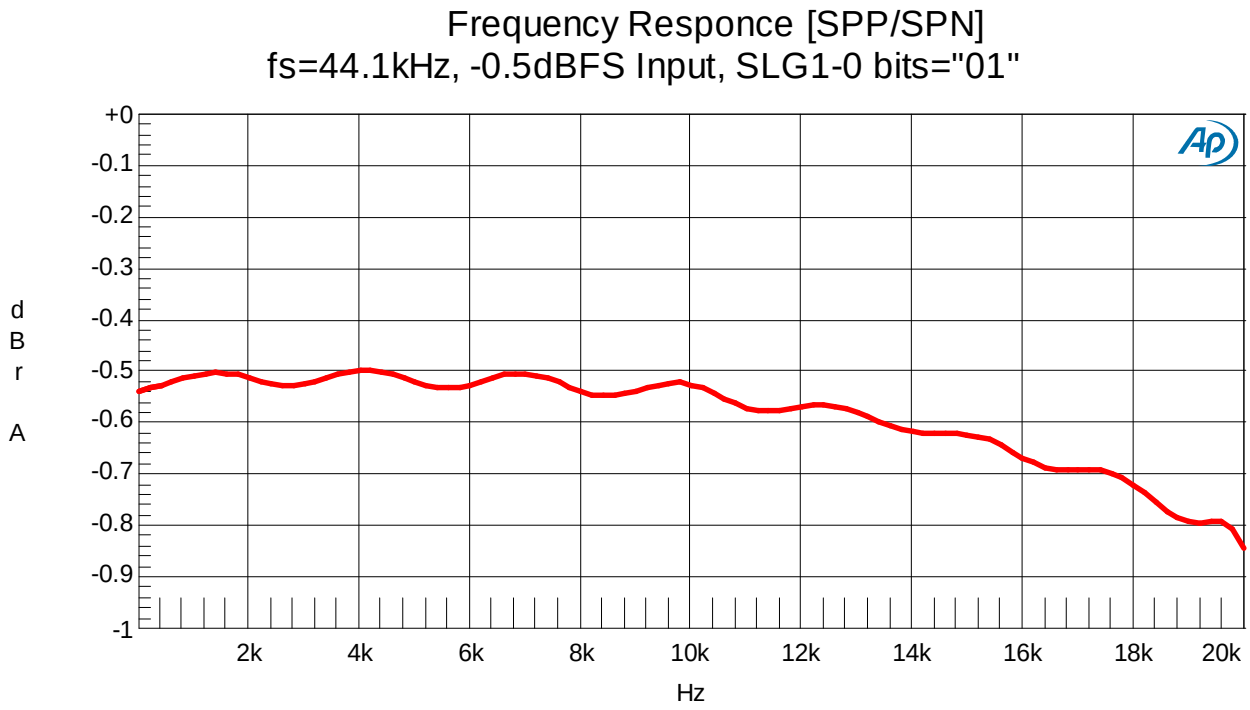



Figure 82. Frequency Response

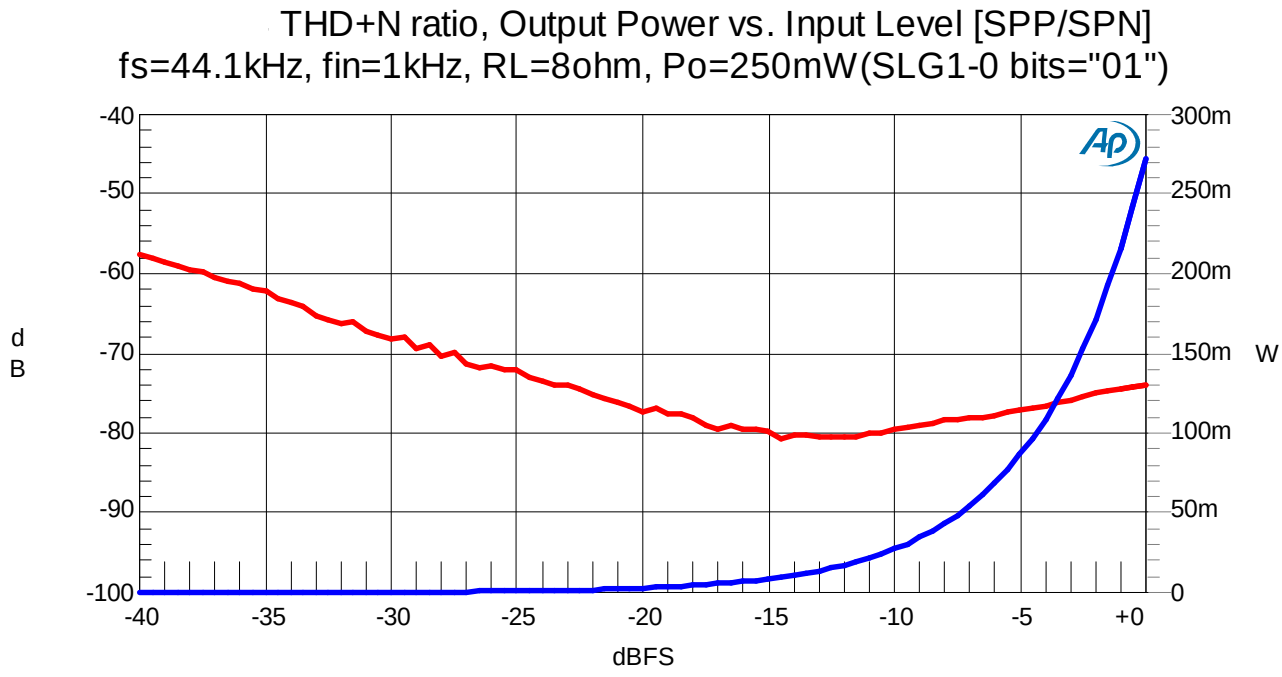



Figure 83. THD+N vs. Output Power

**6. DAC (DAC→ LOUT/ROUT)**
**[fs=44.1kHz]**

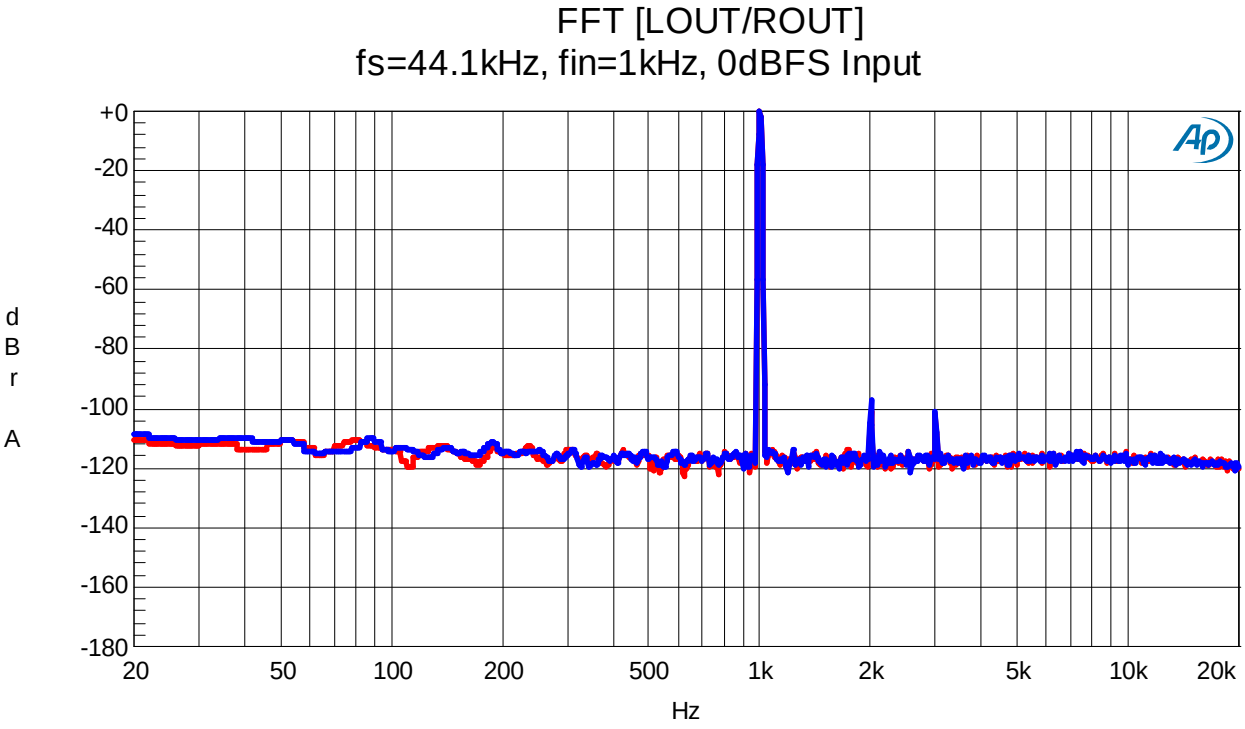



Figure 84. FFT (Input level= 0dBFS)

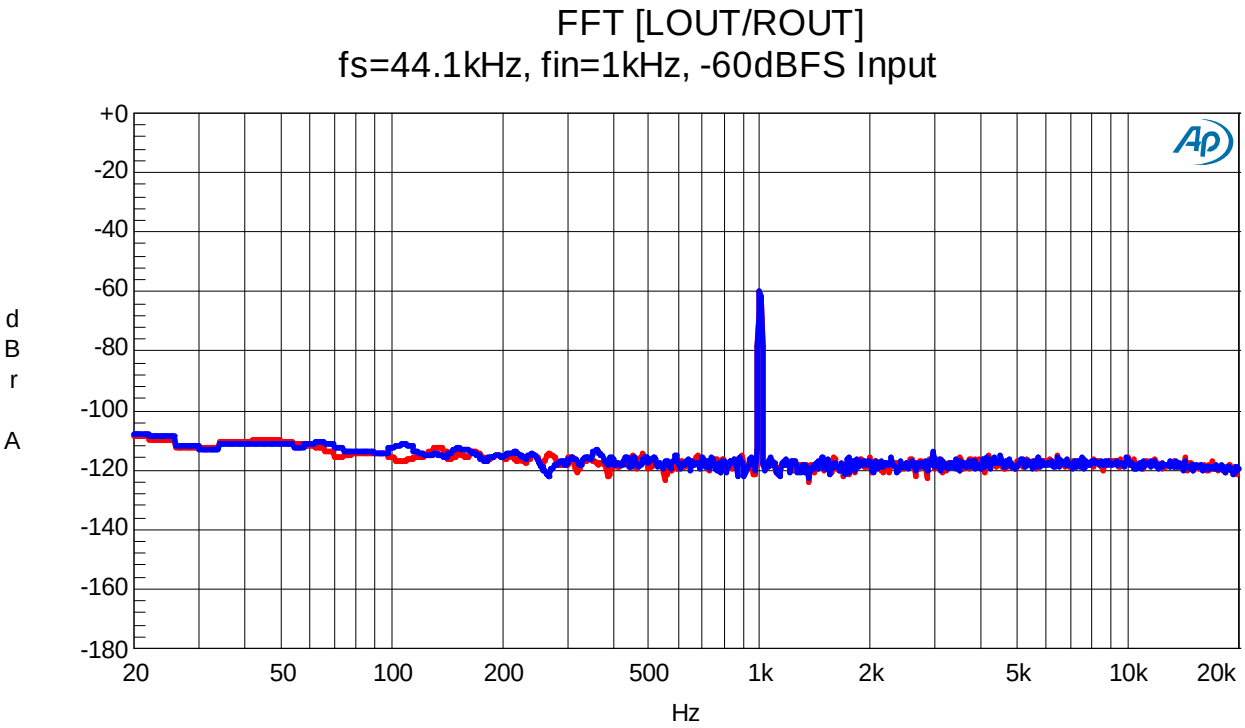



Figure 85. FFT (Input level= -60dBFS)

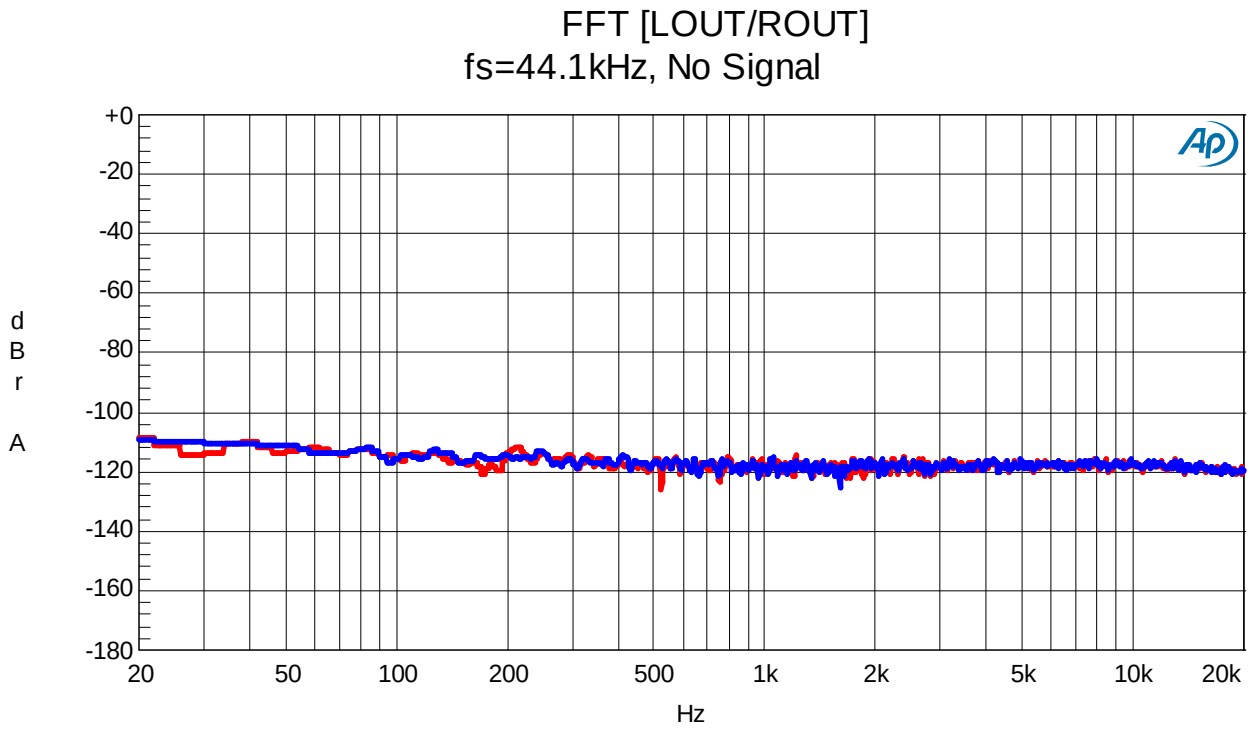



Figure 86. FFT (No signal)

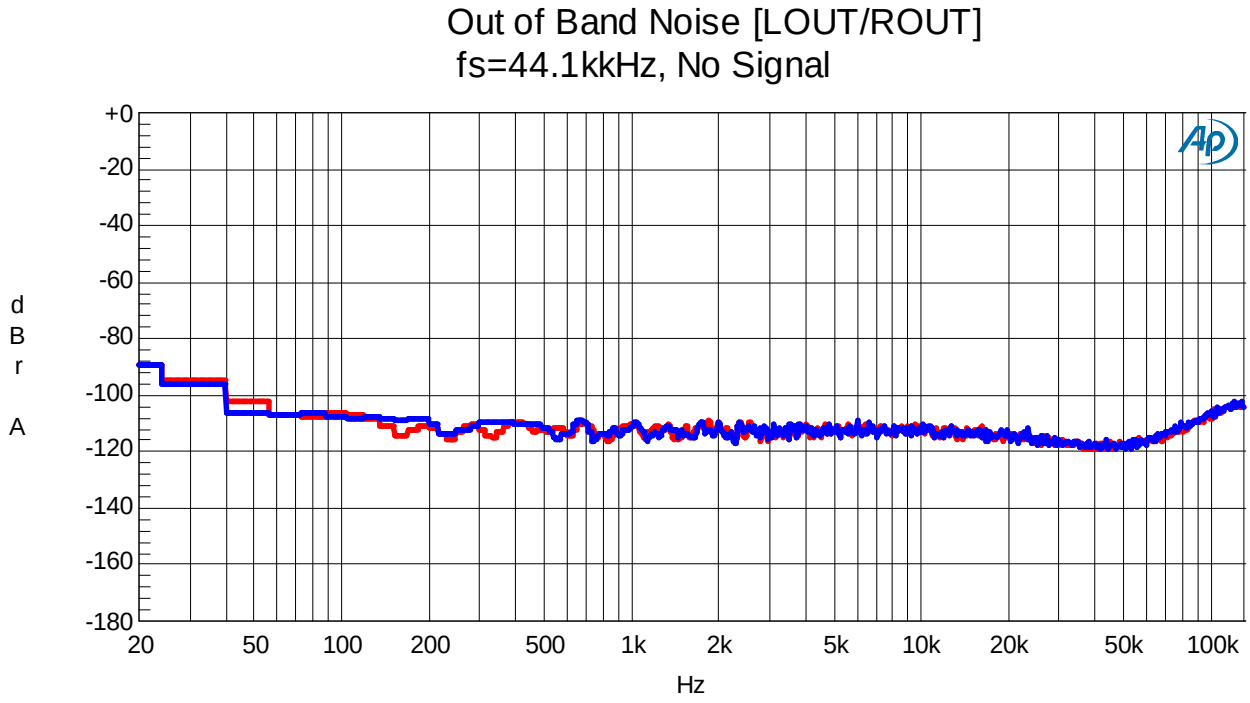



Figure 87. FFT (Out-of-band Noise)

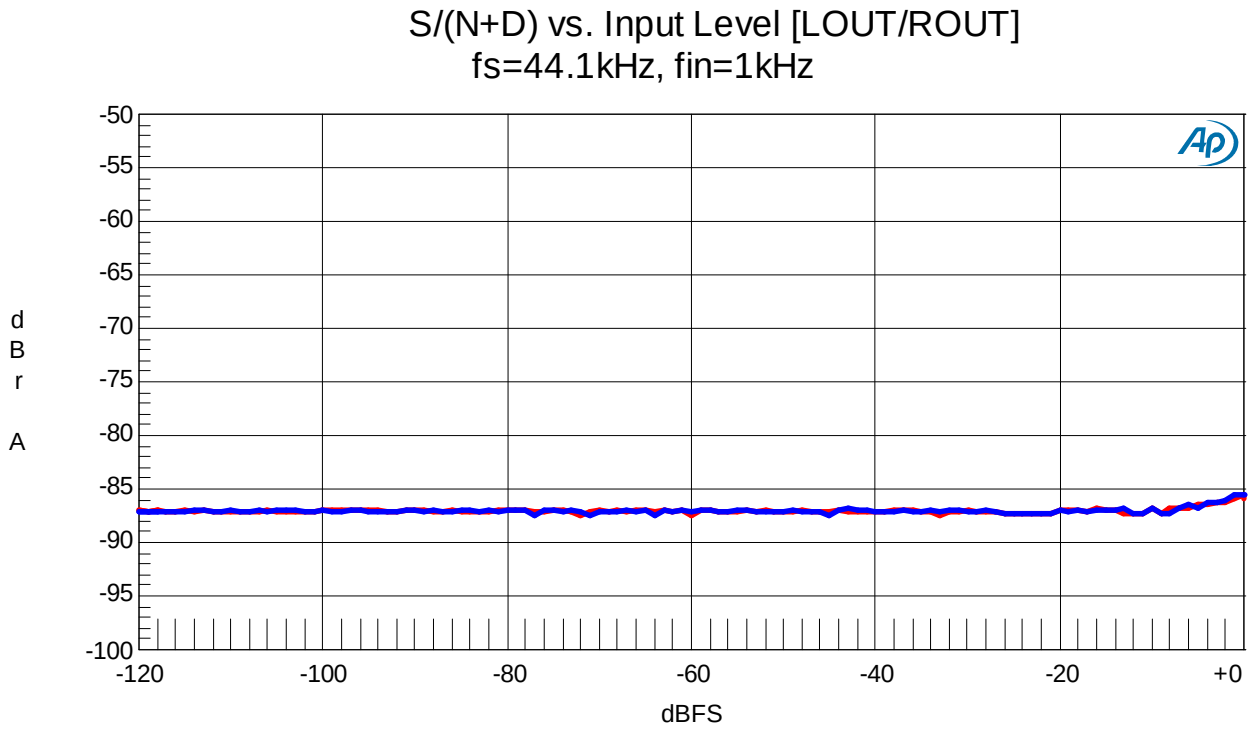



Figure 88. THD+N vs. Input Level

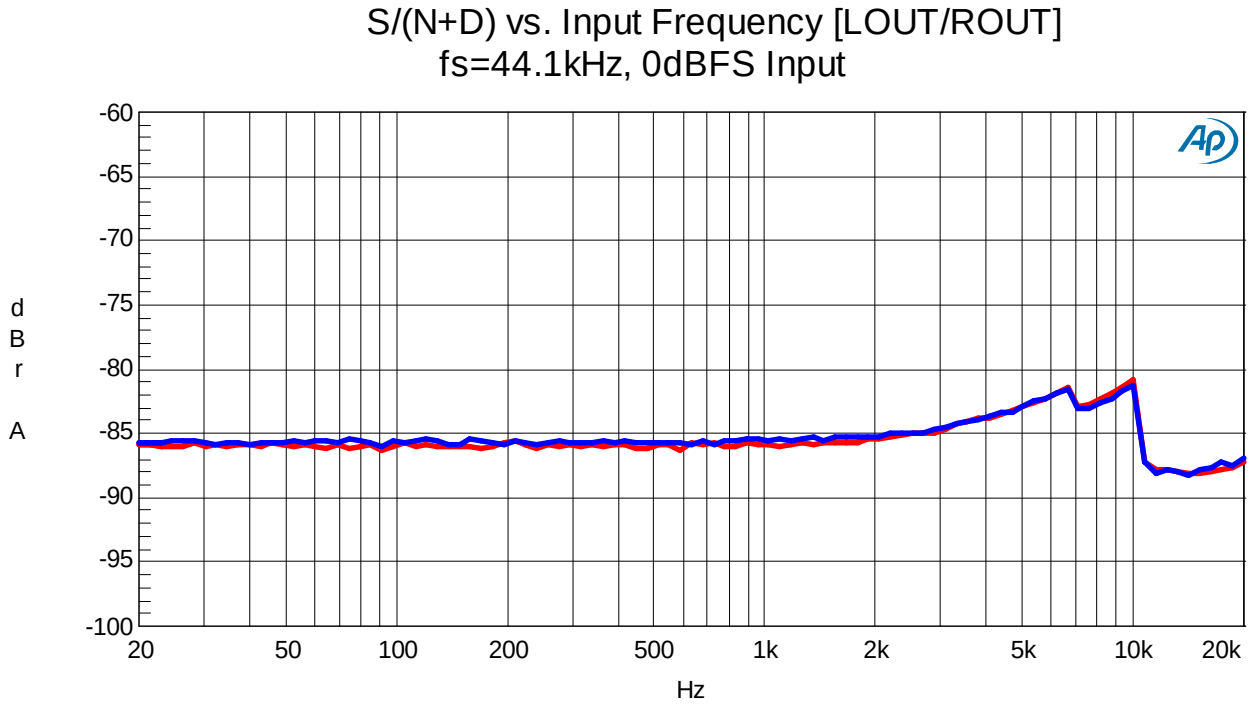



Figure 89. THD+N vs. Input Frequency

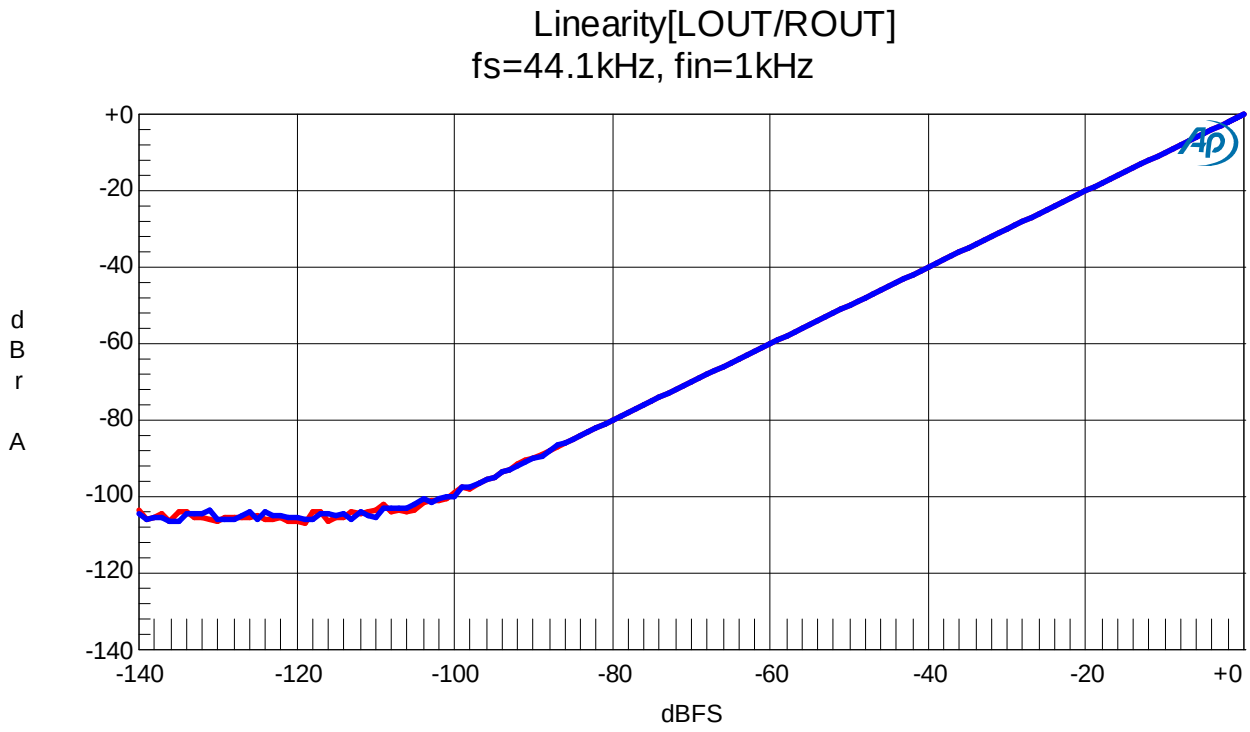



Figure 90. Linearity

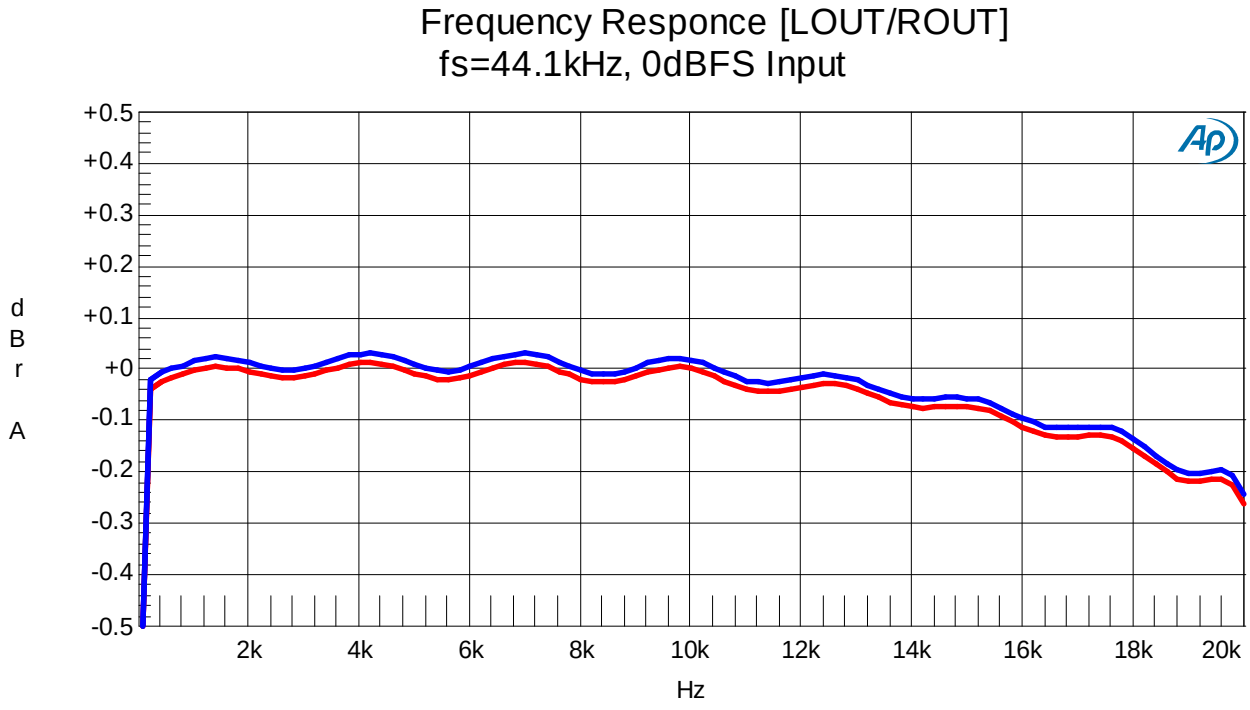



Figure 91. Frequency Response

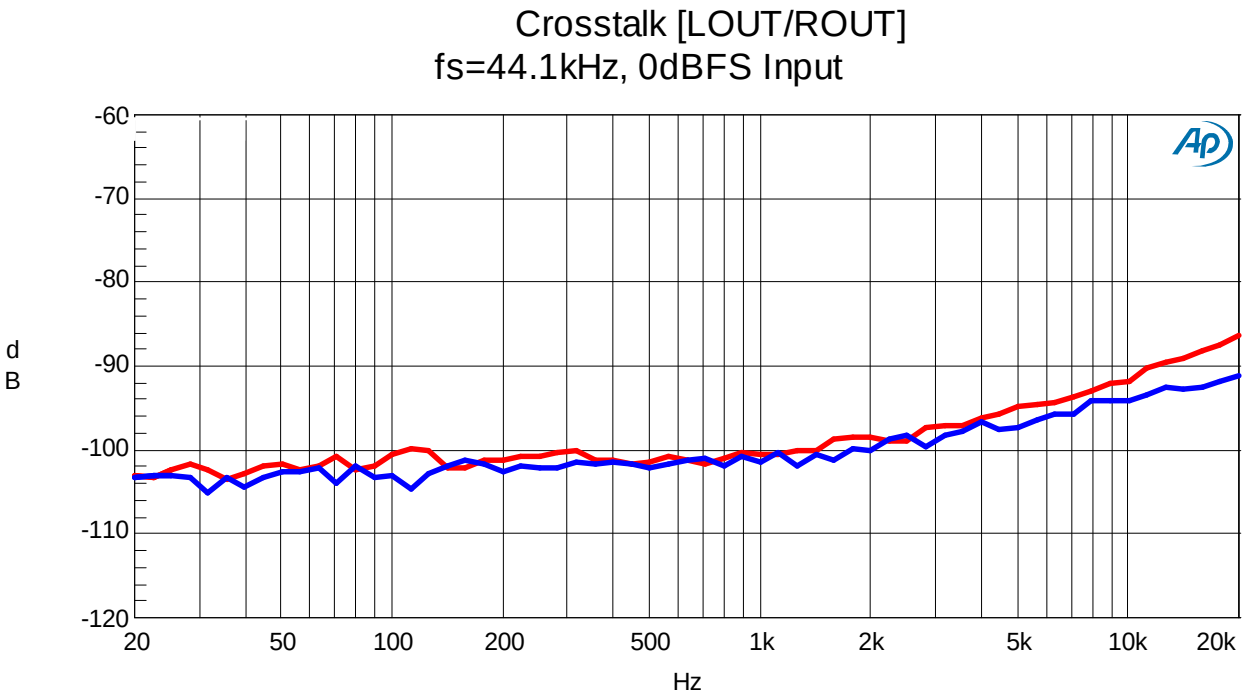



Figure 92. Crosstalk

**7. DAC (DAC→ LOUT/ROUT)**
**[fs=96kHz]**

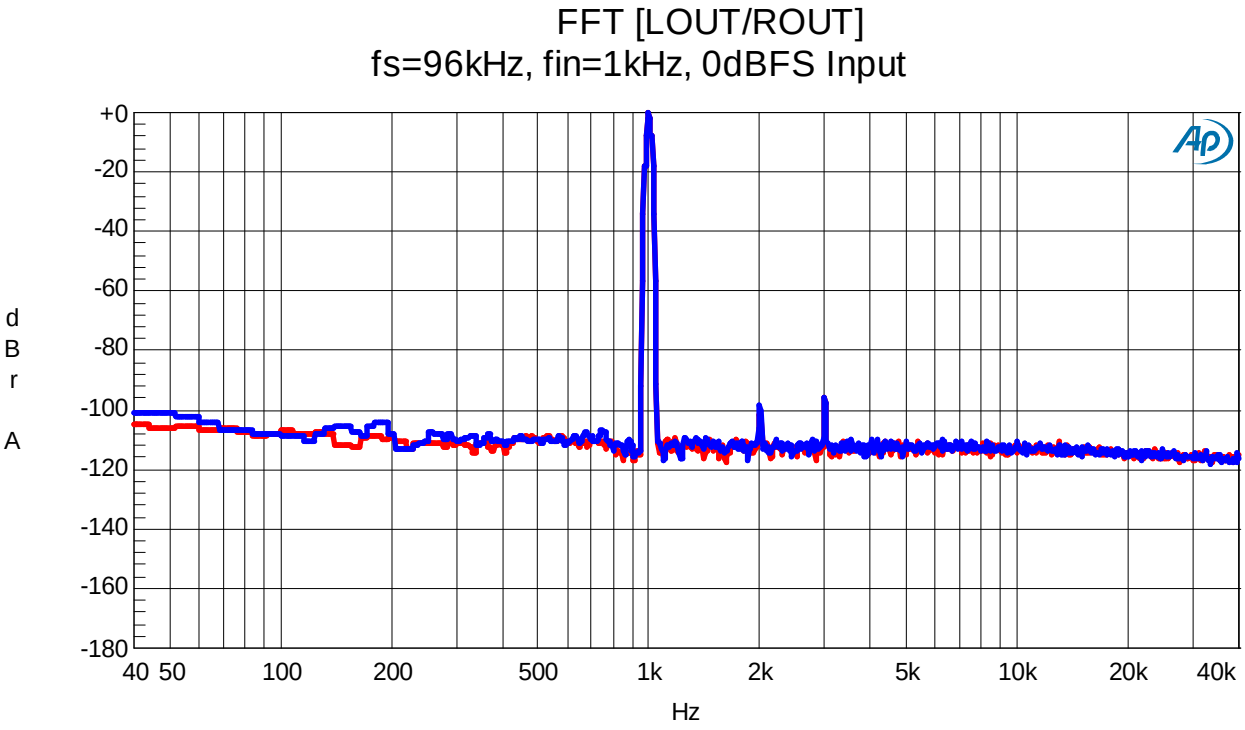



Figure 93. FFT (Input level= 0dBFS)

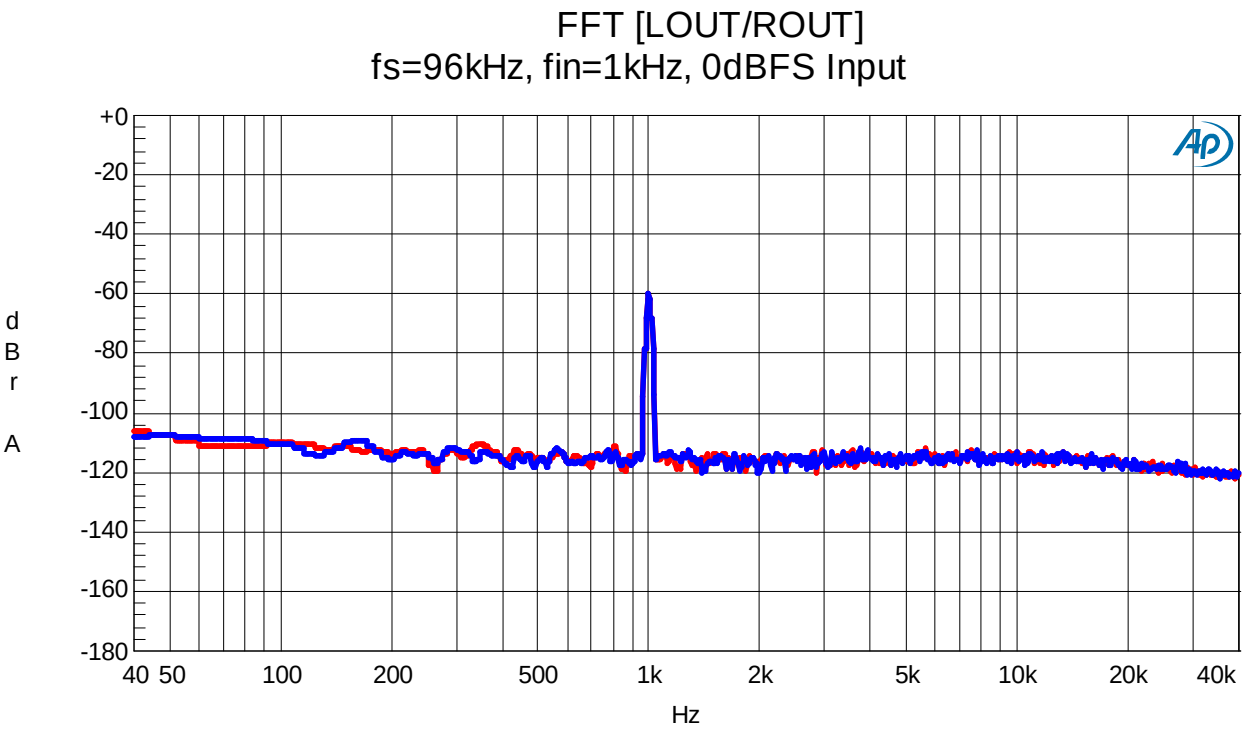



Figure 94. FFT (Input level= -60dBFS)

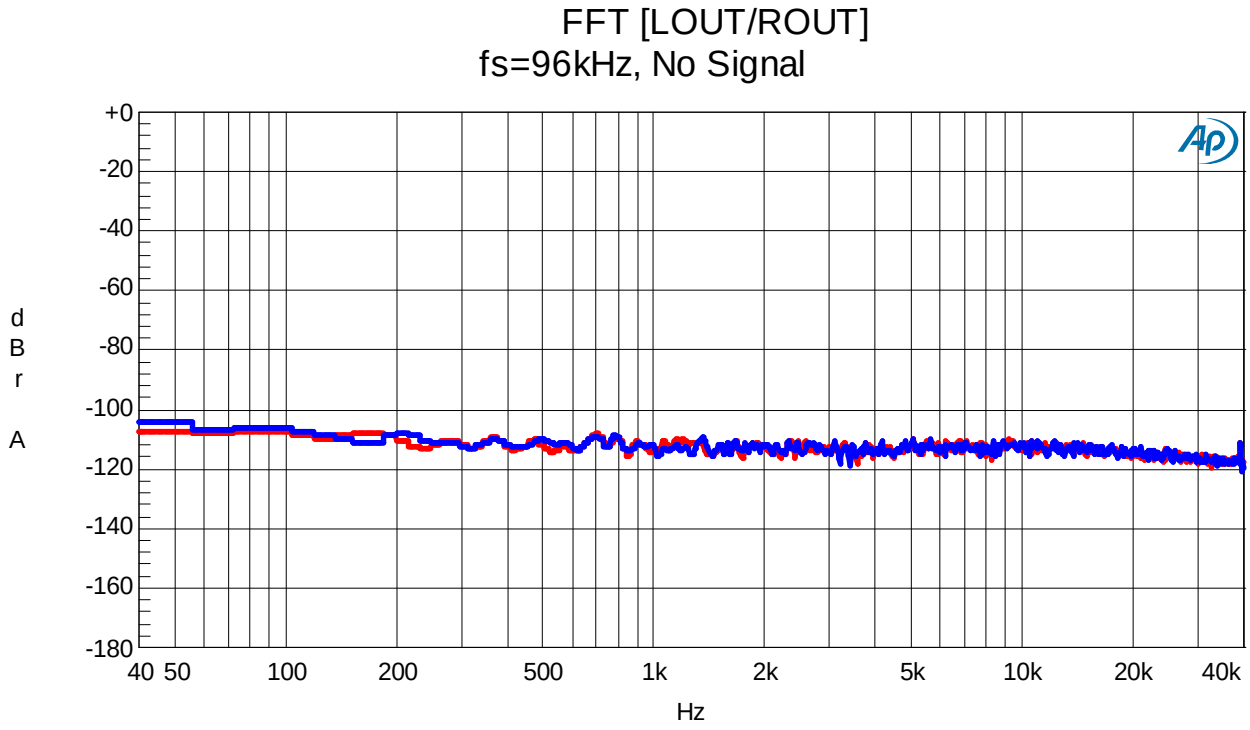



Figure 95. FFT (No signal)

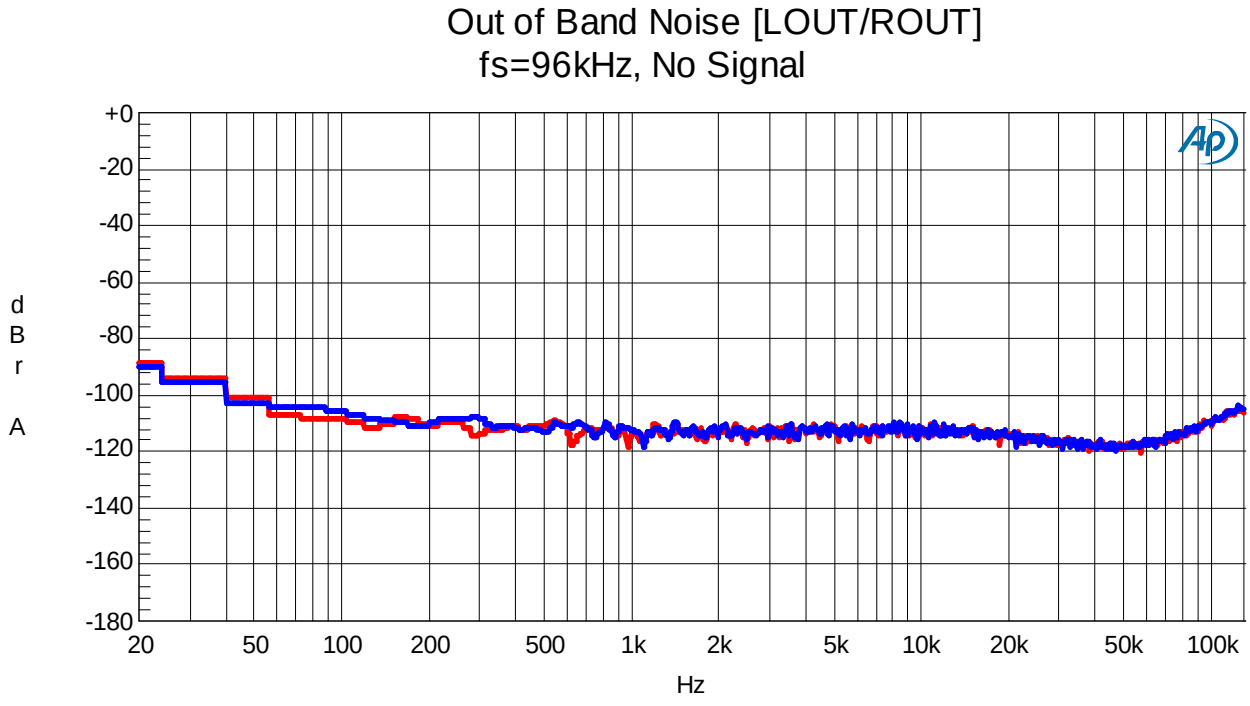



Figure 96. FFT (Out-of-band Noise)

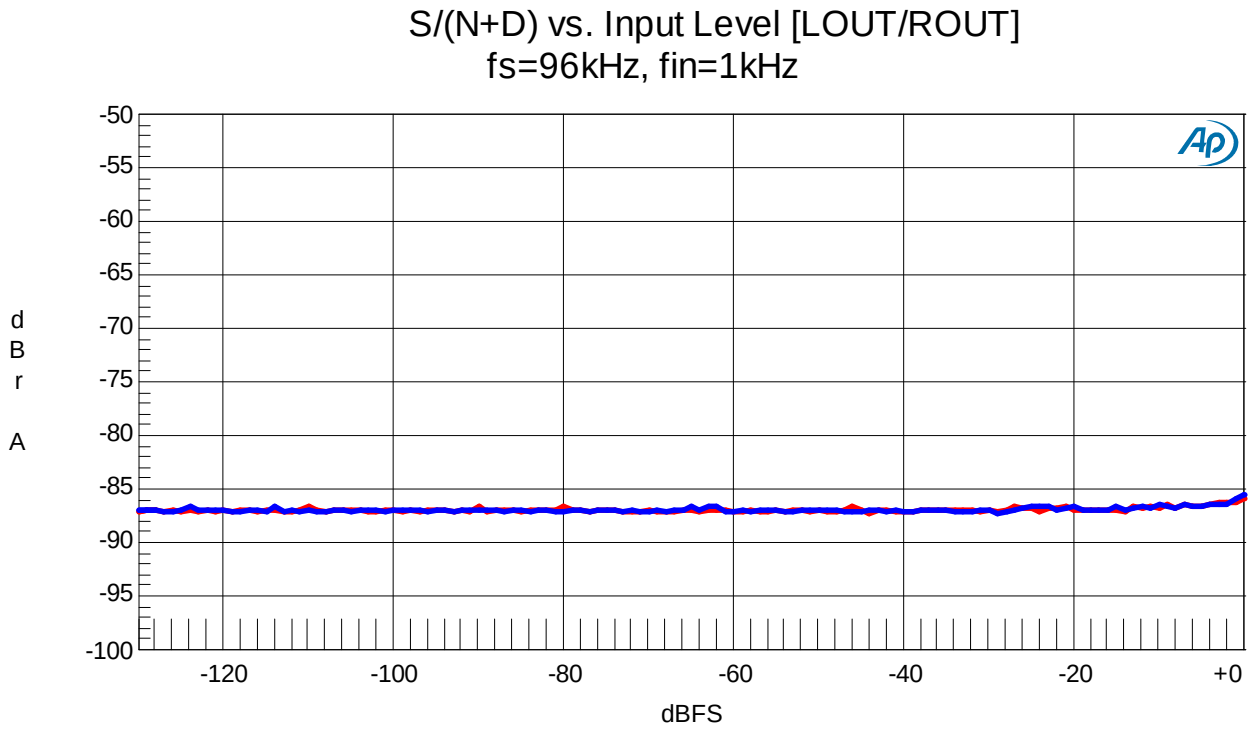



Figure 97. THD+N vs. Input Level

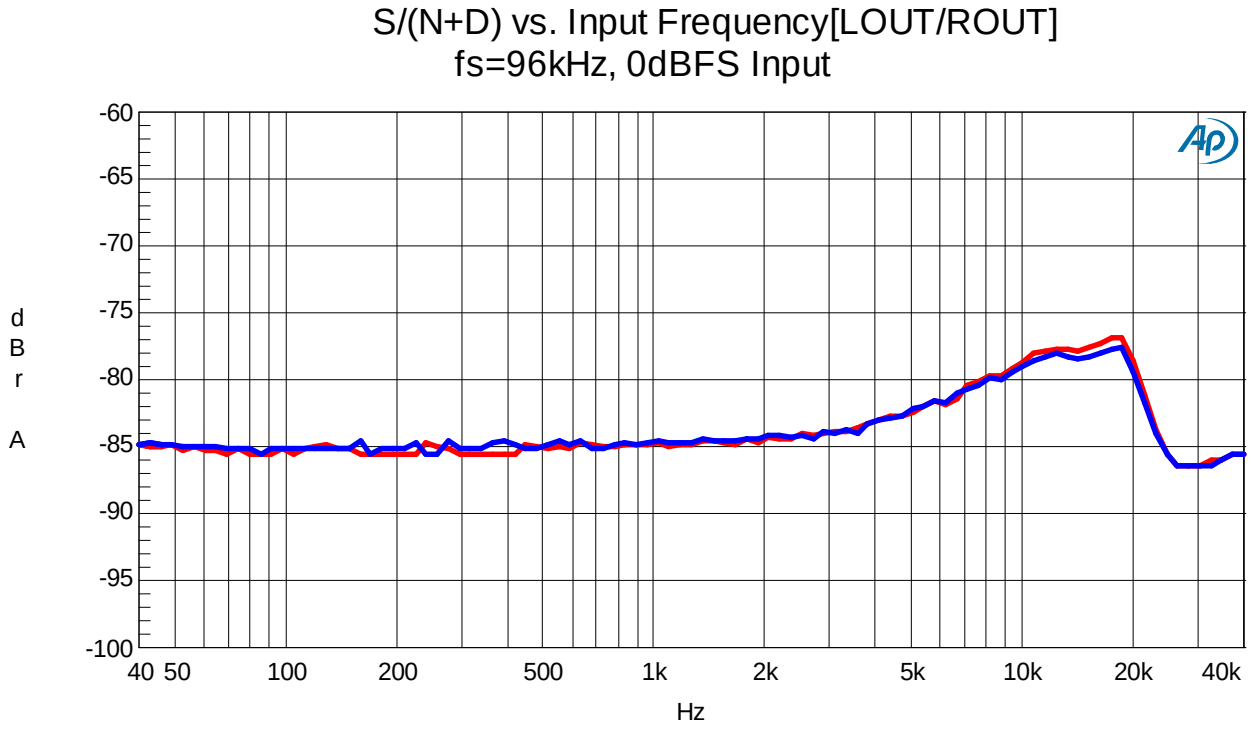



Figure 98. THD+N vs. Input Frequency

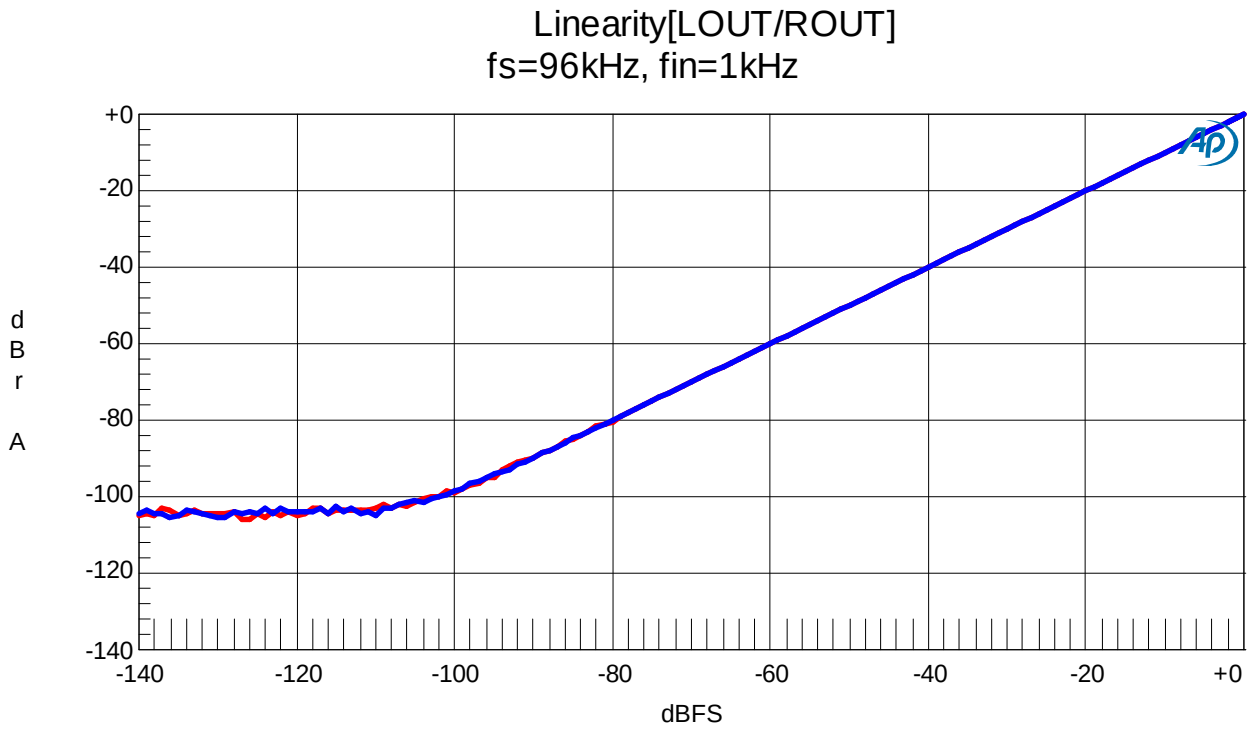



Figure 99. Linearity

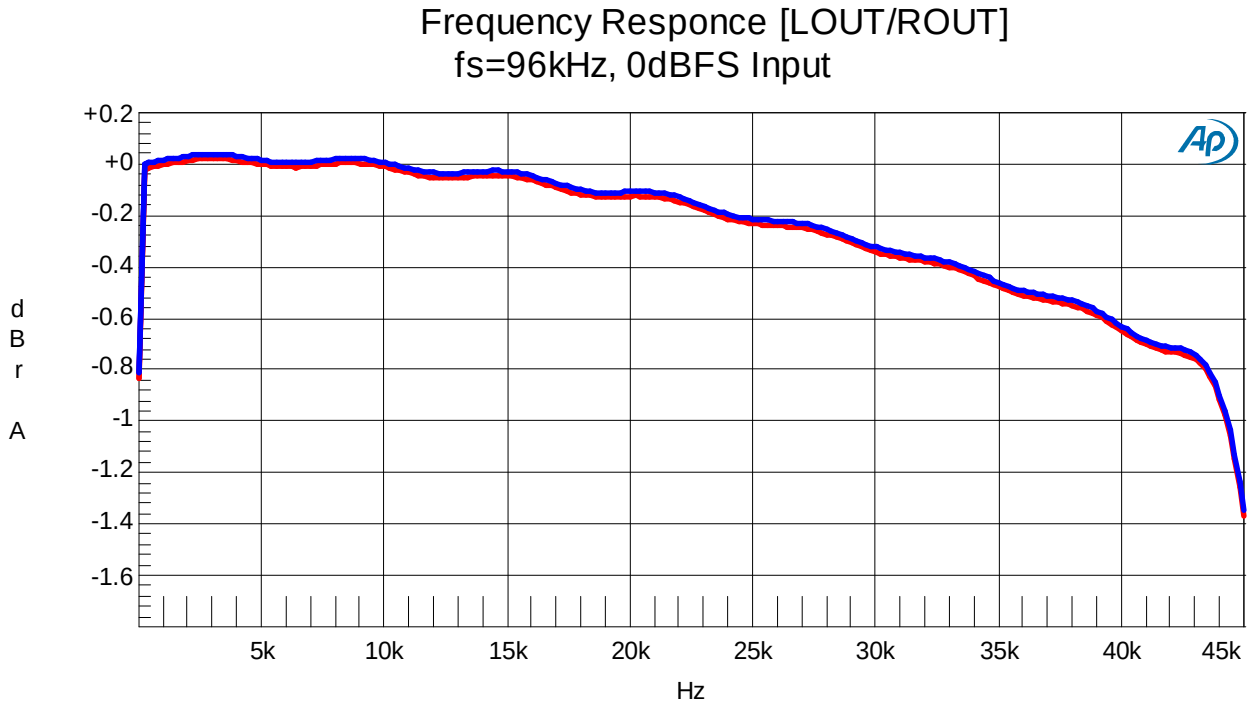



Figure 100. Frequency Response

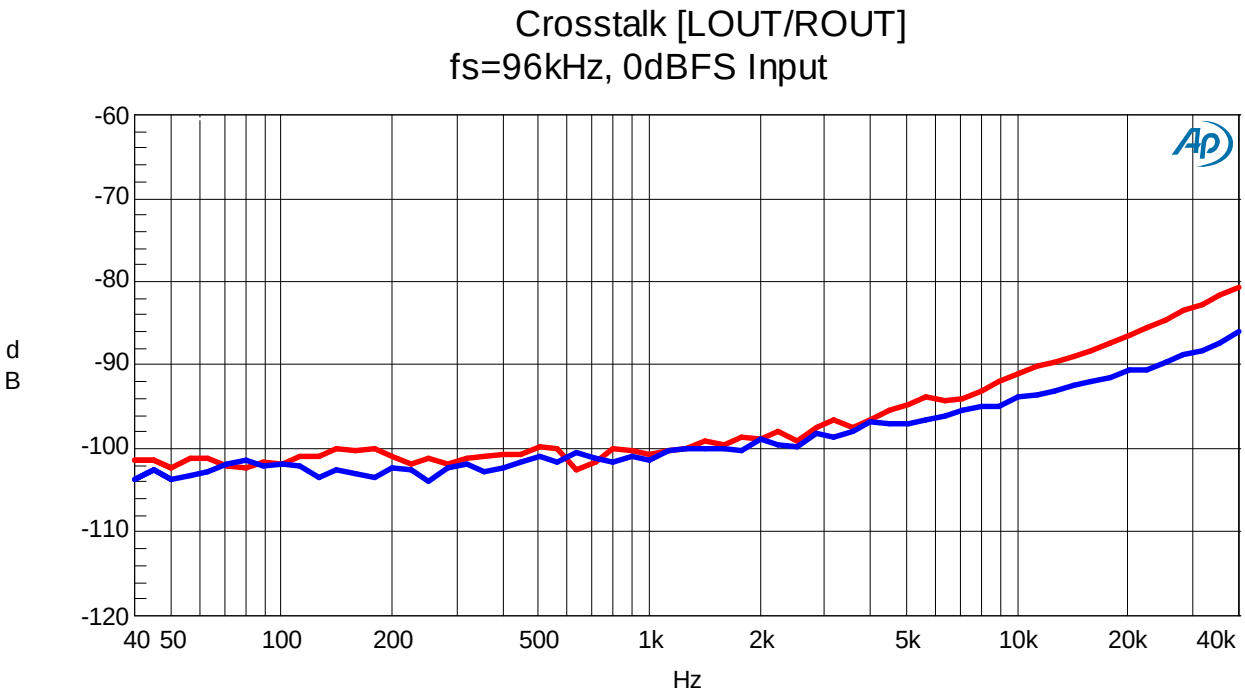



Figure 101. Crosstalk

## REVISION HISTORY

| Date (YY/MM/DD) | Manual Revision | Board Revision | Reason | Page | Contents |
|---|---|---|---|---|---|
| 12/06/14 | KM114100 | 0 | First edition | - | |

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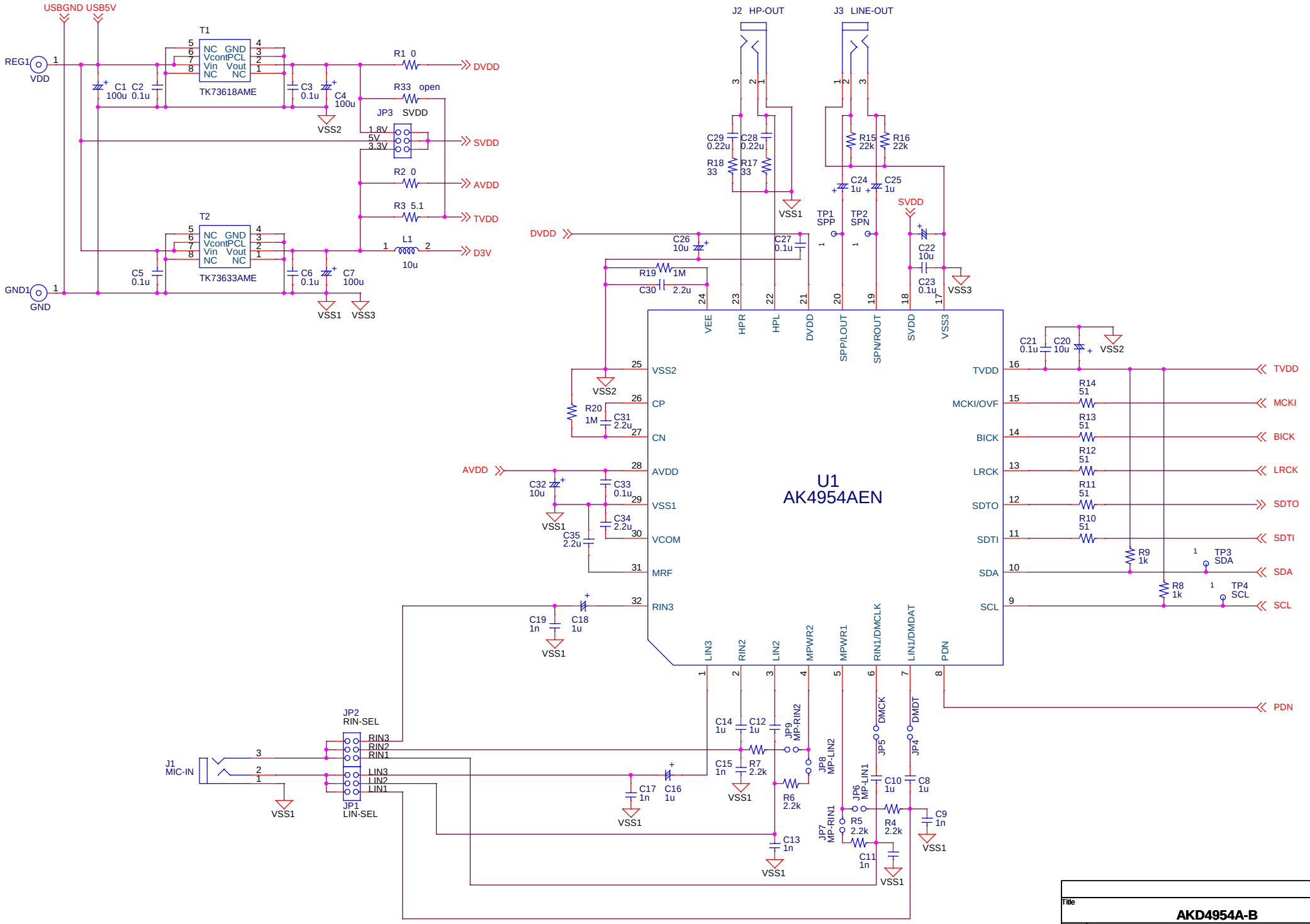




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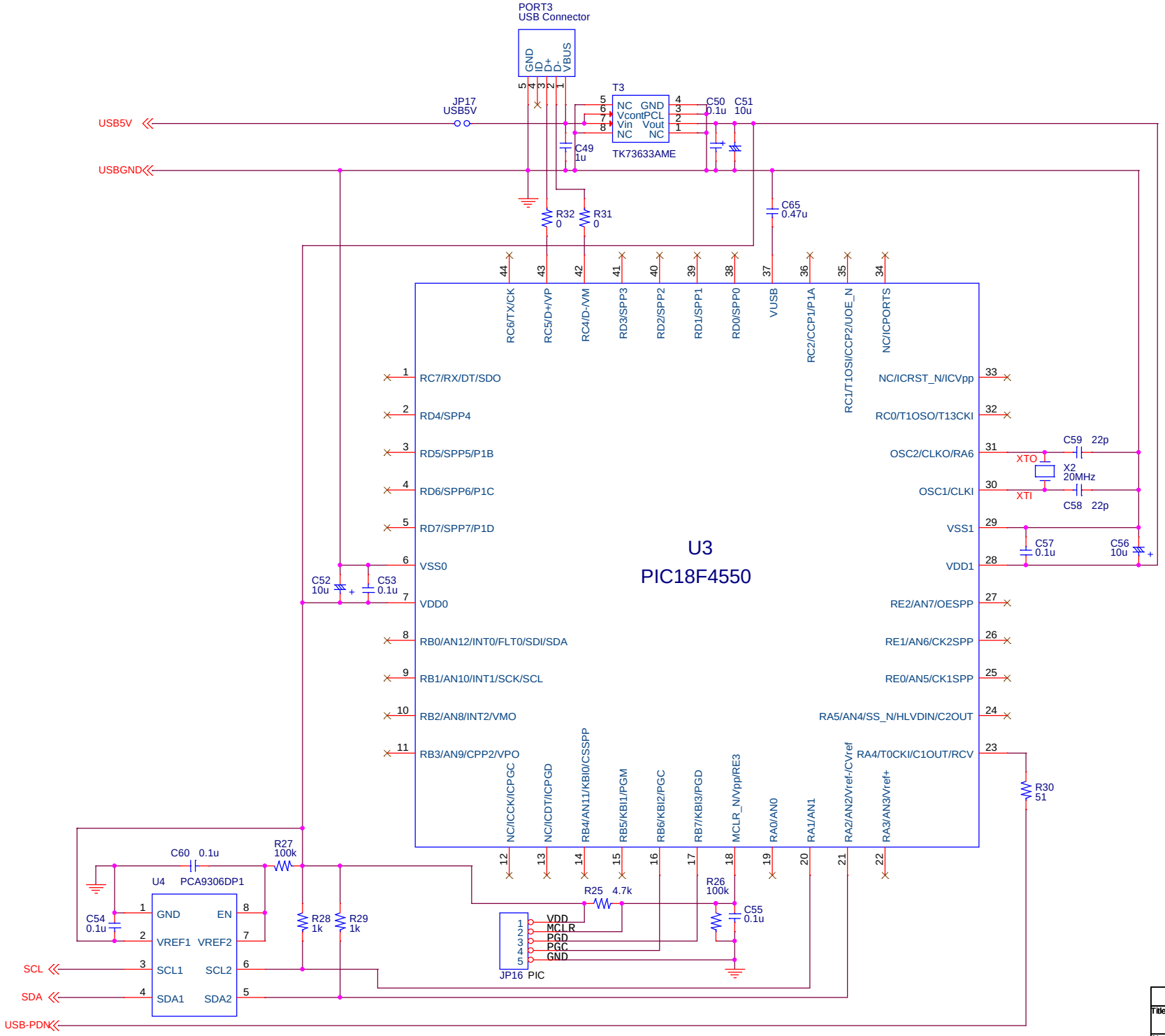


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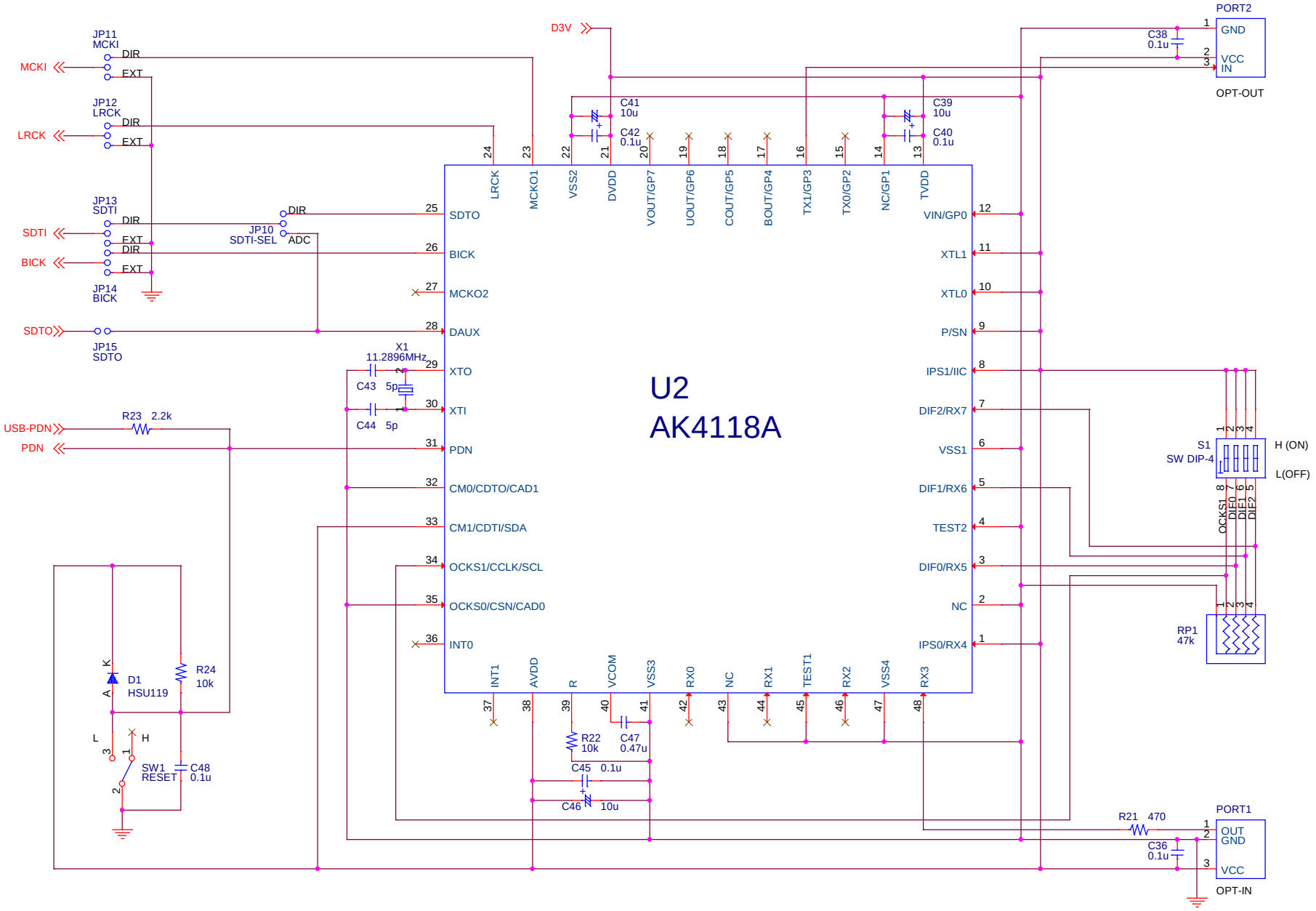




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