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Revisions & Change Log

Rev	Description	Date	Approved
A	Initial Release	09-04-15	
A1	Updated shunt location	01-16-15	

FRDM-KV10Z

OrCAD Capture 16.5

freescale semiconductor

Automotive, Industrial & Multi-Market Solutions Group

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ICAP Classification: FCP: FIUO: PUBI: -X-

Designer: AVID	Drawing Title: **FRDM-KV10Z**		
Drawn by: AVID	Page Title: **TITLE PAGE**		
Approved: P. Sustek	Size C	Document Number SCH-28718 | PDF: SPF-28718	Rev A1
	Date: Monday, January 18, 2016	Sheet 1 of 5	

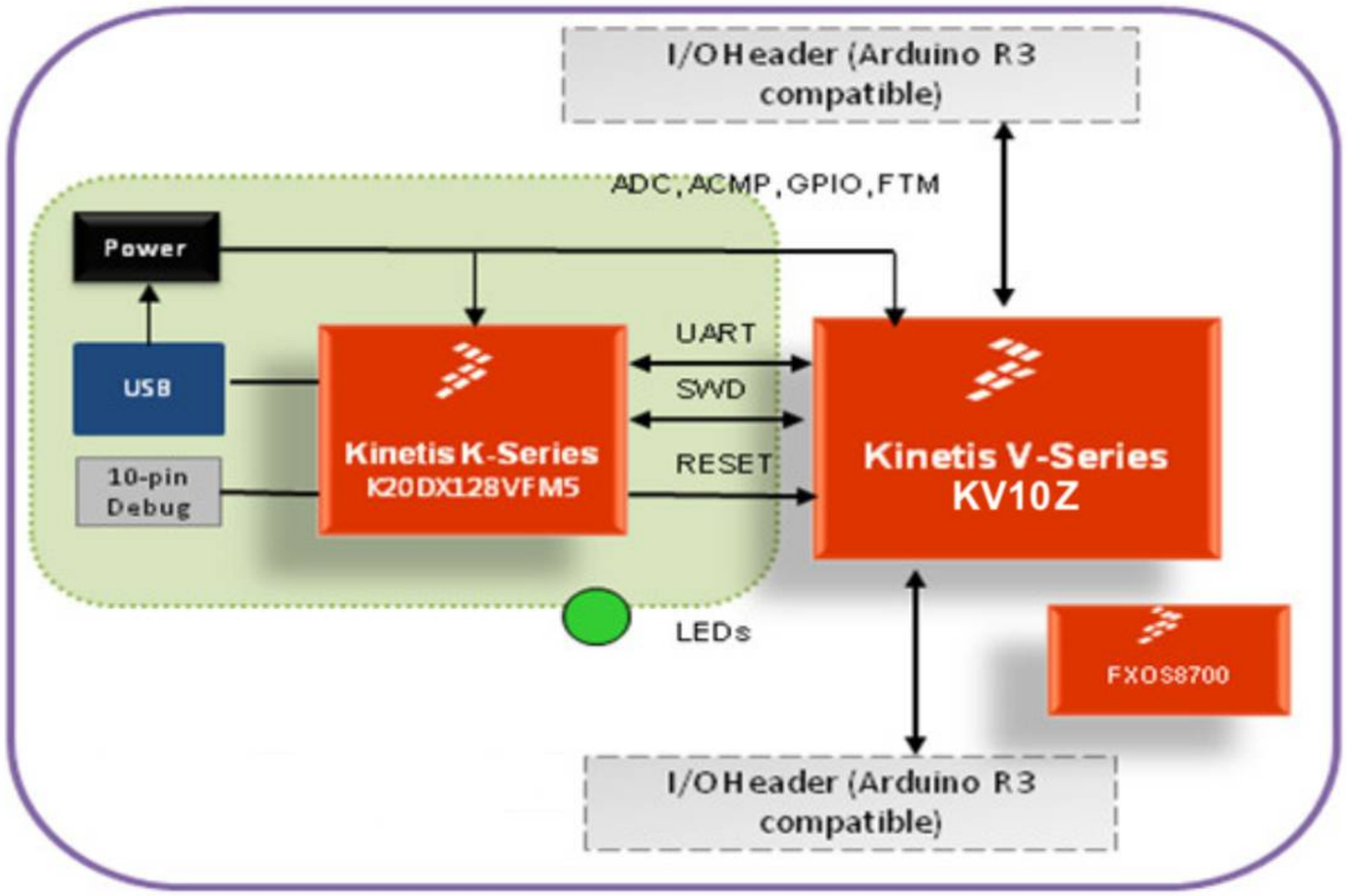
1. Unless Otherwise Specified:
   All resistors are in ohms, most are 1%, 1/10 Watt. Otherwise are 5%, 1/8 Watt.
   All capacitors are in uF, some are 10% or 20%
   All voltages are DC
   All polarized capacitors are tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title:
FRDM-KV10Z

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BLOCK DIAGRAM

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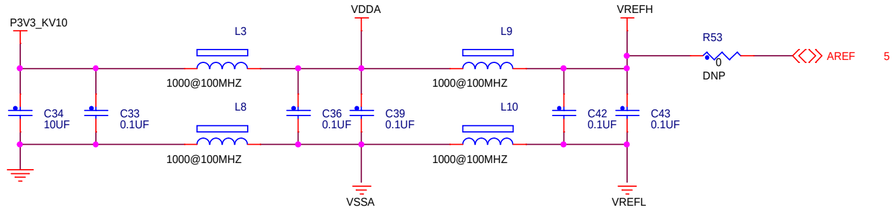
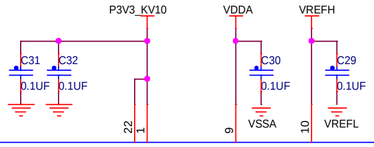
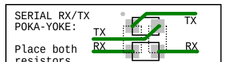
KV10 - 48LQFP





SERIAL RX/TX POKA-YOKE:

Place both resistors with the same orientation and provide same airgap between RX to TX resistors terminals in a square fashion.



U13

NET NAMES	PIN FUNCTIONS USED
SWD_CLK_KV10	17 PTA0/UART0_CTS_b/FTM0_CH5/SWD_CLK
5 PTA1/FTM2_CH0	18 PTA1/UART0_RX/FTM2_CH0/CMP0_OUT/FTM2_QD_PHA/FTM1_CH1
5 PTA2/FTM2_CH1	19 PTA2/UART0_TX/FTM2_CH1/CMP1_OUT/FTM2_QD_PHB/FTM1_CH0
3,4 SWD_DIO_TGTMCU	20 PTA3/UART0_RTS_b/FTM0_CH0/FTM2_FLT0/EWM_OUT_b/SWD_DIO
5 PTA4	21 PTA4/LLWU_P3/FTM0_CH1 PTA4/LLWU_P3/FTM0_CH1/FTM0_FLT3/NMI_b
3..5 RST_TGTMCU_B	26 PTA20/RESET_b
5 PTB0	27 PTB0/LLWU_P5
ADC0_SE9/PTB1	28 ADC0_SE8/ADC1_SE8/PTB0/LLWU_P5/I2C0_SCL/FTM1_CH0/FTM1_QD_PHA/UART0_RX
5 PTB2	29 PTB2/I2C0_SCL ADC0_SE9/ADC1_SE9/PTB1/EWM_IN/FTM0_FLT2/I2C0_SDA/FTM1_CH1/FTM1_QD_PHB/UART0_TX
5 PTB3	30 PTB3/I2C0_SDA ADC0_SE10/ADC1_SE10/ADC1_DM2/PTB2/I2C0_SCL/FTM0_FLT1/UART0_RTS_b/FTM0_FLT3
	31 PTB16/UART0_RX ADC1_SE2/ADC1_DP2/PTB3/UART0_CTS_b/I2C0_SDA/FTM0_FLT0
4,5 UART0_RX_TGTMCU	32 PTB17/UART0_TX PTB16/UART0_RX/FTM_CLKIN2/EWM_IN
4 UART0_TX_TGTMCU	PTB17/UART0_TX/FTM_CLKIN1/EWM_OUT_B
	ADC0_SE1/ADC0_DP1/ADC1_SE0/PTE16/SPI0_PCS0/SS_b/UART1_TX/FTM_CLKIN0/FTM0_FLT3
	ADC0_SE5/ADC1_SE5/ADC0_DM1/PTE17/SPI0_SCK/UART1_RX/FTM_CLKIN1/LPTMR0_ALT3
	ADC0_SE6/ADC1_SE1/ADC1_DP1/PTE18/SPI0_SOUT/UART1_CTS_b/I2C0_SDA/SPI0_SIN
	ADC0_SE7/ADC1_SE7/ADC1_DM1/PTE19/SPI0_SIN/UART1_RTS_b/I2C0_SCL/SPI0_SOUT
	ADC0_SE0/ADC0_DP0/PTE20/FTM1_CH0/UART0_TX
	ADC0_SE4/ADC0_DM0/PTE21/FTM1_CH1/UART0_RX
	PTE24/FTM0_CH0/I2C0_SCL/EWM_OUT_b
	PTE25/FTM0_CH1/I2C0_SDA/EWM_IN
	CMP1_IN5/CMP0_IN5/PTE29/FTM0_CH2/FTM_CLKIN0
24	EXTAL0/PTA18/FTM0_FLT2/FTM_CLKIN0 ADC1_SE4/CMP0_IN4/CMP1_IN4/DAC0_OUT/PTE30/FTM0_CH3/FTM_CLKIN1
25	XTAL0/PTA19/FTM0_FLT0/LPTMR0_ALT1/FTM1_FLT0/FTM_CLKIN1

VDD_22 VDD_1 VDDA VREFH VSS_2 VSS_23 VSSA VREFL

MKV10Z32VLF7

PIN FUNCTIONS USED	NET NAMES
33 PTC0/ADC1_SE11	PTC0 5
34 FTM0_CH0/PTC1	PTC1/FTM0_CH0 5
35 FTM0_CH1/PTC2	PTC2/FTM0_CH1 5
36 FTM0_CH2/PTC3	PTC3/FTM0_CH2 5
37 FTM0_CH3/PTC4	PTC4/FTM0_CH3 5
38 PTC5/LLWU_P9/SPI0_SCK	PTC5 5
39 CMP0_IN0/PTC6/LLWU_P10/SPI0_SOUT/I2C_SCL	PTC6 5
40 CMP0_IN1/PTC7/SPI0_SOUT/I2C_SDA	PTC7 5
41 PTD0/UART1_RX//LLWU_P12	
42 PTD1/UART1_TX	
43 PTD2/LLWU_P13/FTM0_CH2	PTD2 5
44 PTD3/SPI0_SIN	PTD3 5
45 FTM0_CH4	PTD4/FTM0_CH4 5
46 FTM0_CH5	PTD5/FTM0_CH5 5
47 PTD6/LLWU_P15/SPI0_PCS3	PTD6 3,5
48 FTM1_CH1	PTD7 5
3 PTE16/ADC0_SE1	PTE16 5
4 ADC0_SE5/PTE17	
5 ADC0_SE6/PTE18	
6 ADC0_SE7/PTE19	
7 ADC0_DP0	ADC0_DP0 3,5
8 ADC0_DM1	ADC0_DM0 3,5
15 PTE24/FTM0_CH0	PTE24 5
16 PTE25/FTM0_CH1	PTE25 3,5
13 CMP1_IN5/CMP0_IN5/PTE29/FTM0_CH2	PTE29 3,5
14 ADC1_SE4/PTE30	ADC1_SE4/PTE30 3,5

R60 0 PTC6/I2C0_SCL 5
R62 0 PTC7/I2C0_SDA 5
R67 0 PTC6/SPI0_SOUT 5
R68 0 PTD3/SPI0_SIN 5
R58 0 PTD0 5
R59 0 PTD1 5

R65 0
R66 0
R54 0
R55 0

R52 1.0M DNP

QZ1 2 1 10MHZ

C24 18PF
C20 18PF

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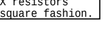
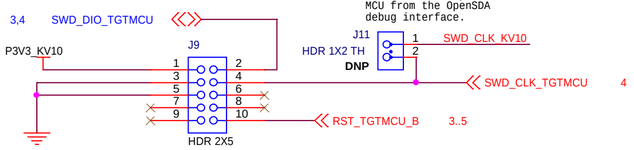
Place both resistors with the same orientation and provide same airgap between RX to TX resistors terminals in a square fashion.



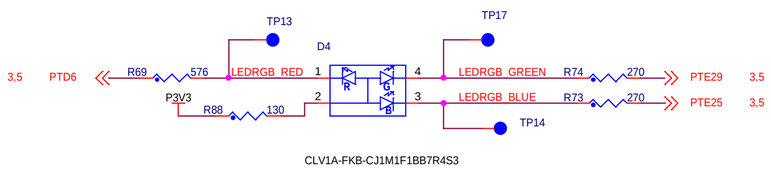
SWD CONNECTOR

SHORTING HEADER ON BOTTOM LAYER

Jumper is shorted by a cut-trace on bottom layer. Cutting the trace will effectively isolate the on-board MCU from the OpenSDA debug interface.

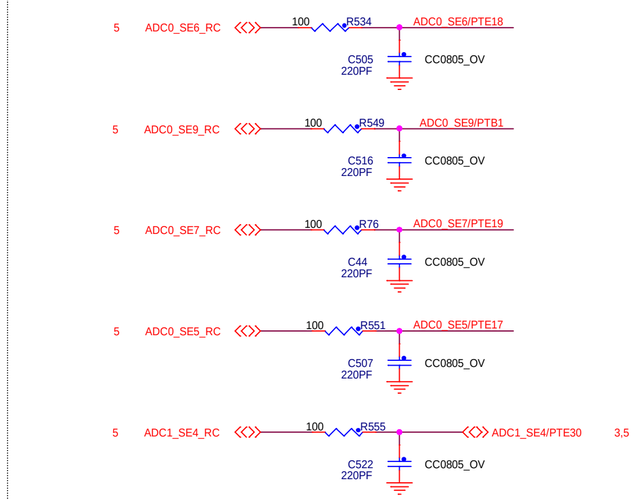


RGB LED FEATURE

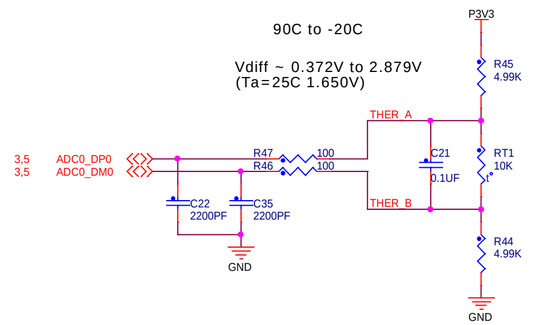


CLV1A-FKB-CJ1M1F1BB7R4S3

RC Filter



THERMISTOR



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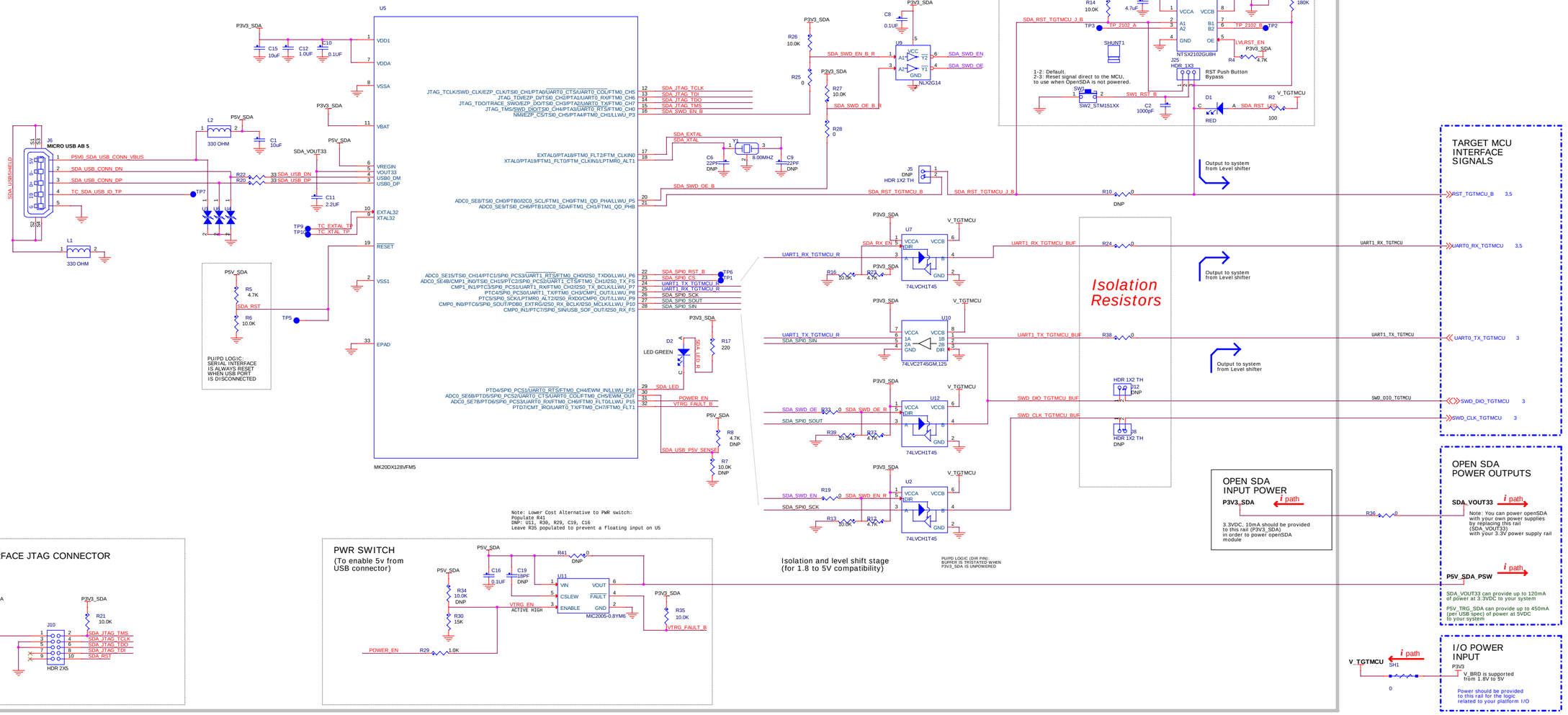
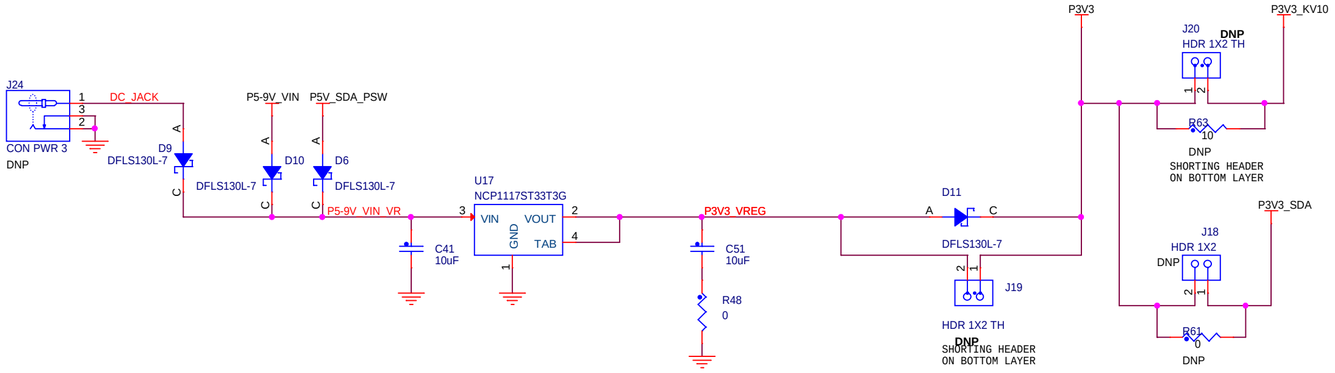
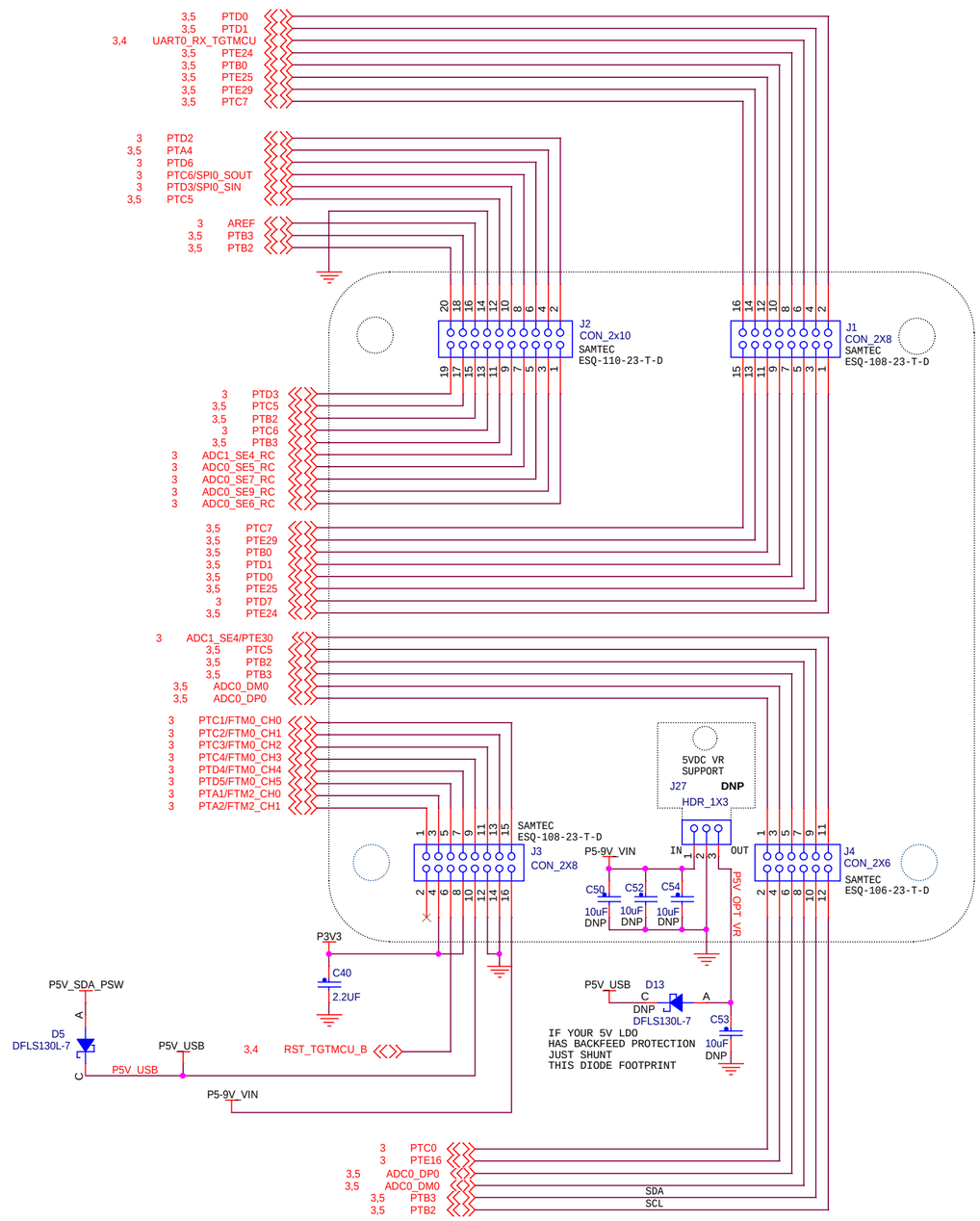
OpenSDA Interface



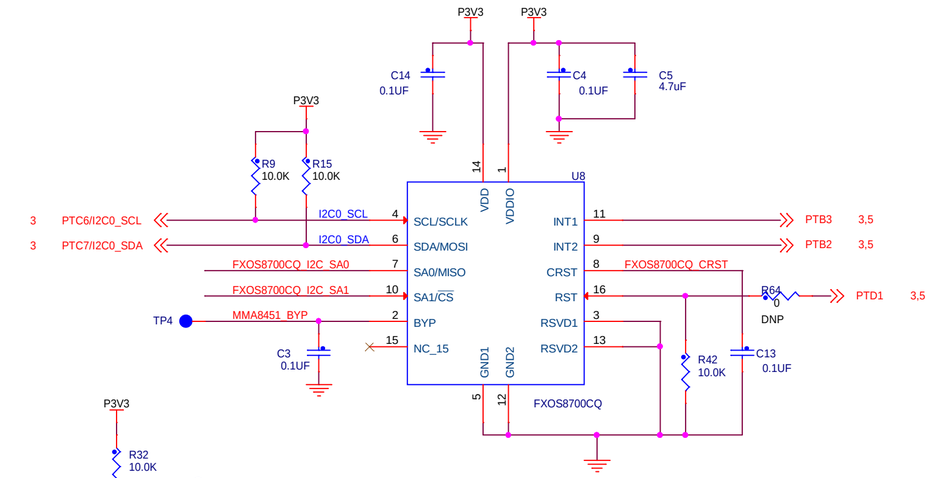


ARDUINO COMPATIBLE HEADERS

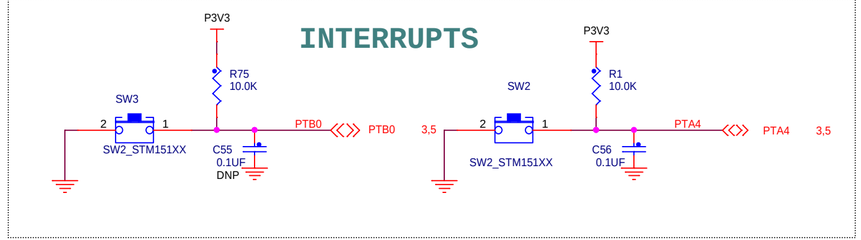


I2C INERTIAL SENSOR

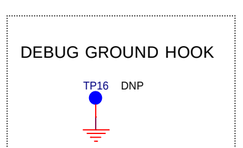
(ACCELEROMETER AND MAGNETOMETER)

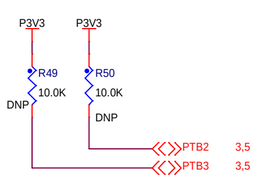


INTERRUPTS



DEBUG GROUND HOOK





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ARDUINO SHIELDS & COMBO SENSOR

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