

6

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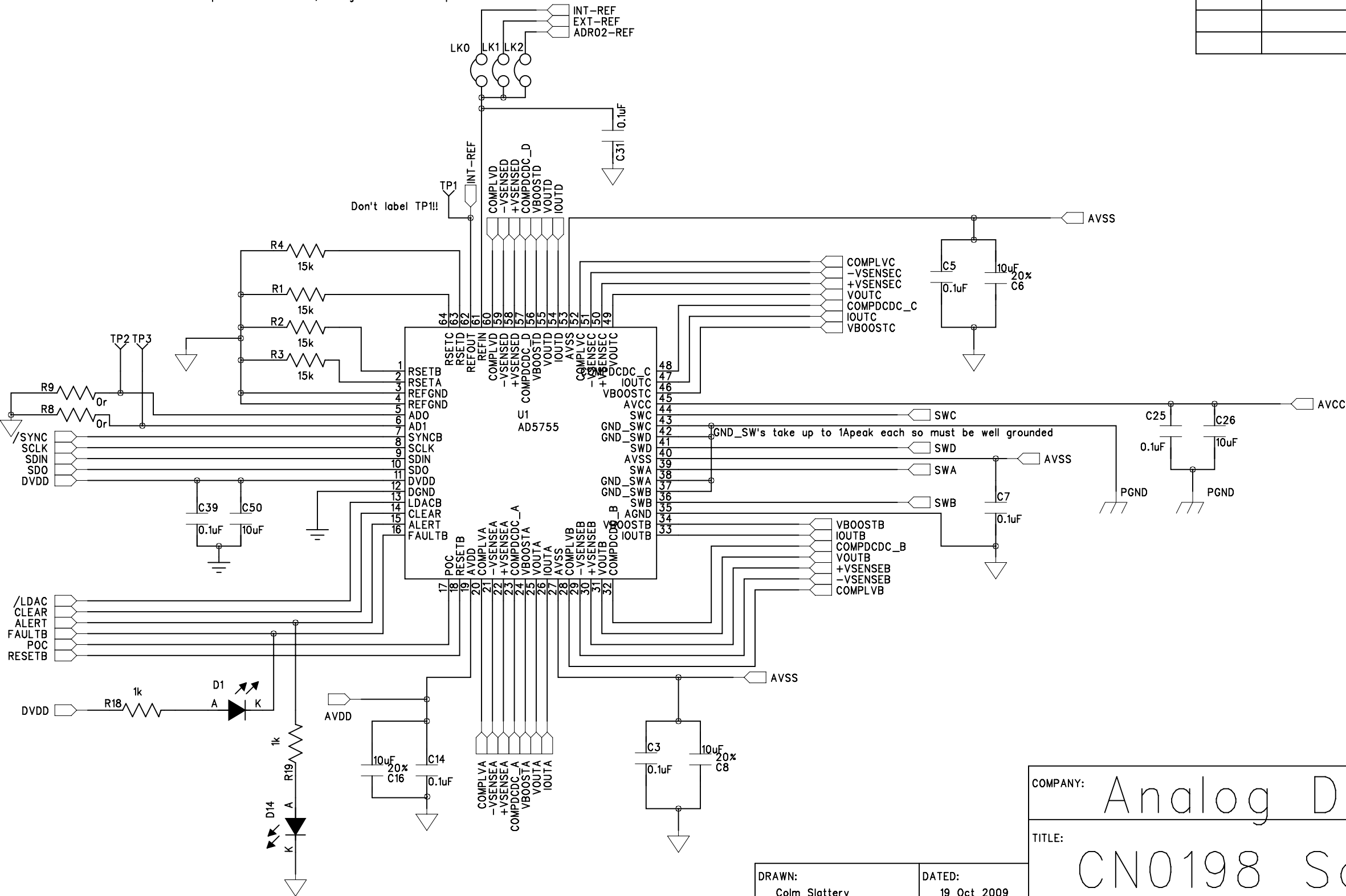
1

REVISION RECORD

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DC-DC ("BOOST INDUCTOR") Layout is important for minimizing ground bounce  
Looking to have some patchwork near the output

Ver B to Ver C - added compensation resistors, changed inductor footprint



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D

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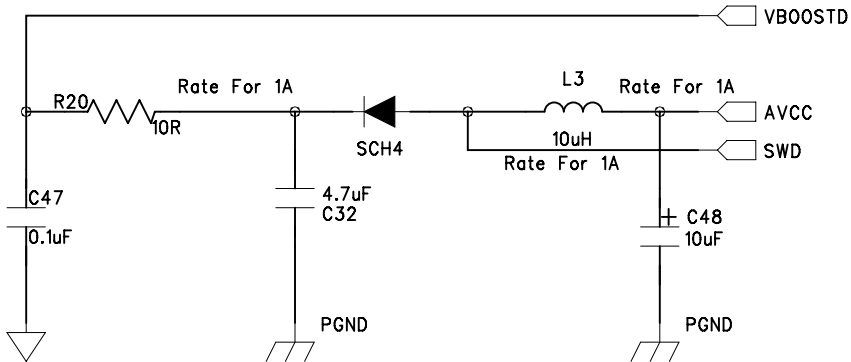
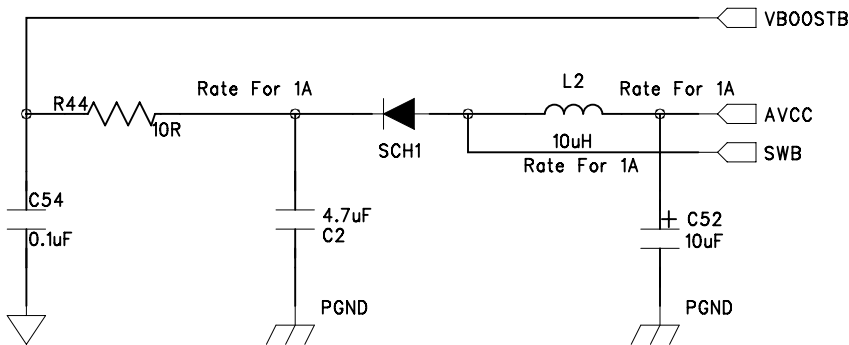
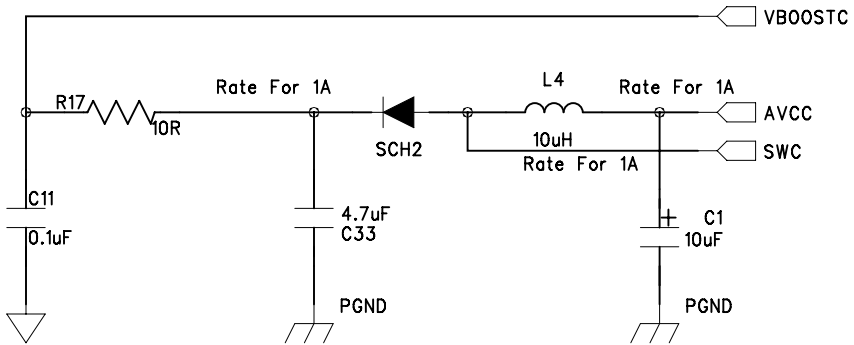
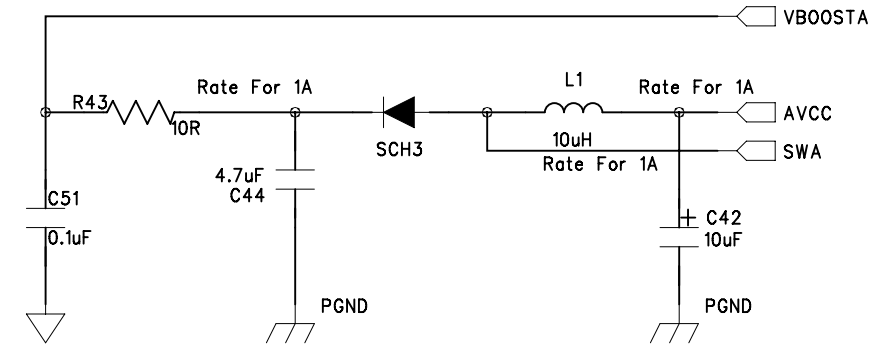
D

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY:			
TITLE:			
CODE:	SIZE:	DRAWING NO:	REV:
SCALE:		SHEET: OF	

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

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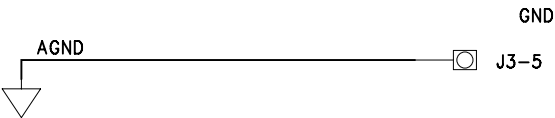
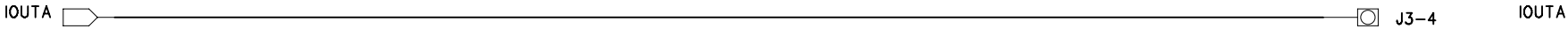
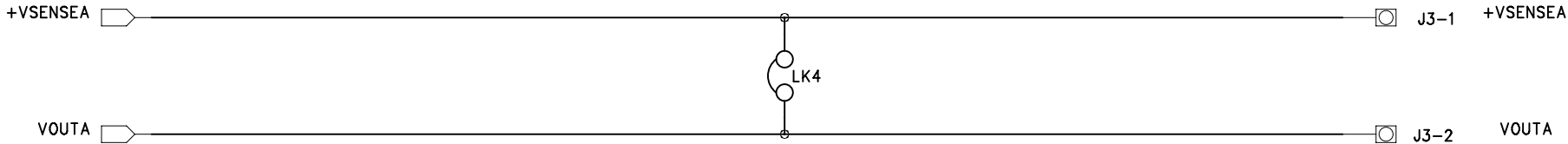
D

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY:			
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RELEASED:	DATED:

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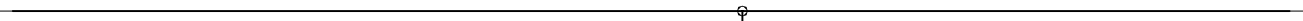
C

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REVISION RECORD			
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+VSENSEB



J2-1

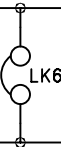
+VSENSEB

VOUTB



J2-2

VOUTB



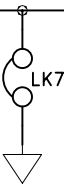
LK6

-VSENSEB



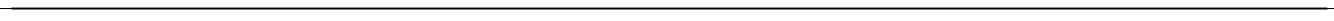
J2-3

-VSENSEB  
or CHARTB



LK7

IOUTB



J2-4

IOUTB



AGND



J2-5

GND

COMPANY:

TITLE:

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

CODE:	SIZE:	DRAWING NO:	REV:
SCALE:			SHEET: OF

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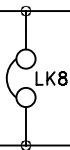
1

REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

D

+VSENSEC



J1-1 +VSENSEC

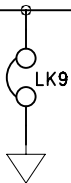
VOUTC



J1-2 VOUTC

C

-VSENSEC



J1-3 -VSENSEC  
or CHARTC

IOUTC



J1-4 IOUTC

B

GND

AGND



J1-5



A

COMPANY:

TITLE:

DRAWN:

DATED:

CHECKED:

DATED:

QUALITY CONTROL:

DATED:

RELEASED:

DATED:

CODE:

SIZE:

DRAWING NO:

REV:

SCALE:

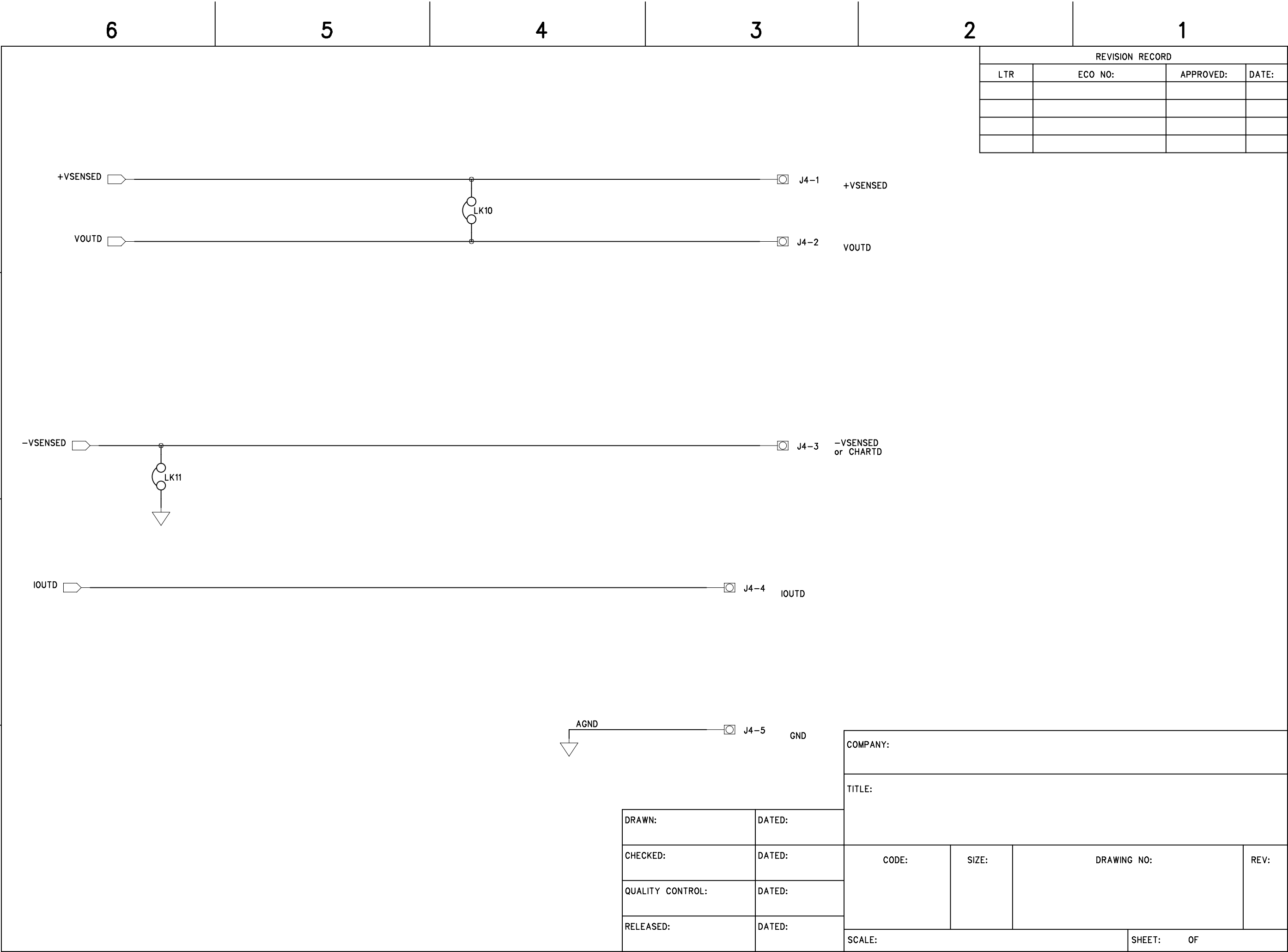
SHEET: OF

D

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A

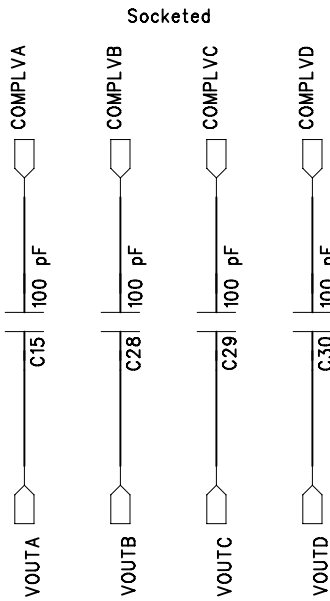
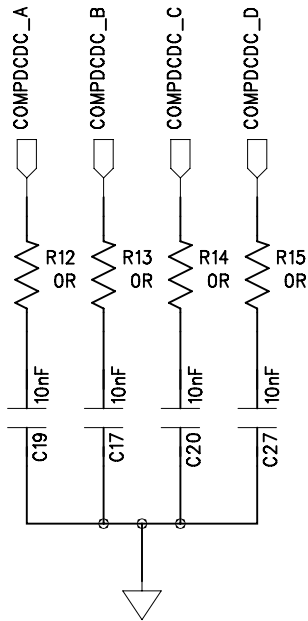
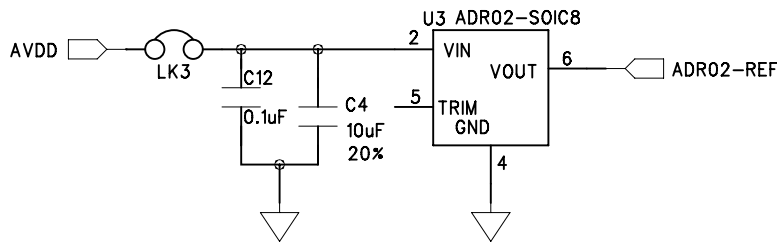
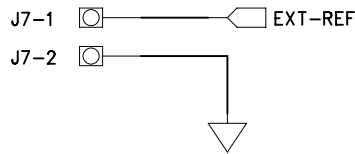


D

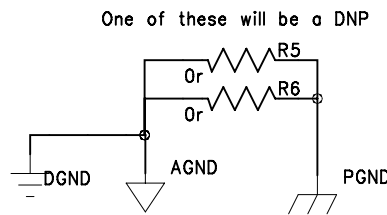
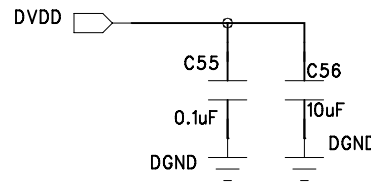
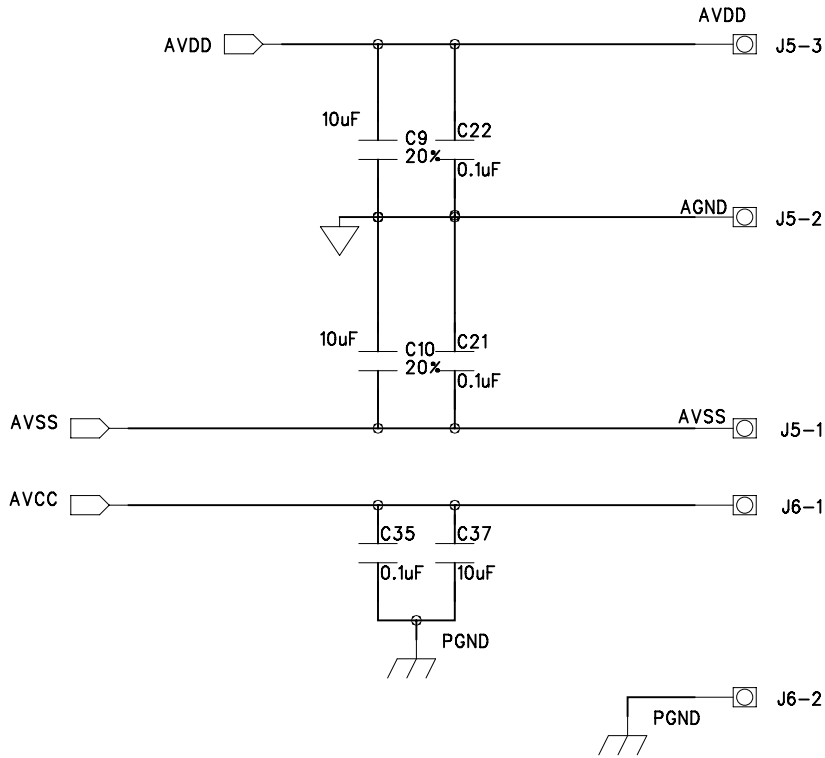
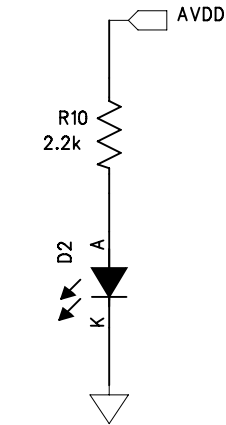
C

B

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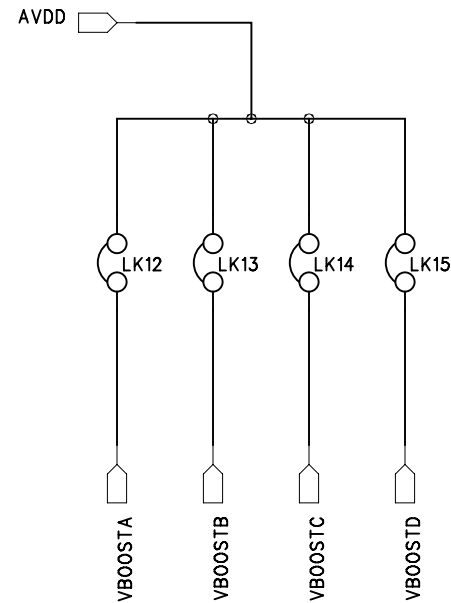
Paddle Connected to AVSS



2

1

REVISION RECORD			
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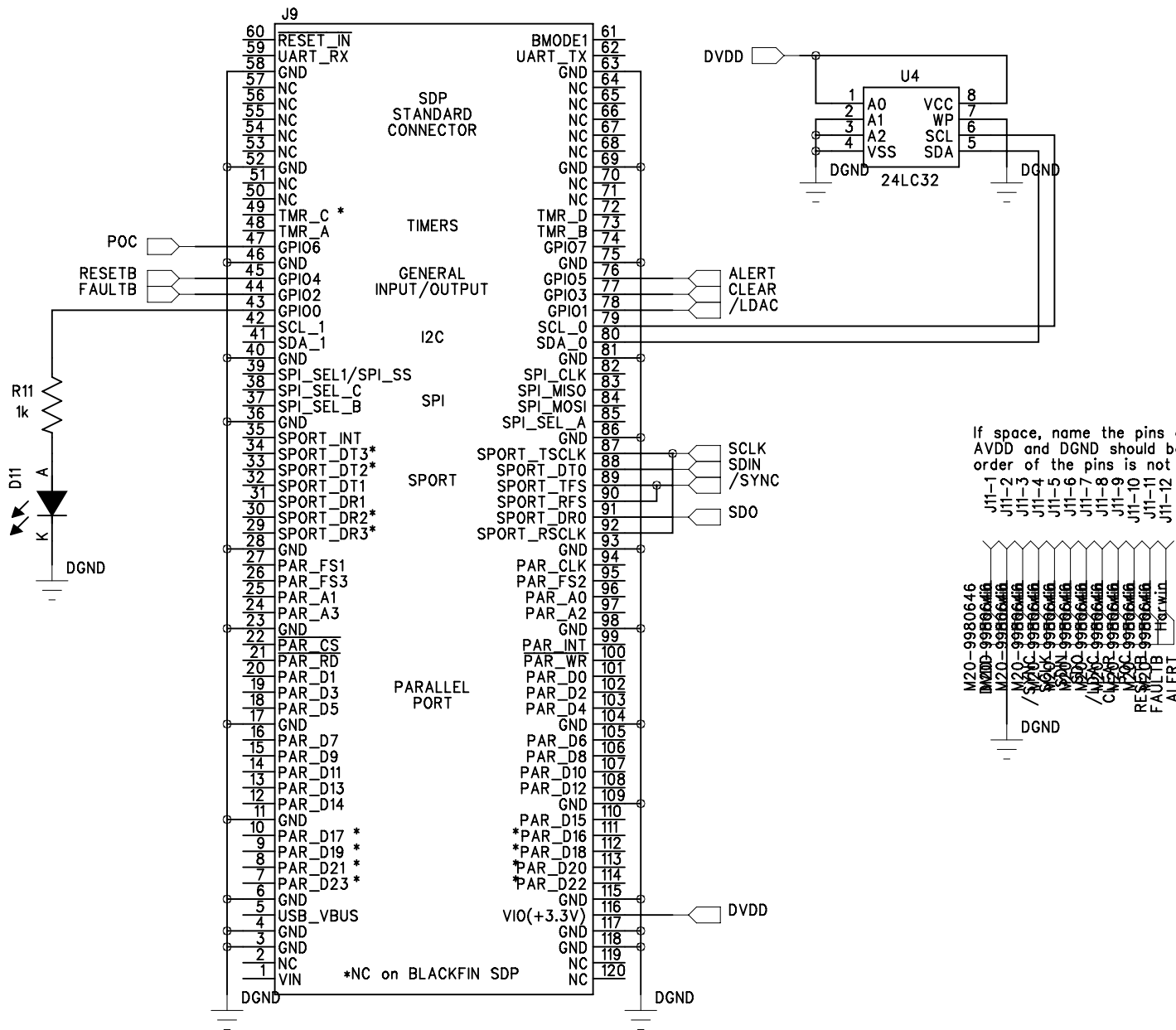
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If space, name the pins on this connector  
AVDD and DGND should both be on one end of the connector, otherwise the  
order of the pins is not important

COMPANY:			
TITLE:			
CODE:		SIZE:	DRAWING NO:
REV:		REV:	
SCALE:		SHEET: OF	

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED: