AN2647
Application note

Using the STR91xFA external memory interface (EMI)

Introduction

The STR91xFA EMI bus is a very flexible bus and is user programmable. The bus can be configured to interface to different types of memory devices, including SRAM, Flash memory, ROM or PSRAM. Some of the programmable features of the EMI bus are:

- Multiplexed or non-multiplexed bus
- Bus width: 8 or 16 bit
- Address lines select: A0-15 or A0-A23
- Read and Write signal timing and wait state insertion
- Asynchronous or synchronous bus access
- Page or burst mode access
- Chip select signals (CS0-3)
- ALE polarity and pulse width
- Bus clock (BCLK) frequency

This application note covers the EMI asynchronous mode configuration for interfacing to standard memory devices in *Section 1: Interfacing with asynchronous memory*.

It covers also EMI Synchronous mode which has a different bus timing and configuration in *Section 2: Interfacing with synchronous memory*.

Software is available with this application note and can be downloaded separately online from www.st.com.

Contents

1 Interfacing with asynchronous memory

1.1 Multiplexed or non-multiplexed EMI bus selection

The multiplexed EMI bus is selected if you have a 16-bit system bus or using 16-bit memory device. The multiplexed bus requires a 16-bit address latch, as most memory devices do not accept multiplexed address/data input.

The 8-bit non-multiplexed bus is suitable for 8-bit memory or I/O devices. In this configuration, the EMI memory banks are limited to 64 KB each, as there are only 16 address lines available.

In general the non-multiplexed bus has a shorter bus cycle that can be completed in one bus clock period (t_{BCLK}) while the multiplexed bus takes minimum of 3 BCLK clocks. The multiplexed bus has a 16 bit data bus, and can provide high data transfer rate for memory device like PSRAM that supports burst mode. The DMA Controller can be programmed to perform burst data transfer between the internal SRAM and the EMI bus.

1.1.1 Multiplexed EMI bus configuration

The multiplexed bus has different bus signals and port assignments than the non-multiplexed bus. As shown in Table 1, Ports 8 and 9 provide the multiplexed 16 bit address and data bus (AD0-AD15), the optional higher address A16-A23 are assigned to Port 7. *Figure 1.* & *Figure 2.* show a typical EMI multiplexed bus connecting to two 16-bit memory devices: a 4 MB ISSI SRAM and a 4 MB SPANSION Flash memory. The SN74LVC16373A is a high speed 16-bit address latch with maximum t_{PD} delay of 4.2 ns. Note only four pins on Port 7 are address lines, the remaining four pins are for other I/O functions.

Table 1. Multiplexed bus signals

Signal name	Pin / Port assignment	Signal description
AD0-AD7	Port 8	Multiplexed address/data bus AD0-AD7
AD8-AD15	Port 9	Multiplexed address/data bus AD8-AD15
A16-A23	Port 7	Address A16-A23, pin configurable
ALE	EMI_ALE	Address Latch signal. Polarity and width is programmable
Read	EMI_RDn	Read signal
Write Low (Low Byte Select)	EMI_BWRn (EMI_WRLn or EMI_LBn)	Low Byte (D0-D7) Write signal or Low Byte Select signal.
Write High (High Byte Select)	EMI_WRHn (EMI_UBn)	High Byte (D8-D15) Write signal or High Byte Select signal
Write Enable	EMI_WEn	Write Enable signal, use together with the UB/LB byte select signals in synchronous mode.
CS0-CS3	Port 0(P0.4-P0.7) or Port 5 (P5.4-P5.7) or Port 7 (P7.4-P7.7)	One chip select for each of the 4 Memory Banks.Can be assigned to any of the 3 port.

Figure 1. 16-bit Flash multiplexed bus connection

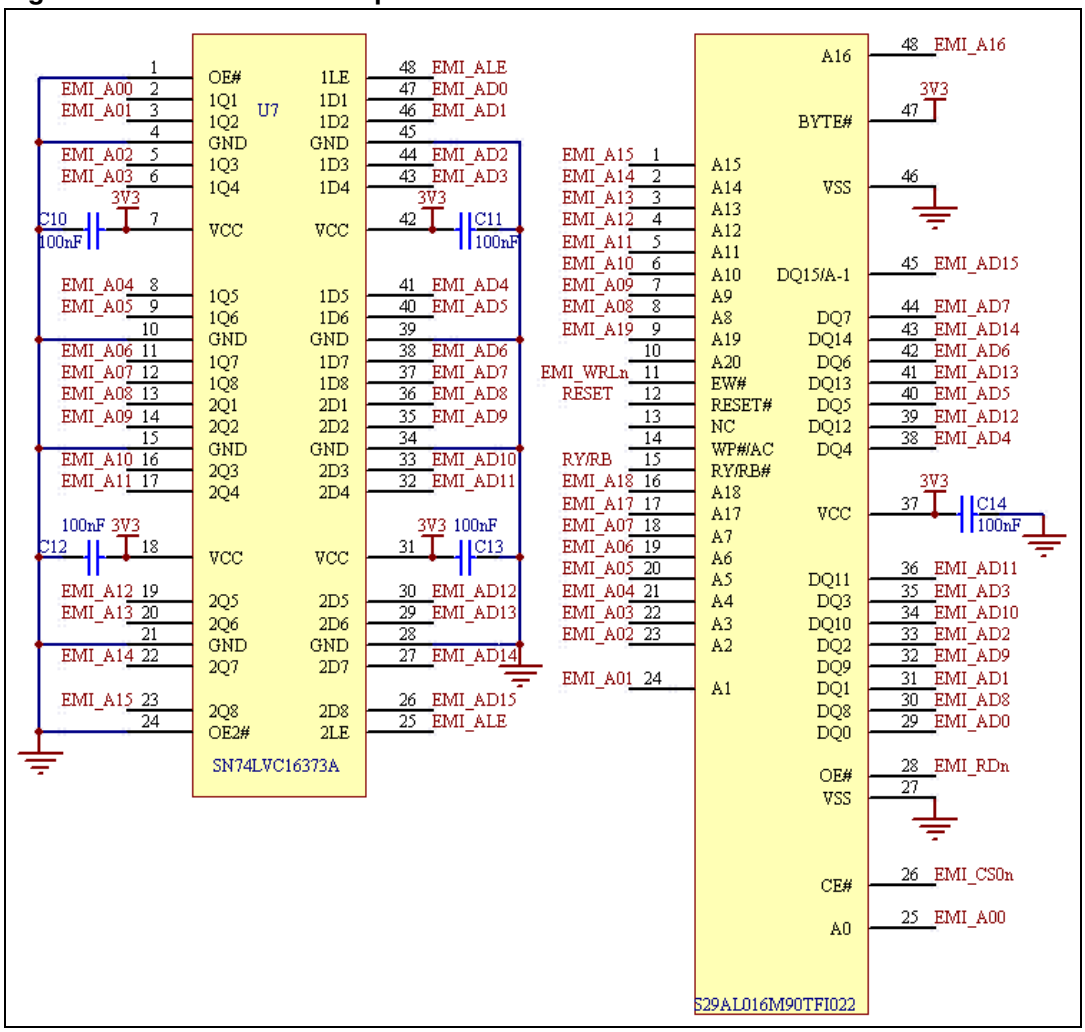
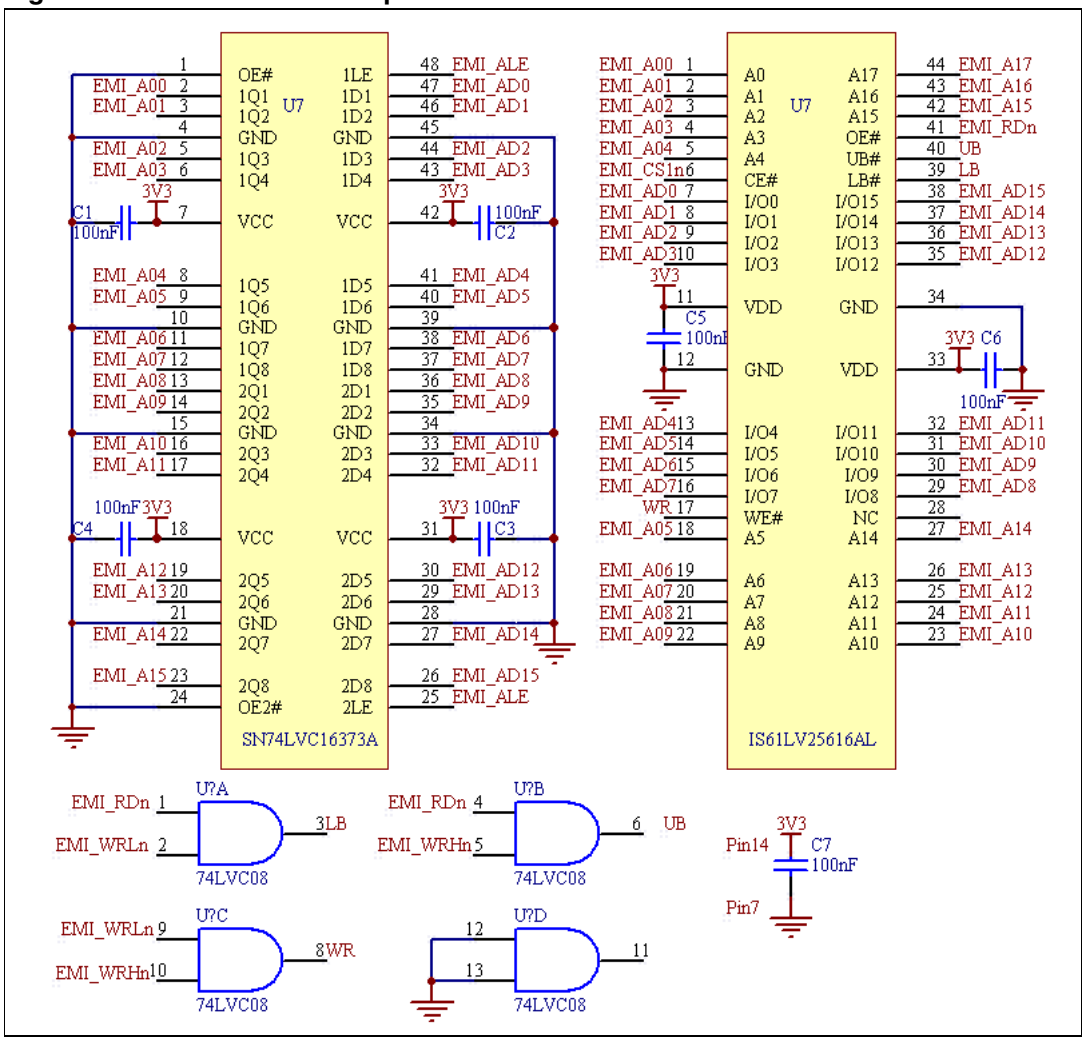


Figure 2. 16-bit SRAM multiplexed bus connection



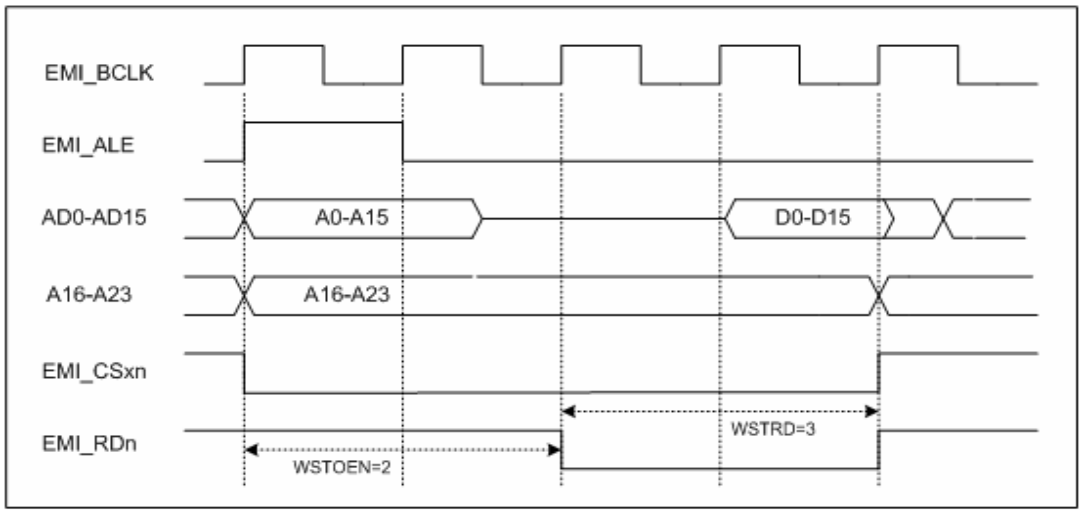
Note: Please note the logic gates used are needed to tolerate the 8-bit data operations.

After power up or system reset, the EMI bus is default to a very slow, asynchronous, multiplexed bus. User need to configure the GPIO ports. The read and write timings listed below to set up a memory bus that meets your system's requirement for optimal performance.

Read bus cycle timing configuration

Figure 3. shows a typical Read Bus Cycle. All bus timings are referenced to the internal BCLK clock signal. BCLK clock is only available on an external pin for various usage on the 144 pin BGA package.

Figure 3. Read bus cycle, 16-bit multiplexed bus



EMI_ALE signal configuration

The EMI_ALE signal is used to latch the address A0-15 by the external address latch, or as a direct input to memory device that have an ALE pin. The EMI_ALE by default is one BCLK period in length with active high polarity. It can be programmed to be 2 BCLK period in asynchronous mode and the polarity can be active low. The ALE length and polarity are defined in the SCU_SCR0 register.

Address A0-A15 are valid at the leading edge of EMI_ALE and are driven for another half BCLK period after the trailing edge. The AD bus is tri-stated after the address phase is over. A16-23 are not multiplexed and remain stable until the end of the bus cycle.

EMI_RD signal configuration

The EMI_RDn timing is controlled by the WSTRD value in the EMI_RCRx register (Read Wait State Control) and the WSTOEN value in the EMI_OECRx register (Output Enable Control).

- **WSTOEN:** Output Enable. WSTOEN specifies the delay between the assertion of the chip select and the time EMI_RDn signal goes low. The delay is defined in terms of t_{BCLK}.
  The minimum WSTOEN value is 2 in a multiplexed bus (for ALE with one BCLK period width). EMI_RDn becomes active after 2 t_{BCLK} so as not to overlap the address phase of the bus cycle.
- **WSTRD:** Read wait state. WSTRD specifies the pulse width, or the rising edge of EMI_RDn. The pulse width is defined in terms of number of t_{BLCK} and is = (WSTRD-WSTOEN+1).

The choice of the WSTRD value depends on the access time of the memory device, slow memory requires more wait states. Typically, the memory access time must meet the following condition:

$$\text{Memory Read access time} < (t_{RAS} + t_{RP} - t_{RDS})$$

Where t_{RAS} is the EMI read address setup time, t_{RP} is the EMI_RDn pulse width and t_{RDS} is the data setup time.

The EMI Bus stops driving address A16-A23 and the CSx signal at the rising edge of EMI_RDn.

The read bus cycle in *Figure 3.* has the following configuration:

ALE Length = 1

WSTOEN = 2

WSTRD = 3

The above read signal configuration can read a memory device with access time of less than $(4*t_{BCLK} - t_{RDS})$ns, where t_{RDS} is the data setup time as specified in the STR91xFA data sheet.

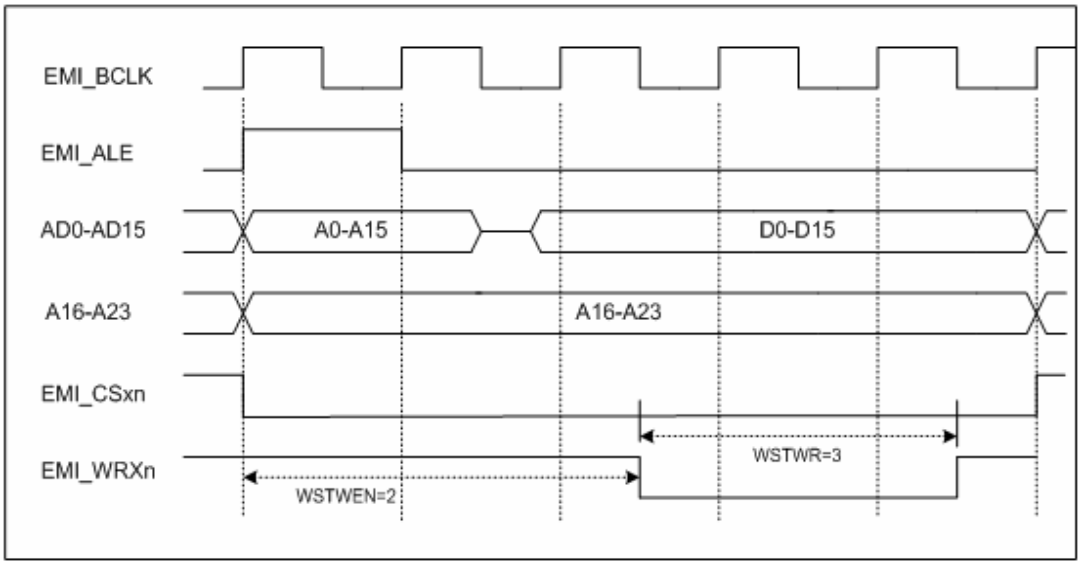
Write bus cycle timing configuration

In asynchronous bus configuration, the default write signals are EMI_WRLn and EMI_WRHn. The other set of write signal selection, EMI_WEN, EMI_LBn and EMI_UBn, are available in BGA package in synchronous mode only. *Figure 4.* shows a typical Write Bus Cycle. The write bus cycle timing differs from the read bus cycle in two ways:

– The write signals EMI_WRLn and EMI_WRHn (EMI_WRXn) align with the falling edge of the BCLK

– The write signals are terminated half BCLK period before the CSx signal.

Figure 4. Write bus cycle, 16-bit multiplexed bus



EMI_WR signal configuration

The EMI_WRxn timings are controlled by the WSTWR value in the EMI_WCRxn register (Write Wait State Control) and the WSTWEN value in the EMI_WECRx (Write Enable Control) register.

- **WSTWEN**: Write Enable. WSTWEN specifies the delay period between the assertion of the CSx chip select and the falling edge of EMI_WRxn. The delay is defined in terms of BCLK clock periods which is (WSTWEN + 1/2) for asynchronous write cycles. The minimum WSTWEN value is 1 in a multiplexed bus (for ALE with one BCLK period width).With WSTWEN=1, EMI_WRxn becomes active only after the address phase is over.
- **WSTWR**: Write wait state. WSTWR specifies the pulse width of EMI_WRx. The pulse width is defined in terms of BLCK periods and is equal to (WSTWR-WSTWEN+1) for asynchronous write cycles.

The choice of the WSTWEN and WSTWR values depend on the address and data setup time and data hold time of the memory device. The STR9 provides at least 1.5 t_{BCLK} of address setup time with WSTEN=1; and by default 0.5 t_{BCLK} of data and address hold time. The WSTWR or pulse width is then set accordingly to meet the data setup time of the memory device

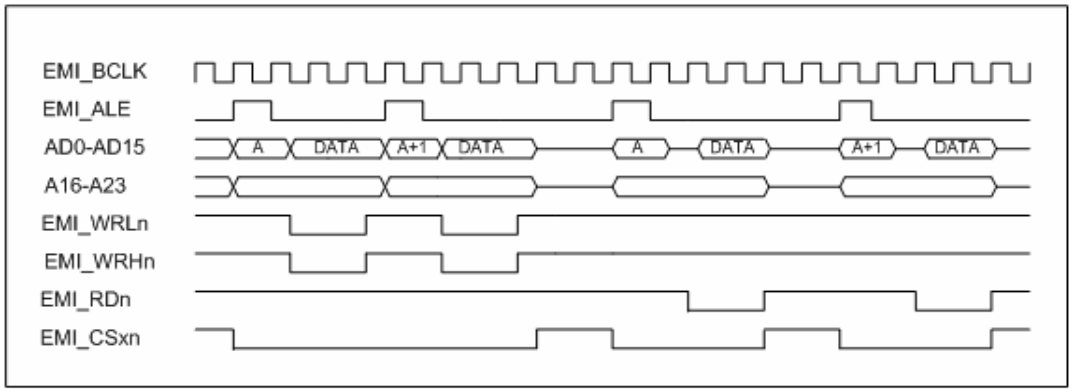
The write bus cycle in *Figure 4.* provides address setup time of 2.5 *t_{BCLK}, data setup time of 1*t_{BCLK} and 0.5*t_{BCLK} of data hold time.

Byte and word access in 16-bit multiplexed mode

The previous sections describe the read and write timings for 16-bit or half word access. The CPU can generate 8-bit or 32-bit access using the assembly instruction of STRB, LDRB or STR, LDR. The 8-bit bus cycle is the same as the 16-bit bus cycles, except AD15-AD8 are not driven during the data phase of the cycle.

For a 32-bit access, the EMI generates two consecutive 16-bit bus cycles. The two bus cycles are identical to the standard 16-bit cycle, the only difference is the EMI_CS chip select signal stays low during the two write cycles. *Figure 5.* shows the bus timings when the CPU executes a 32-bit STR instruction followed by a LDR instruction. Note the EMI_CS signal stays low in the two write bus cycles, but are separated in the two read bus cycles. The two half words that were read in the two LDR read cycles are combined into one word in the EMI block before being transferred to the CPU.

Figure 5. Word (32-bits) write and read bus cycles in 16-bit multiplexed mode



Address shifting in 16-bit multiplexed mode

The internal address (A31-A0) in the ARM core is "byte addressable address", so every address points to a byte location. The internal address is right shifted by one when it is driven to the external 16-bit EMI bus. The resulting EMI address is then pointing to a 16-bit or half word location. There is no need to shift the address by one when connecting the EMI bus to a 16-bit memory device. The EMI A0 address should be connected to the A0 pin of the memory device.

Note: 1 The EMI multiplexed bus can also be configured as an 8-bit bus by setting the memory width bits in the EMI_BCRx register to "00". In this configuration, Port 8 drives the AD7-AD0 address/data bus, while Port 9 drives A15-A8. Please note address A15-A8 must be latched externally as in 16-bit mode.

2 A related software is provided for both SRAM and Flash interfaces already defined.

1.1.2 Non-multiplexed EMI bus configuration

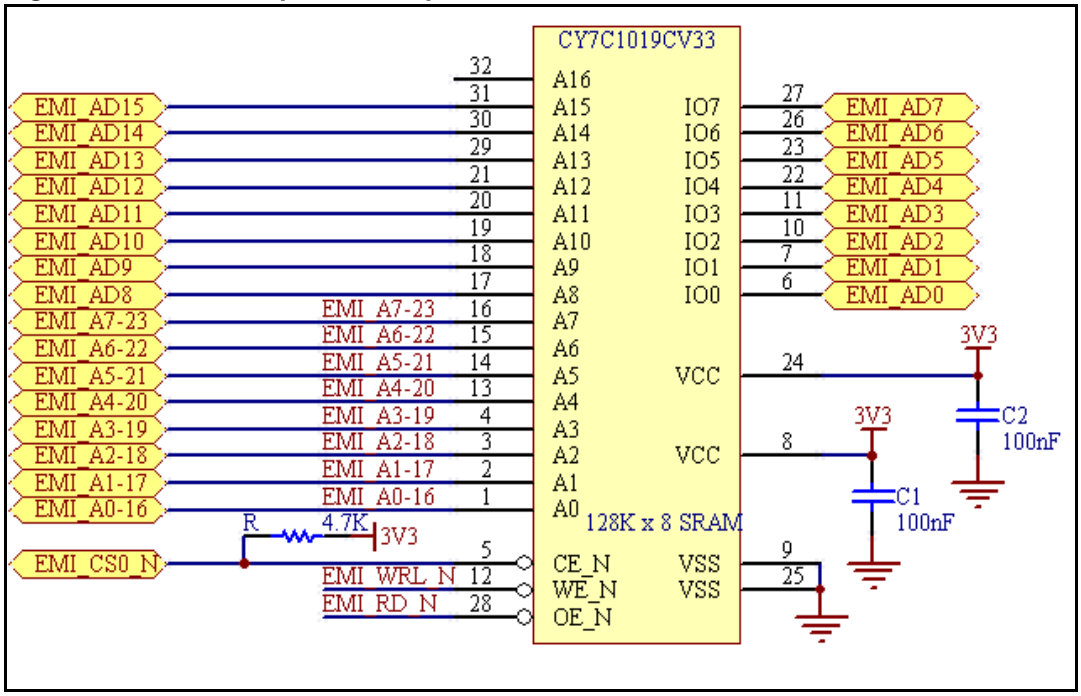
The 8-bit non-multiplexed bus has a different set of bus signal, port assignment and bus timing. Table 2 shows the non-multiplexed bus signal pin assignments.

The non-multiplexed bus has 16 address lines and this limits the memory bank size to no more than 64 KB. *Figure 6.* shows a typical non-multiplexed bus connection to an 8-bit Cypress SRAM.

Table 2. Non-multiplexed bus signals

Signal name	Pin / Port assignment	Signal description
D0-D7	Port 8	Data bus D0-D7
A0-A7	Port 7	Address A0-A7
A8-A15	Port 9	Address A8-A15
Read	EMI_RDn	Read signal
Write	EMI_BWRn	Write signal, same as EMI_WRLn
CS0-CS3	Port 0(P0.4-P0.7) or Port 5 (P5.4-P5.7) or	One chip select for each of the 4 Memory Banks.Can be assigned to any of these two ports.

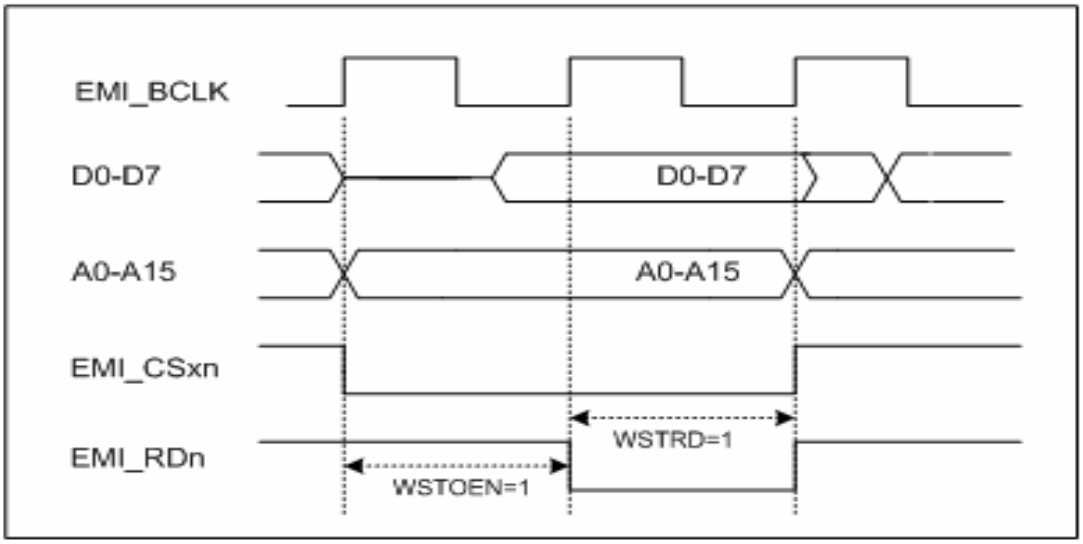
Figure 6. Non-multiplexed bus port connection



Read bus cycle timing configuration

Figure 7 shows a typical Read Bus Cycle. All bus timings are referenced to the internal BCLK clock signal. BCLK clock is only available on an external pin for various usage on the 144 pin BGA package.

Figure 7. Read bus cycle, non-multiplexed bus



EMI_RD Signal Configuration

The EMI_RD signal's timing is controlled by the WSTRD value in the EMI_RCRx register (Read Wait State Control) and the WSTOEN value in the EMI_OECRx register (Output Enable Control).

- **WSTOEN**: Read Enable. WSTOEN specifies the delay between the assertion of the chip select and EMI_RDn goes low. The delay is defined in terms of BCLK clock periods.The minimum WSTOEN value is 0 in a non-Multiplexed bus, EMI_RDn can be active at the same time as the CSx signal.
- **WSTRD**: Read wait state. WSTRD specifies the pulse width, or the rising edge of EMI_RDn. The pulse width is defined in terms of BLCK periods and is = (WSTRD-WSTOEN+1)The choice of WSTRD value depends on the access time of the memory device, slow memory requires more wait states. Typically, the memory access time must meet the following condition:

$$\text{Memory Read access time} < (t_{RAS} + t_{RP} - t_{RDS})$$

where t_{RAS} is the read address setup time, t_{RP} is the EMI_RDn pulse width and t_{RDS} is the data setup time.

The read bus cycle in *Figure 7.* has the following configuration:

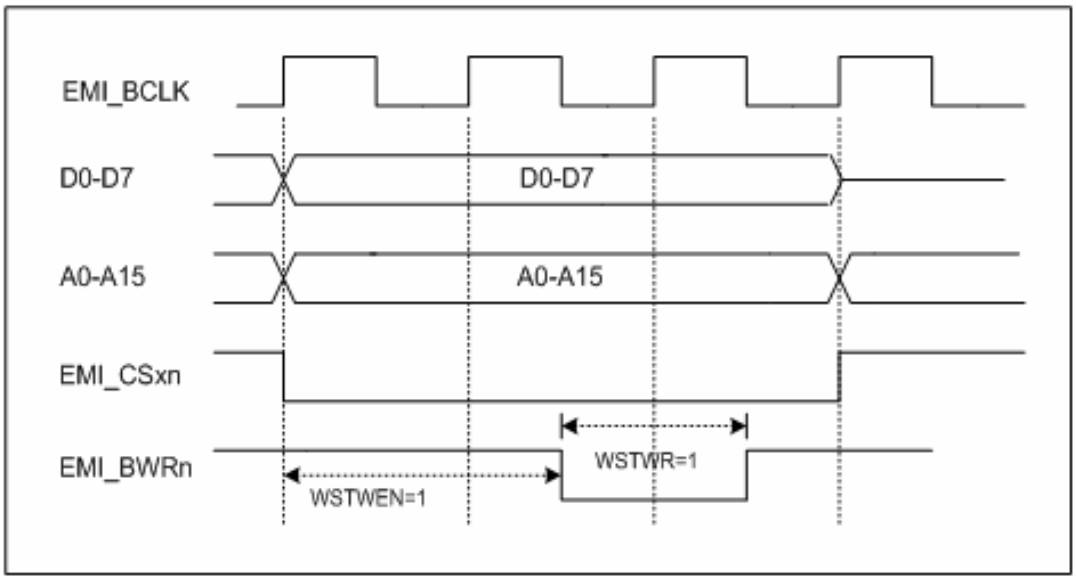
WSTOEN = 1

WSTRD = 1

Write bus cycle timing configuration

Figure 8. shows a typical Write Bus Cycle. The write bus cycle timing differs from the read bus cycle in two ways:

Figure 8. Write bus cycle, non-multiplexed bus



– The write signal (EMI_BWRn) aligns with the falling edge of the BCLK
– EMI_BWRn is terminated half t_{BCLK} before the CSx signal

EMI_BWR signal configuration

The EMI_BWRn signal timing is controlled by the WSTWR value in the EMI_WCRxn register (Write Wait State Control) and the WSTWEN value in the EMI_WECRx (Write Enable Control) register.

- **WSTWEN:** Write Enable. WSTWEN specifies the delay period between the assertion of the CSx chip select and the falling edge of EMI_BWRn. The delay is defined in terms of BCLK clock periods and is (WSTWEN + 1/2) for asynchronous write cycles. The minimum WSTWEN value can be 0 in a non-Multiplexed bus.
- **WSTWR**: Write wait state. WSTWR specifies the pulse width of EMI_BWRn. The pulse width is defined in terms of BLCK period and is equal to (WSTWR-WSTWEN+1) for asynchronous write cycles.

The choice of the WSTWEN and WSTWR values depend on the address setup time, data setup time and data hold time of the memory device. The STR9 provides at least 1.5 t_{BCLK} of address setup time with WSTEN=1; and by default 0.5 t_{BCLK} of data and address hold time. The WSTWR or pulse width is set accordingly to meet the memory's data setup time requirement.

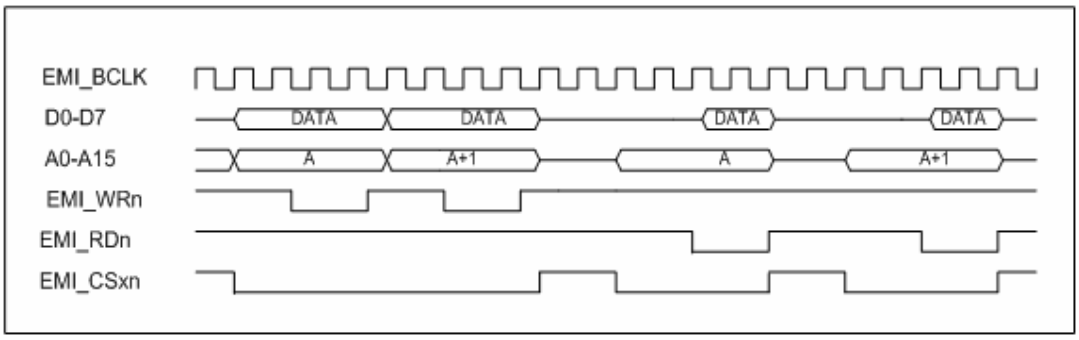
The WSTWEN and WSTWR are set to one in *Figure 8.*, providing address setup time of 1.5*t_{BCLK}, data setup time of 1.5*t_{BCLK} and 0.5*t_{BCLK} of data hold time.

Half word and word access in 8-bit non-multiplexed mode

In the 8-bit non-multiplexed mode, the CPU is able to read or write 16-bit or 32-bit data using the assembly instruction of STRH, LDRH or STR, LDR. For 16-bit access, the EMI generates two consecutive 8-bit bus cycles; while 32-bit access results in 4 consecutive 8-

bit bus cycles. The bus cycle is identical to the standard 8-bit cycle except the EMI_CS chip select signal stays low during the consecutive write cycles. *Figure 9.* shows the bus timings when CPU executes a halfword write instruction (STRH) followed by a LDRH instruction. Note the EMI_CS signal stays low throughout the two write bus cycles. The two bytes that are read in the LDRH cycles are combined into one halfword in the EMI block before being transferred to the CPU.

Figure 9. Halfword write and read bus cycles in 8-bit non-multiplexed mode



Page mode timing

The EMI bus in non-Multiplexed mode can be configured to support memory with Page mode. When in Page mode data are transferred in burst of four, eight or sixteen bytes. The Page mode bit and the data transfer size is specified in the EMI_BCRx register.

The configuration of the EMI_RDn signal timing is the same as in asynchronous read cycles. When page mode is enabled, the read cycle consists of an asynchronous read, followed by multiple burst reads of one byte per BCLK clock. The EMI_RDn and chip select signal will automatically be extended and stay active until the end of the last page read.

If the page mode access time of your memory device plus the EMI data setup time (t_{RDS}) is more than one BCLK period, you need to insert burst read wait state in the EMI_BRDCRx register.

1.2 Other EMI bus configurations

After the bus read/write bus timing configuration is determined, the next step is to set up the Bus Control register and other GPIO port control registers to support the bus type that you selected (Mux or Non_Mux).

1.2.1 Bus control register (BCR)

Each of the memory banks has its own Bus Control register that specifies the bus operating mode. The bits that need to be configured for asynchronous memory read and write are listed in *Table 3.*. Some of the register bits that are dedicated for synchronous bus mode are not included in the table.

Table 3. BCR register configuration bits

Bit	Name	Bit value
Bit 17	SYNCWRITEDEV	0: Asynchronous write device (default) 1: Synchronous device
Bit [11:10]	BRLEN[1:0]	Burst Read Transfer Length. These bits are written by software to define the transfer length for burst or page mode read cycle. Page mode is limited to 4 or 8 transfer. 00: 4-transfer burst read 01: 8-transfer burst read 10: 16-transfer burst read 11: Continuous (synchronous only)
Bit 9	SYNCREADDEV	Synchronous read access device. Access the device using synchronous accesses for reads: 0: Asynchronous device (default). 1: Synchronous device.
Bit 8	BPM	Burst and Page Mode Read Selection This bit is set and cleared by software to select/deselect Burst or Page Mode read. 00: 8-bit 01: 16-bit
Bit[5:4]	MW[1:0]	Memory width define the data bus and memory width of the EMI bus. 00: 8-bit EMI bus 01: 16-bit EMI bus
Bit 3	WP	Write protect - to protect/unprotect the bank from write access. 0: Bank not write protected 1: Bank write protected

1.2.2 EMI port configuration

Ports 7, 8 and 9 at power up are default to GPIO ports; your software has to program the ports to function as an EMI bus. *Table 4.* below shows all possible port function and configuration. The registers that need to be configured include:

SCU_GPIOOUTx - Select the Alternative output function: ALT2 or ALT3

SCU_GPIOTYPEx - Select the port driver: push-pull or open drain

SCU_EMI -Select EMI mode

SCU_SCR0 - Select the multiplexed mode, ALE length and polarity.

Table 4. EMI port configuration

	Port7	Port8 and 9	Port0 (P0.4-P0.7)	Port5 (P5.4-P5.7)
	EMI bus signals:A16-A23 or CS0-CS3 (Multiplexed bus) A0-A7 (Non-multiplexed bus)	**EMI bus signals:AD0-AD15 (Multiplexed bus) D0-D7 & A8-A15 (Non-multiplexed bus)**	**EMI bus signals: CS0-CS3**	**EMI bus signals: CS0-CS3**
Multiplexed Bus Port Register configuration	SCU_GPIOOUT7 [13:0]=to ALT 2 function SCU_GPIOOUT7 [15:14]=to ALT 3 function SCU_GPIOOUT7=0XEAAA (A16-A23 are pin selectable, you only need to configure the pins that are required)	SCU_EMI Register GPIOEMI bit =0 (Set ports 8 and 9 as EMI AD bus)	SCU_GPIOOUT0 [8:15]= to ALT 3 function. SCU_GPIOOUT0= 0XFFxx (CS0-3 are pin selectable, you only need to configure the pins that are required)	SCU_GPIOOUT0 [8:15]= to ALT 3 function. SCU_GPIOOUT0= 0XFFxx. (CS0-3 are pin selectable, you only need to configure the pins that are required)
	SCU_GPIOTYPE7 =0X00 (push-pull)	SCU_GPIOTYPE8,9 =0X00 (push-pull)	SCU_GPIOTYPE0 =0X0x (push-pull)	SCU_GPIOTYPE5 =0X0x (push-pull)
	EMI_Multiplexed mode bit in SCU_SCR0 [6]=0			
Non-Multiplexed Bus Port Register Configuration	SCU_GPIOOUT7 [13:0]=to ALT 2 function SCU_GPIOOUT7 [15:14]=to ALT 3 function SCU_GPIO=0XEAAA SCU_EMI Register	GPIOEMI bit =1 (set ports 8 as data bus and 9 as address bus)	Same as Multiplexed bus	Same as Multiplexed bus
	SCU_GPIOTYPE7 =0X00 (push-pull)	SCU_GPIOType8,9 =0X00 (push-pull)		
	EMI_Multiplexed mode bit in SCU_SCR0 [6]=1			

1.2.3 BCLK clock frequency

The EMI bus clock (BCLK) can be configured to have the same frequency or half the frequency of the AHB bus clock (HCLK). The maximum BCLK frequency supported by the EMI bus is specified in the STR91xFA Data Sheet.

The BCLK frequency is controlled by the EMIRATIO bit in the SCU_CLKCNTR register to divide the HCLK by 1 or by ½.

The BCLK pin is available as an output in BGA package only. The BCLK clock is enabled by setting bit 1 in the SCU_EMI register

1.2.4 Memory bank read and writing timings

The EMI supports 4 external memory banks, up to 64Mbyte in each bank. Depending on the address in the current bus cycle, the EMI activates one of the 4 chip selects (CS0-CS3) to select the targeted device.

Every memory bank has its own set of bus configuration registers and therefore is configured to have its own set of bus timing as well. Usually high speed device like SRAM resides in one bank while slow Flash memory and I/O device reside in another bank. Bus timing can be switched dynamically from one bank to the other bank.

1.3 EMI bus configuration examples

Table 5 lists all the configuration registers and control bits that you need to configure the EMI bus for asynchronous mode. The multiplexed mode example is configured for the 10ns, 16-bit SRAM (IS61LV25616AL) in *Figure 2.* The non-multiplexed mode example is configured for the 20ns, 8-bit SRAM (C1019CV33) in *Figure 6*. The timings in *Table 5* are based on a 96 MHz BCLK clock.

Table 5. EMI Bus configuration examples for asynchronous memory devices

Configuration register	Register bit		Multiplexed 16-bit bus		Non-Multiplexed 8-bit bus	
	Bit	Name	Bit value	Function	Bit value	Function
EMI_BCRx	17	SYNCWRITEDEV	0	Asynchronous write device	0	Asynchronous write device
	9	SYNCREADDEV	0	Asynchronous read device	0	Asynchronous read device
	8	BPM	0	Normal mode (non-burst or page mode)	0	Normal mode (non-burst or page mode)
	5:4	MW	01	16-bit data bus width	00	8-bit data bus width
	3	WP	0	Bank not write protected	0	Bank not write protected
EMI_RCR	4:0	WSTRD	11	Read Wait State 10 ns access time	11	Read Wait State 20 ns access time
EMI_OECR	3:0	WSTOEN	10	EMI_RDn assertion delay	00	EMI_RDn assertion delay
EMI_WCR	4:0	WSTWR	11	Write Wait State	11	Write Wait State
EMI_WECR	3:0	WSTWEN	10	EMI_WRn assertion delay	00	EMI_WRn assertion delay
EMI_ICR	3:0	IDCY	11	Idle Cycle = 3 BCLK	11	Idle Cycle=3 BCLK
EMI_BRDCR	4:0	WSTBRD	00	Burst read wait state=0	00	Burst read wait state=0

Table 5. EMI Bus configuration examples for asynchronous memory devices

Configuration register	Register bit		Multiplexed 16-bit bus		Non-Multiplexed 8-bit bus	
	Bit	Name	Bit value	Function	Bit value	Function
SCU_CLKCNTR	18:17	EMIRatio	00	BCLK=HCLK (96 MHz)	01	BCLK=HCLK (96 MHz)
SCU_SRC0	8	EMI_ALE_LNGT	0	ALE length=1 t_{BCLK}	0	Don't care
	7	EMI_ALE_POLR	1	ALE polarity-active high	0	Don't care
	6	EMI_MULTIPLEXED	0	Multiplexed mode	1	Non-Multiplexed mode

1.4 Executing code from external SRAM vs. internal Flash

The EMI bus is designed for supporting external data storage. However, the CPU can also fetch and execute instruction codes from external memory; the performance would be lower when compared to execution from internal Flash. Please note the Prefetch Queue and Branch Cache are dedicated for internal Flash memory and are not available for external code fetch.

There is a four-word buffer on the AHB bus to facilitate the external code fetch. The buffer is flushed whenever there is a non-sequential fetch, this results in a series of burst fetch requests to the EMI bus to fill up the buffer. Using memory that has burst mode or page mode would enhance the CPU performance.

The ARM instructions are 32-bits, to fetch an instruction the EMI in general generates 1 burst mode read request, of length 4, when the EMI bus is 8-bit wide and 2 read requests for 16-bit bus. *Table 6* below lists the number of BCLK clocks needed to fetch an instruction sequentially from external memory and internal Flash. The 8-bit non-multiplexed EMI bus is configured for page mode or fast SRAM access, which takes one BCLK clock to read a byte. The 16-bit multiplexed bus is configured for the shortest possible read cycle and takes 3 BCLK clocks to read a halfword. As shown in the table, the CPU takes more time to fetch an instruction from external memory and results in lower performance.

Table 6. Number of BCLK clocks required to fetch a sequential instruction

Program code	Read bus cycle length	#of bus cycle per instruction	#of BCLK between cycles	#of BCLK per instruction fetch
External memory 8-bits non-mux bus (page mode)	1 BCLK Clock	4	2	(1BCLK*4)+2=6
External memory 16-bit mux bus (SRAM)	3 BCLK Clock	2	2	(3BCLK+2)*2=10
Internal Flash memory 32-bit bus	1 BCLK Clock	1	0	1

2 Interfacing with synchronous memory

STR91xFA has up to 96 KB of internal SRAM which is enough for most applications. For systems that need large amount of SRAM, an attractive alternative is to use PSRAM (Pseudo Static RAM). PSRAM is widely used in mobile phone, PDA and other portable electronic products, mainly due to its high density, high performance, low power and low cost. It takes more work to interface and configure a PSRAM than the standard SRAM, but it is worth the effort. Please note the STR91xFA with the 144-ball BGA package is the only device that has the additional EMI signals to interface to a PSRAM.

This Part of application note describes how to configure the STR91xFA EMI bus to access a PSRAM. Topics include:

- Connecting a PSRAM to the EMI bus
- Asynchronous mode configurations and timings
- Burst mode configurations and timings
- High Speed data transfer using the DMA Controller

Please refer to *Section 1* to get familiar with the basic EMI bus timings and configurations.

There are many PSRAM suppliers to choose from, device with density ranging from 16 Mb to 128Mb, and clock rate from 66 MHz to 133 MHz. The PSRAM used in this application note is a Micron Technology 64 Mb Async/Page/Burst CellularRAM^{TM} 1.5 Memory (part # MT45W4MW16BCGB-708 WT). It is organized as 4M x 16 with a clock rate of up to 80 MHz. This AN includes a brief overview of the PSRAM; it is recommended that the reader refer to the Data Sheet for detail descriptions.

2.1 PSRAM overview

The key functional block of the MT45W4M (MT45W4MW16BC), as shown in *Figure 10 on page 21*, consists of a 4096K x 16 DRAM memory array, the Control Logic, the Configuration registers and the Input/Output Buffer. The Bus Configuration Register (BCR) controls the operating modes and timings of the MT45W4M.

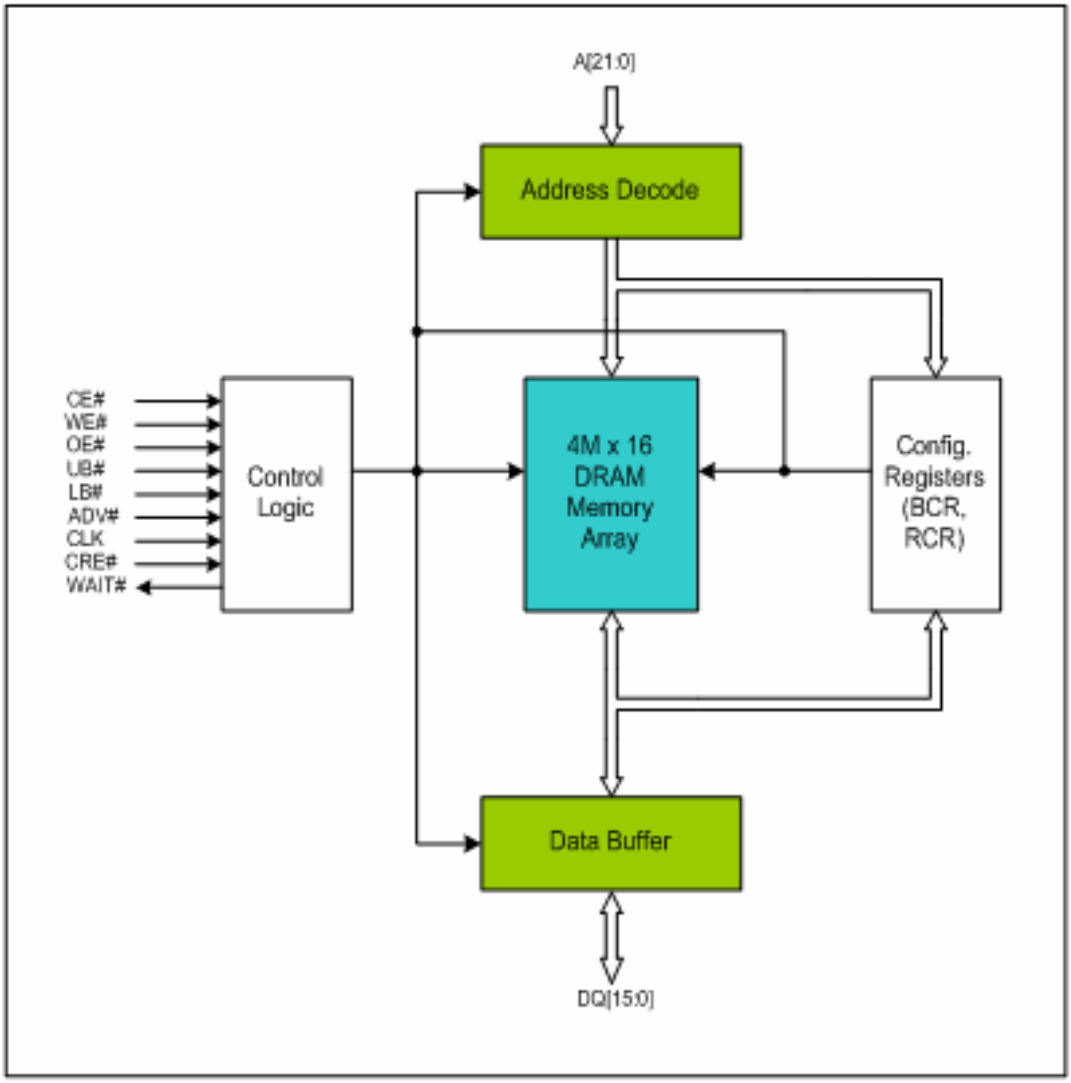
2.1.1 Bus interface signals

The MT45W4M is usually connected to a non-multiplexed bus, with a 16-bit data bus and 23 address inputs. However, it can be configured to interface to a multiplexed bus like the STR91xFA EMI bus. In addition to the standard SRAM control signals such as CE, OE, WE, UB and LB, the PSRAM has four additional signals that are required for synchronous (burst) mode operation and are described in *Table 7*.

Table 7. PSRAM control signals

Signal name	Type	Description
CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK must be static LOW during asynchronous access READ and WRITE operations
ADV#	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations.
CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR registers, and READ operations access the RCR, BCR, or DIDR registers.
Wait	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted at the end of a row. WAIT is asserted and should be ignored during asynchronous mode.
CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
LB#	Input	Lower byte enable. DQ[7:0]
UB#	Input	Upper byte enable. DQ[15:8]

Figure 10. MT45W4MW16BC functional block diagram

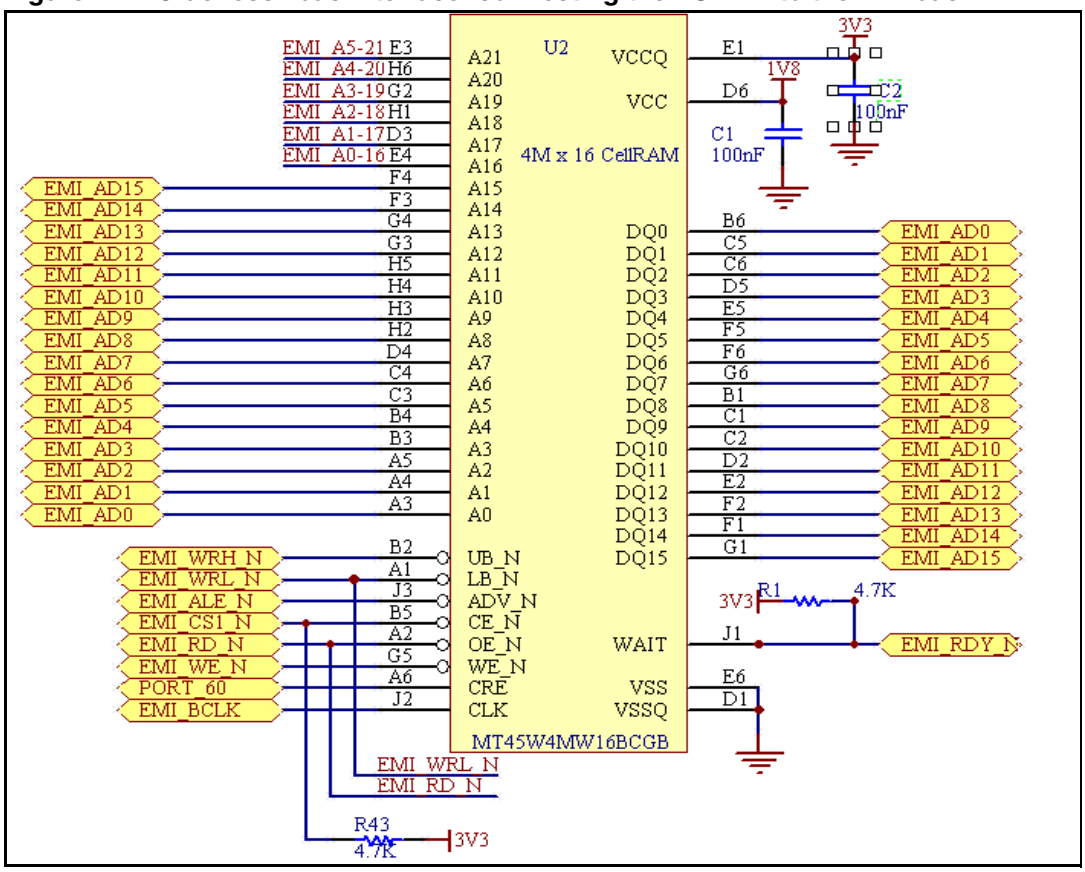


2.2 Connecting the EMI bus to a PSRAM

The EMI bus operates in 16-bit multiplexed mode. The PSRAM itself has a non-multiplexed bus interface with separate address and data bus inputs. However, the ADV# signal in the PSRAM is able to latch the address internally and the address is not required to stay throughout the bus cycle. The EMI's multiplexed bus takes advantage of this feature, it drives the address and the ADV# in the address phase of the bus cycle. After the address is latched by PSRAM, the EMI then drives data out in a write cycle or floats the bus in a read cycle.

Figure 11. shows the EMI bus connection to a PSRAM. Port 7 drives the non-multiplexed address A[21:16]. A[23:22] pins are not needed, the P5.1 and P6.0 pins are configured to drive the chip select signals CS1 and the CRE signal respectively. CRE (Configuration Register Enable) must be high when the EMI is accessing the configuration registers of the PSRAM. The CS1 is generated automatically by the EMI when accessing the PSRAM, but CRE is a software controlled GPIO signal and must be set before you can access the PSRAM registers. Please note no logic gate is needed in the EMI/PSRAM interface.

Figure 11. Glue-less" bus interface: connecting the PSRAM to the EMI bus



2.2.1 PSRAM bus operating modes

The MT45W4M supports multiple configurations in Asynchronous mode, Synchronous burst mode, and Page mode. Page mode requires a non-multiplexed bus connection and is not compatible with the EMI bus.

In this application note, only the PSRAM configurations that are compatible to the EMI bus are discussed. The EMI bus supports both the asynchronous and synchronous mode; The mode can be changed by software on the fly to match the PSRAM bus cycle. Typically, Synchronous burst mode is recommended for high speed data transfer, while asynchronous mode is used by the EMI bus to:

- Read or write a single halfword to the PSRAM
- Configure the PSRAM registers

Asynchronous mode

After power up the MT45W4M is default to asynchronous mode. There are variations of asynchronous mode, the one that the EMI bus can support is the "Asynchronous access Using ADV". The read bus timing is shown in *Figure 12.* Please note the address inputs are latched by the rising edge of ADV# and become "don't care" after the latching. The PSRAM WAIT# output signal is not used in asynchronous mode and is ignored by the EMI.

Figure 12. PSRAM asynchronous read using ADV (EMI_ALE)

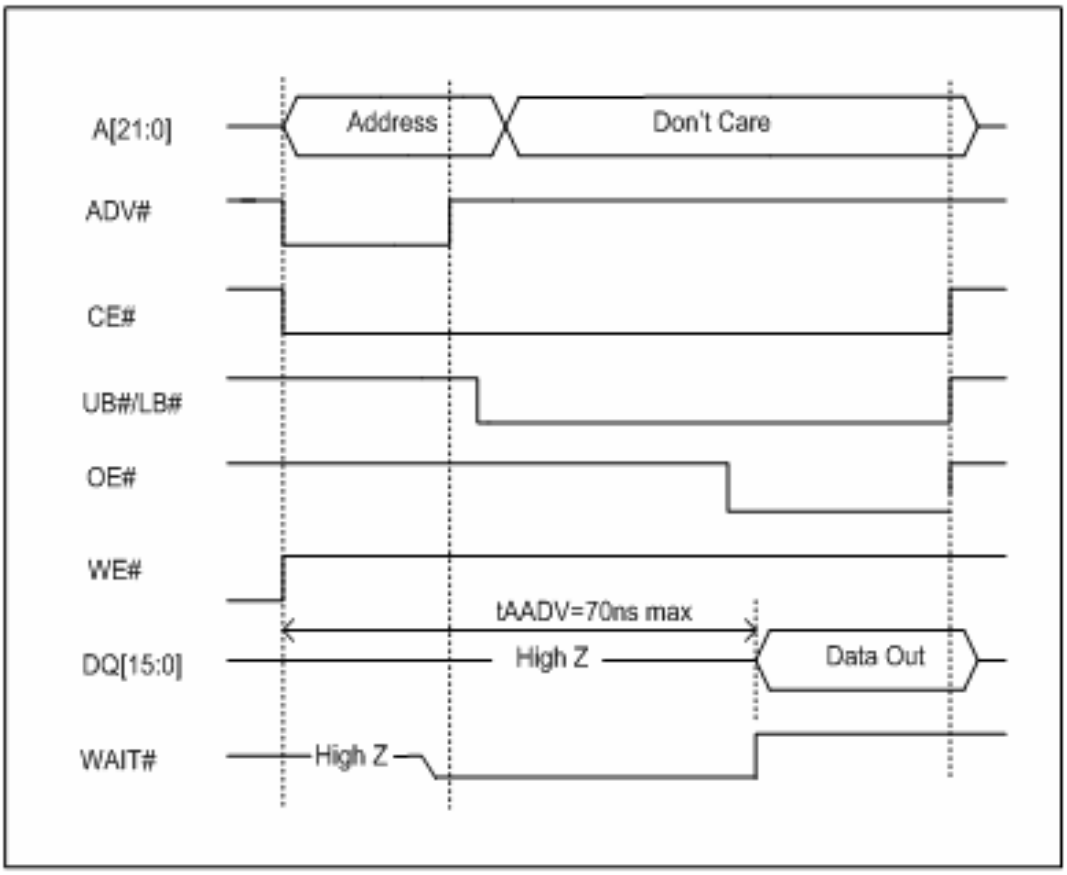
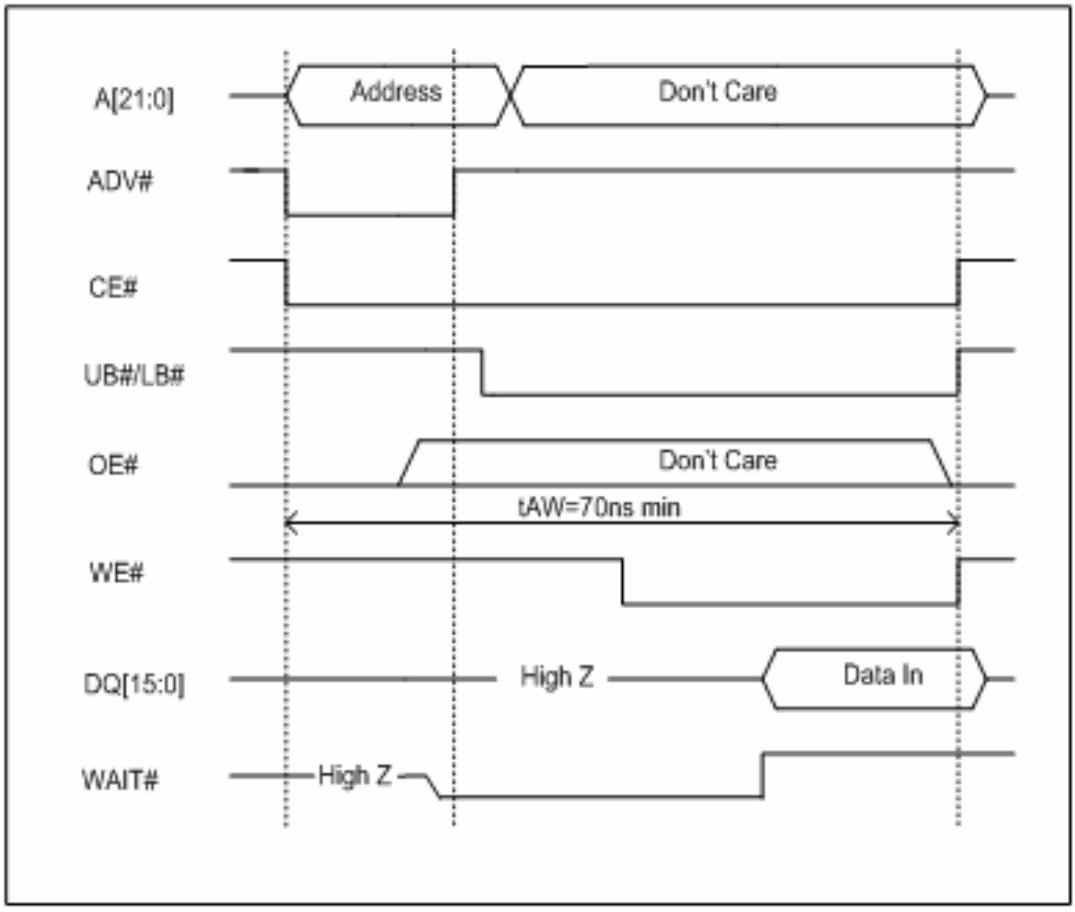


Figure 12. and *Figure 13.* show typical PSRAM asynchronous read and write bus cycles using ADV# to latch the address. The EMI bus is configured to match the PSRAM timing and input signal waveform. The EMI_ALE is configured as active low with a 2 t_{BCLK} pulse width to meet the ADV# address setup and hold time. The EMI_UBn and EMI_LBn are enabled by setting the Byte_En bit in the SCU_EMI register and the BLE bit in the EMI_BCR register. The EMI_WEn and EMI_RDn are configured with enough wait state to meet the 70ns of read and write access time of the MT45W4M.

Note: Setting the EMI_ALE_LNGT bit in SCU_SCR0 selects an EMI ALE length of Two clock cycles in asynchronous mode but one and a half clock cycles in synchronous Mode.

Figure 13. PSRAM asynchronous write using ADV# (EMI_ALE)



EMI bus configuration for asynchronous mode

Table 8 shows the EMI bus registers and control bits that are required for the STR91xFA to access the PSRAM in asynchronous mode. The burst mode parameters are included in the table but are not don't cares in asynchronous mode

The key parameters that you have to configure are:

1. BCLK clock frequency, which is set to 80 MHz to match the MT45W4M's maximum clock rate. Note the BCLK pin is disabled in asynchronous mode.
2. Select the EMI_WEn, EMI_UBn, EMI_LBn signals for 16-bit write
3. Set EMI_RDn timing (WSTRD=5, WSTOEn=4), EMI_WEn timing (WSTWR=5, WSTWEn=0). The read and write timings should meet the MT45W4M's 70 ns access time.
4. Set EMI_ALE to 2 t_{BCLK} wide and active low.
5. Configure Port5,6, 7, 8 and 9 as EMI bus port. Set Port 6 pin P6.0 as CRE output and Port 5 pin P5.1 as CS1 chip select.

Table 8. EMI and port register configuration for PSRAM async mode (80 MHZ BCLK)

EMI configuration register	Register bit		Multiplexed 16-bits asynchronous mode	
	Bit	Name	Bit value	Function
EMI_BCRx (maintain reserved bits' default value)	19:18	BWLEN	00	Burst write transfer length
	17	SYNCWRITEDEV	0	Asynchronous write device
	16	BMWrite	0	Burst mode write disabled
	11:10	BRLEN	00	Burst read transfer length
	9	SYNCREADDEV	0	asynchronous read device
	8	BPM	0	Normal mode (non burst or page mode)
	5:4	MW	01	16-bit data bus width
	3	WP	0	Bank not write protected
	0	BLE	1	Byte Lane Enable
EMI_RCR	4:0	WSTRD	101	Read Wait State = 5 70 ns PSRAM access time
EMI_OECR	3:0	WSTOEN	100	EMI_RDn assertion delay = 4
EMI_WCR	4:0	WSTWR	101	Write Wait State = 5
EMI_WECR	3:0	WSTWEN	000	EMI_WRn assertion delay = 0
EMI_ICR	3:0	IDCY	011	Idle Cycle = 3 BCLK
EMI_BRDCR	4:0	WSTBRD	000	Burst read wait state= 0
SCU_EMI	2	BYTE_EN	1	Enable EMI_UBn and LBn signals
	1	BCLK_EN	1	Disable BCLK output
	0	GPIOEMI	1	Set Port 8/9 as EMI bus
SCU_CLKCNTR	18:17	EMIRatio	00	BCLK=HCLK (80 MHz)

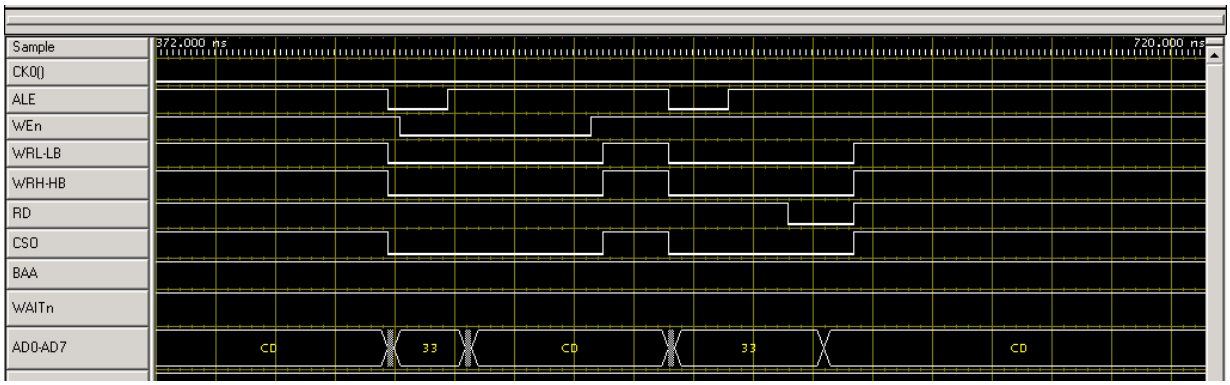
Table 8. EMI and port register configuration for PSRAM async mode (80 MHZ BCLK)

EMI configuration register	Register bit		Multiplexed 16-bits asynchronous mode	
	Bit	Name	Bit value	Function
SCU_SCR0	8	EMI_ALE_LNGT	1	ALE length=2 t_{BCLK}
	7	EMI_ALE_POLR	0	ALE polarity-active low
	6	EMI_MULTIPLEXED	0	Multiplexed mode
SCU_GPIOTYPE [5:9]	7:0	Push-pull	0x00	Configure Port 5,6,7,8 and 9 as push-pull
SCU_GPIOOUT7	15:0	Output Function	0x0AAA	Set Port 7 pins P7.5-P7.0 as A[21:16]
SCU_GPIOOUT6	15:0	Output Function	0x0001	P6.0 as GPIO out
SCU_GPIOOUT5	15:0	Output Function	0x0C00	Set P5.5 as CS1

EMI read and write asynchronous bus cycle

The EMI configurations in *Table 8* will generate the write and read timing as shown in *Figure 14*. The EMI_ALE signal, which indicates the start of a bus cycle, is connected to the ADV# pin. The MT45W4M latches the address "33h" at the rising edge of EMI_ALE, and then latches the write data "CDh" at the rising edge of EMI_WEn. Please note the MT45W4M ignores the inputs on its address pins after the address latching. This allows the EMI to take over the AD bus and drive the data "CDh".

Figure 14. EMI bus write and read bus cycles in asynchronous mode



Note: For your reference an asynchronous software example is delivered with this application note.

Synchronous burst mode

PSRAM BCR register configuration for synchronous burst mode

For a system that requires high speed data transfer, you have to configure the PSRAM and the EMI bus to operate in synchronous burst mode. Before writing to the PSRAM BCR (Bus Configuration Register) to set up burst mode, the CRE signal must be driven high by writing a 1 to GPIO pin P6.0. After the configuration, CRE must be set to low to return to normal bus operation. The BCR configuration bus cycle operates in asynchronous mode and is described in the previous section.

Table 9. shows the BCR configuration bit values. When writing to BCR, the register gets the write data value not from the data bus input, but rather from the address lines A[21:0]. The BCR data must then be embedded in your EMI address. Please note the internal 32-bit ARM address is a byte aligned address. Before it is driven to the EMI bus, the address lines are right shifted by one and is converted to a half-word (16-bit) aligned address.

Table 9. PSRAM bus configuration register bit setting for burst mode

Register bit	Bit name	Bit value	Function
21:20	reserved	0	
19:18	Select BCR	10	Select BCR as target register
17:16	reserved		
15	Operating mode	0	Synchronous Burst access(default=1, asynchronous access)
14	Initial latency	1	Fixed Latency; first access time in a burst cycle
13:11	Latency counter	100	Set to code 4
10	Wait polarity	0	Active low
9	reserved	0	
8	Wait configuration	1	Asserted one data cycle before delay (default)
7:6	reserved	00	
5:4	Drive strength	01	½ (default)
3	Burst Wrap	1	Burst no wrap (default)
2:0	Burst length	111	Continuous Burst (default)

After the PSRAM BCR register is configured for burst mode, the EMI bus also need to be re-configured from asynchronous to synchronous burst mode. An EMI burst cycle consists of an asynchronous access to read or write the first halfword and then followed by multiple burst cycles, where each data transfer takes only one BCLK clock to complete. The timings of the first access in a burst cycle are the same as defined in asynchronous mode.

EMI bus configuration for synchronous burst mode

Table 10 shows the EMI bus registers and control bits for synchronous mode operation. The configuration is similar to the asynchronous mode, with the following additional bits are set in the EMI_BCR register:

1. Enable synchronous mode
2. Enable BCLK clock
3. Enable burst read and write
4. Burst read data transfer length
5. Burst write data transfer length

Table 10. EMI and port register config. for PSRAM sync mode (80 MHZ) BCLK)

EMI configuration register	Register bit		Multiplexed 16-bits asynchronous mode	
	Bit	Name	Bit value	Function
EMI_BCRx (maintain reserved bits' default value)	19:18	BWLEN	11	Burst write transfer length: Continuous Burst
	17	SYNCWRITEDEV	1	synchronous write device
	16	BMWrite	1	Burst mode write enabled
	11:10	BRLEN	00	Burst read transfer length: Continuous Burst
	9	SYNCREADDEV	0	synchronous read device
	8	BPM	0	Burst mode read
	5:4	MW	01	16-bit data bus width
	3	WP	0	Bank not write protected
	0	BLE	1	Byte Lane Enable
EMI_RCR	4:0	WSTRD	101	Read Wait State = 5 70 ns PSRAM access time
EMI_OECR	3:0	WSTOEN	100	EMI_RDn assertion delay =4
EMI_WCR	4:0	WSTWR	101	Write Wait State =5
EMI_WECR	3:0	WSTWEN	000	EMI_WRn assertion delay =0
EMI_ICR	3:0	IDCY	011	Idle Cycle = 3 BCLK
EMI_BRDCR	4:0	WSTBRD	000	Burst read wait state=0
SCU_EMI	2	BYTE_EN	1	Enable EMI_UBn and LBn signals
	1	BCLK_EN	0	Enable BCLK output
	0	GPIOEMI	1	Set Port 8/9 as EMI bus
SCU_CLKCNTR	18:17	EMIRatio	00	BCLK=HCLK (80 MHz)
SCU_SCR0	8	EMI_ALE_LNGT	1	ALE length=1.5 t_{BCLK}
	7	EMI_ALE_POLR	0	ALE polarity-active low
	6	EMI_MULTIPLEXED	0	Multiplexed mode
SCU_GPIOTYPE [5:9]	7:0	Push-pull	0x00	Configure Port 5,6,7,8 and 9 as push-pull

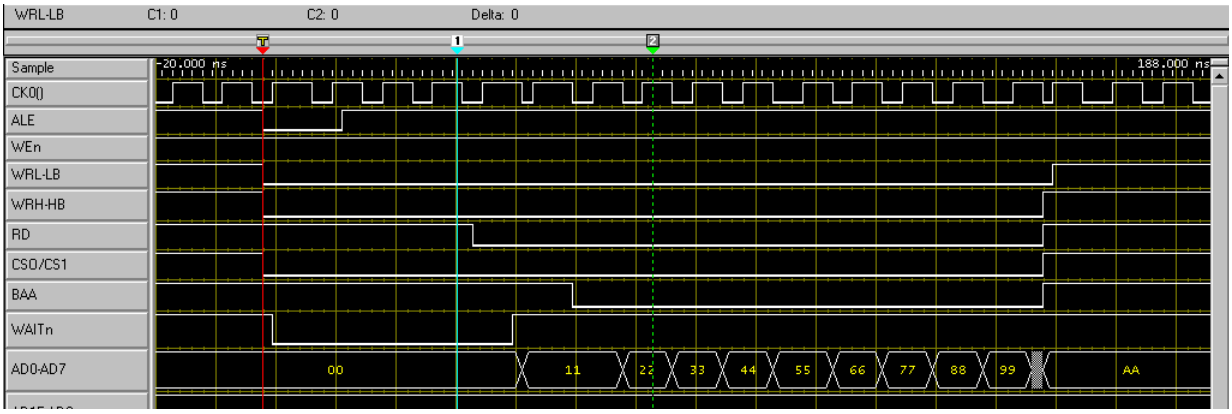
Table 10. EMI and port register config. for PSRAM sync mode (80 MHZ) BCLK)

EMI configuration register	Register bit		Multiplexed 16-bits asynchronous mode	
	Bit	Name	Bit value	Function
SCU_GPIOOUT7	15:0	Output Function	0x0AAA	Set Port 7 pins P7.5-P7.0 as A[21:16]
SCU_GPIOOUT6	15:0	Output Function	0x0001	P6.0 as GPIO out
SCU_GPIOOUT5	15:0	Output Function	0x0C00	Set P5.5 as CS1

EMI burst read bus cycle

In synchronous mode, the PSRAM latches the address at the rising clock edge while ALE is low. The write signal WEn must be high when the address is sampled to start a read bus cycle. The STR91xFA always reads in 16-bit with the UB/LB byte select signals staying low for the entire cycle. For the initial access of the read cycle, the PSRAM is set up for fixed latency with a latency counter value of 4. The read wait state WSTRD in the EMI is set up to 5 to match the PSRAM timing. Burst read cycle starts after the first initial access and the PSRAM is driving data out every BCLK clock until the end of the chip select signal CSx. The timing in *Figure 15.* shows a burst read cycle initiated by STR91xFA while executing a Load Multiple instruction.

Figure 15. EMI read bus cycle in burst mode

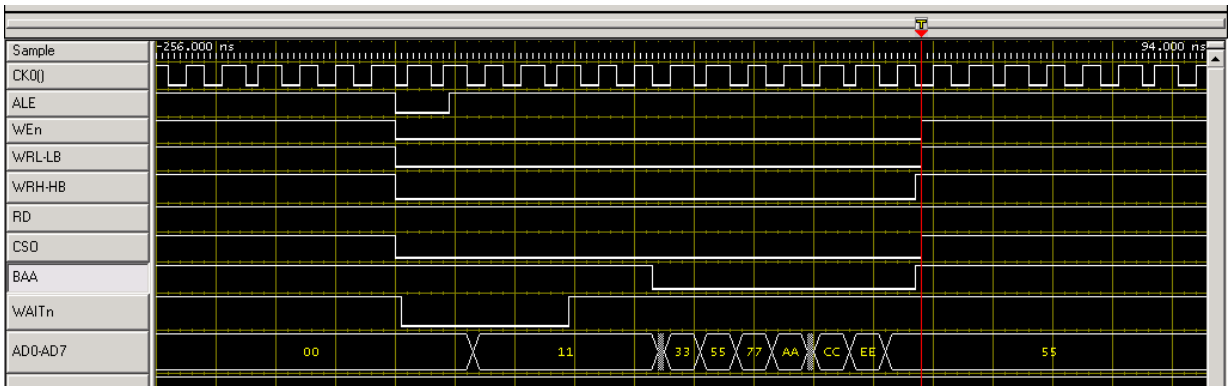


EMI burst write bus cycle

In synchronous mode the write signal WEn is sampled at the same time the address is latched. This requires the write assertion delay WSTWEN to be "0" so WEn will stay low at the beginning of the bus cycle. STR91xFA always writes to PSRAM in 16-bit mode and the two byte-select signals UB/LB are low for the entire write cycle.

The latency counter in the BCR register defines when the write data is sampled by PSRAM, and this time has to match the EMI write timing so the first write data is latched at the right clock edge. In this example the write wait state WSTWR is set to 5 and the latency counter is set to 4. Refer to the MT45W4M data sheet for the timing details.

Figure 16. EMI write bus cycle in burst mode



Note: The EMI_BAA signal is not needed for the PSRAM interface.

DMA for high speed data transfer

STR91xFA has up to 96 KBytes of internal SRAM for data storage. DMA is the most efficient way to transfer data between internal SRAM and the external PSRAM. The advantages of using the DMA Controller are:

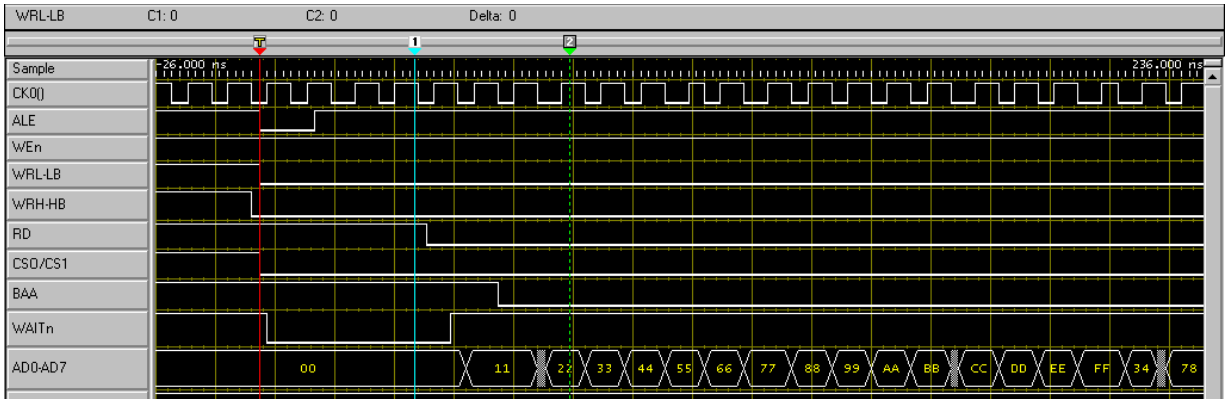
– Reduce the load on CPU
– Data is transferred in high speed burst mode

You can select one of the eight available DMA channel for data transfer. The transfer is of the memory-to-memory type. Therefore, the DMA channel commences transfers without DMA requests.

For burst Write, the source address is the internal SRAM and the destination address is the external PSRAM.For more details user can refer to the PSRAM synchronous example accompanied with the current application note which use DMA to generate burst writes in the external PSRAM.

For burst read, the source address is the PSRAM and the destination address is the internal SRAM. The continuous burst read cycle in Figure 8 supports a data transfer rate of one BCLK clock period per halfword. Note the chip select CSx and EMI_RDn stay low until the burst cycle is completed.

Figure 17. EMI continuous burst read during DMA



3 Revision history

Table 11. Document revision history

Date	Revision	Changes
13-Dec-2007	1	Initial release.