PoE Powered Device and 12V/600mA No-Opto Flyback DC-DC Converter Using the MAX17690 and MAX5969B

MAXREFDES1177

Introduction

Power over Ethernet (PoE) is a technology that allows network cables to deliver power to a powered device (PD) through power-sourcing equipment (PSE) or midspan, and has many advantages over traditional methods of delivering power. PoE allows power and data to be combined, removing the need for altering the AC mains infrastructure and can be installed by non-electricians. PoE is an intelligent system designed with protection at the forefront, preventing overload, underpowering, and installation errors, while allowing simple scalability and reliability.

The MAX17690 implements an innovative algorithm to accurately determine the output voltage by sensing the reflected voltage across the primary winding during the flyback time interval. By sampling and regulating this reflected voltage when the secondary current is close to zero, the effects of secondary-side DC losses in the transformer winding, the PCB tracks, and the rectifying diode on output voltage regulation can be minimized. The MAX17690 also compensates for the negative temperature coefficient of the rectifying diode.

Other features include the following:

- IEEE 802.3af/at Compliance
- Thermally Enhanced, 3mm × 3mm, 10-Pin TDFN Package (MAX5969B)
- 30V to 60V Input Voltage Range
- Programmable Switching Frequency from 50kHz to 250kHz
- Programmable Input Enable/UVLO Feature
- Programmable Input Overvoltage Protection
- Adjustable Soft-Start
- 2A/4A Peak Source/Sink Gate Drive Capability
- Hiccup Mode Short-Circuit Protection
- Fast Cycle-by-Cycle Peak Current Limit
- Thermal Shutdown Protection
- Space-Saving, 16-Pin, 3mm × 3mm TQFN Package
- -40°C to +125°C Operating Temperature Range

Hardware Specification

This reference circuit consists of the MAX5969B PD controller and an isolated no-opto flyback DC-DC converter using the MAX17690 to demonstrate a 12V DC output application. A 1GbE RJ45 magnetic jack is also included as well as two diode bridges for separating data and DC power provided by an endspan or midspan PoE system. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplifies layout. The power supply delivers up to 600mA at 12V. Table 1 is an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Power Range	P_{IN}	6.49W	12.95W
Undervoltage Lockout Voltage	V_{UVLO}		29V
Input Voltage	V_{IN}	30V	60V
Frequency	f_{SW}	143.41kHz	
Peak Efficiency at Full Load	η_{MAX}	88%	
Efficiency at Minimum Load	η_{MIN}	60%	
Output Voltage	V_{OUT}	12V	
Output Voltage Ripple	ΔV_O	120mV	
Maximum Output Current	I_{OUT}	600mA	
Maximum Output Power	P_{OUT}	7.2W	

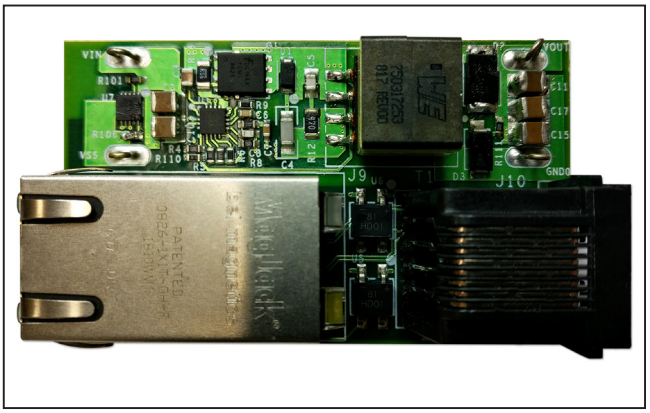

Figure 1. MAXREFDES1177 hardware.

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed technical guide to designing a complete interface for a PD to comply with the IEEE 802.3af/at standard in a PoE, class 3 system and an isolated no-opto flyback DC-DC converter using Maxim's MAX17690 controller. The power supply has been built and tested.

MAX5969B PD Interface

A PoE system delivers power and data to an end device (PD) typically through an RJ45 cable power from an endspan (PSE) (Figure 2) or a midspan (Figure 3). The power is separated from the data through diode bridges to deliver a typical 48V for efficient power transfer, which is low enough to be considered a safe voltage, removes the need to rewire AC mains, and saves cost.

Although this voltage is safe for humans, it still can damage equipment if not properly delivered. This is where MAX5969B classification is required, ensuring the equipment can handle the power delivery. Before the PSE can enable power to a connected IP camera or other PD, it must perform a signature detection.

Signature Detection

Signature detection uses a lower voltage to detect a characteristic signature of IEEE-compatible PDs (a 24.9kΩ resistance). See Figure 4. Once this signature has been detected, the PSE knows that higher voltages can be safely applied. The PSE applies two voltages on V_{IN} in the range of 1.4V to 10.1V (1V step minimum) and then records the current measurements at the two applied voltages. The PSE then computes the change in current when each voltage was applied (ΔV/ΔI) to ensure the presence of the 24.9kΩ signature resistor.

Classification

In classification mode, the PSE classifies the PD based on the power consumption required. (The IEEE 802.3af/at standard defines only Class 0 to 4 and Class 5 for any special requirement.)

An external resistor (R_{CLS}) of 43.7Ω connected from CLS to V_{SS} sets the classification current. The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced from the PSE. When the PSE applies a voltage between 12.6V and 20V, the MAX5969A/MAX5969B exhibit a current of 26mA to 30mA.

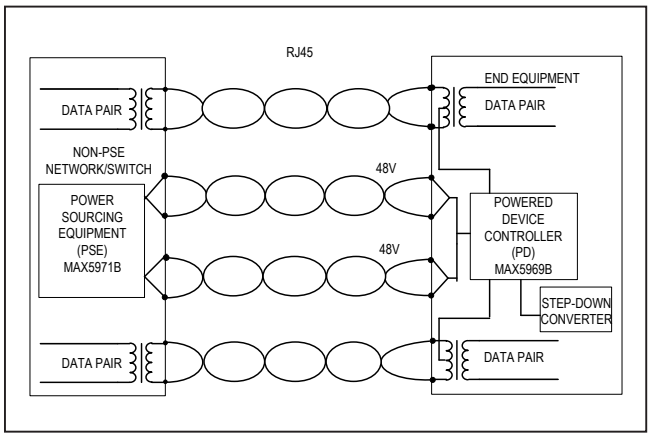

Figure 2. PoE endspan power injector.

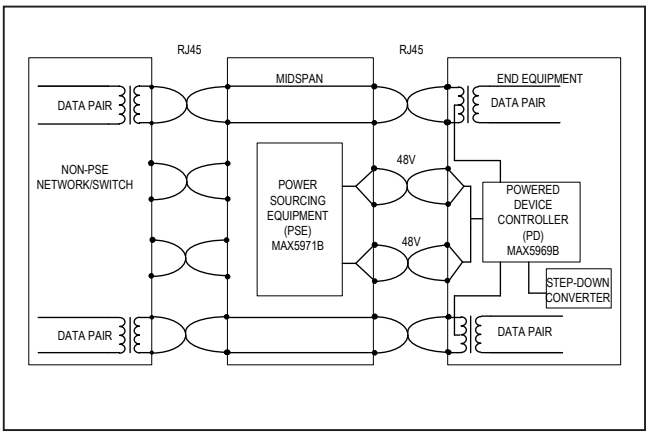

Figure 3. PoE midspan power injector.

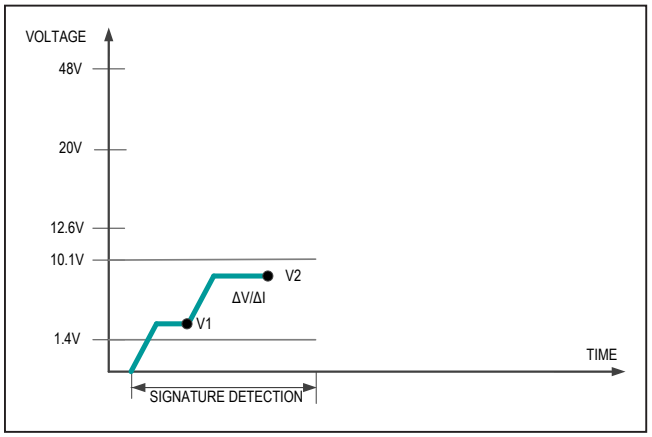

Figure 4. Signature detection.

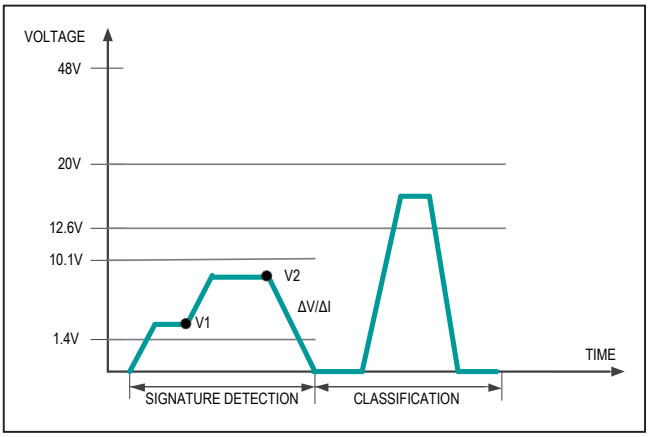

Figure 5. Classification.

The PSE uses the classification current information to classify the power requirement of the PD (MAX5969B).

The classification current includes the current drawn by R_{CLS} and the supply current of the MAX5969A/MAX5969B so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode (Figure 5).

Power Mode

The final stage after detection and classification of a newly connected PD is to enable power. The 48V supply from the PSE is connected to the PD through the RJ45 cable. Once enabled, the PSE continues to monitor how much current is being delivered to the PD and cuts power to the cable if the power drawn is not within the correct range. This protects the PSE against overload, underpowering and ensuring that the PSE is disconnected from the cable if the PD is unplugged or faulted. See Figure 6.

The MAX5969B enters power mode when V_{IN} rises above the undervoltage lockout threshold (V_{ON}). Note that V_{ON}/V_{OFF} = 38.6V/31V for the MAX5969B. When V_{IN} rises above V_{ON}, the MAX5969B turns on the internal n-channel isolation MOSFET to connect GND to RTN. The open-drain power-good output (PG) remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. The P_{GOOD} open-drain output is also connected to three small-signal transistors to prevent the DC converters from powering up before the power from the PD is allowable.

Design Considerations for MAX5969B

Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5969A/MAX5969B. Use large SMT component pads for power dissipating devices such as the MAX5969A/MAX5969B and the external diodes. Use short and wide traces for high-power paths.

The MAX5969B enters undervoltage lockout when the input voltage drops below 31V. When the input drops below this value, the isolation MOSFET switches off, disconnecting the 48V from the buck converters. The MAX5969B exits undervoltage lockout when the input exceeds 38.6V, where the isolation MOSFET switches on again, connecting the MAX17690 Flyback Converter.

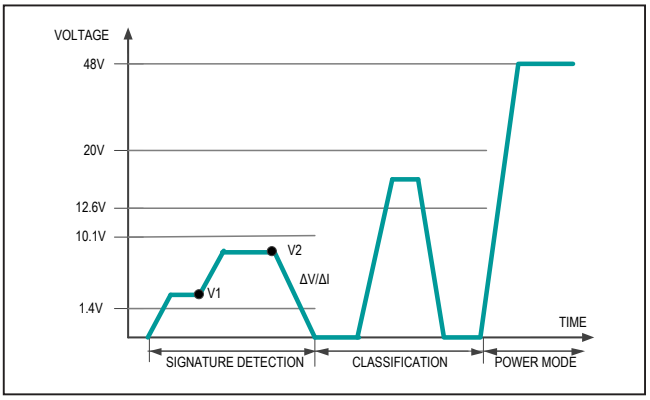

Figure 6. Power enabled.

Table 2. Setting Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af/at PSE CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	619	12.6 to 20	0	4	0	5
1	0.44 to 3.94	117	12.6 to 20	9	12	8	13
2	3.84 to 6.49	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	> 25.5	21.3	12.6 to 20	52	64	—	—

**V_{IN} is measured across the MAX5969A/MAX5969B input V_{DD} to V_{SS}.*

Designing the No-Opto Flyback Converter Using MAX17690

The converter design process can be divided into three parts: the power stage design, the setup of the MAX17690 no-opto flyback controller, and closing the control loop. This document is intended to complement the information contained in the MAX17690 data sheet.

The following design parameters are used throughout this document:

SYMBOL	FUNCTION
V_{IN}	Input voltage
V_{UVLO}	Undervoltage turn-on threshold
V_{OVI}	Overvoltage turn-off threshold
t_{SS}	Soft-start time
V_{OUT}	Output voltage
ΔV_O	Steady-state output ripple voltage
I_{OUT}	Output current
P_{OUT}	Nominal output power
$\eta_{(MAX)}$	Target efficiency at maximum load
$\eta_{(MIN)}$	Target efficiency at minimum load
P_{IN}	Input power
f_{SW}	Switching frequency
D	Duty cycle
n_{SP}	Secondary-primary turns ratio

Throughout the design procedure reference is made to the schematic. See the *Design Resources* section.

Part I: Designing the Power Components

Step 1: Calculate the Minimum Turns Ratio for the Flyback Transformer

The secondary-primary turns ratio, n_{SP}, and the duty cycle, D, for the flyback converter are related by the flyback DC gain function as follows:

$$n_{SP} = \frac{V_{OUT}}{V_{IN}} \times \left(\frac{1-D}{D}\right)$$

The converter's absolute minimum input voltage is the undervoltage lockout threshold (V_{IN} falling) which is programmed with a resistor divider for the MAX17690. At this voltage, and at maximum output power, D should be less than or equal to 66% (maximum duty cycle at which the MAX17690 can operate) to ensure reliable operation of the converter. For the current design the undervoltage lockout threshold (V_{IN} falling) occurs at 29V, so with D set at 66% the absolute minimum turns ratio, $n_{SP(MIN)}$, for the flyback transformer is calculated:

$$n_{SP(MIN)} = 0.24$$

This transformer turns ratio assumes that there are no DC voltage drops in the primary and/or secondary circuits. In practice a larger transformer turns ratio must be chosen to account for these DC voltage drops. For the current design a transformer turns ratio n_{SP} = 0.50 was chosen.

Step 2: Estimate the Maximum and Minimum Duty Cycle Under Normal Operating Conditions

Normal input voltage operating conditions are defined as $V_{IN(MIN)}$ and $V_{IN(MAX)}$ on page 1. By using the flyback DC gain function again, the duty cycle is estimated as:

$$D = \frac{1}{1 + n_{SP} \times \left(\frac{V_{IN}}{V_{OUT}}\right)}$$

n_{SP} and V_{OUT} are fixed so clearly D_{MAX} occurs when V_{IN} is a minimum, i.e., at $V_{IN(MIN)}$. For the current design $V_{IN(MIN)}$ = 30V, so:

$$D_{MAX} = 0.44$$

The MAX17690 derives the current, ΔI_{LP}, in the primary magnetizing inductance by measuring the voltage, ΔV_{RCS}, across the current-sense resistor (R_{CS}) during the on-time of the primary-side MOSFET, So:

$$\Delta I_{LP} = \frac{\Delta V_{RCS}}{R_{CS}}$$

ΔI_{LP} is a maximum at D_{MAX} and $V_{IN(MIN)}$ and a minimum at D_{MIN} and $V_{IN(MAX)}$, so:

$$\frac{V_{IN(MIN)}}{L_P} = \frac{\Delta V_{RCS(MIN)} \times f_{SW}}{R_{CS} \times D_{MAX}}$$

and

$$\frac{V_{IN(MAX)}}{L_P} = \left(\frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{\Delta V_{RCS(MIN)}}{R_{CS}}\right) \times \frac{f_{SW}}{D_{MIN}}$$

Solving these two equations:

$$D_{MIN} = D_{MAX} \times \frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \times \frac{\Delta V_{RCS(MIN)}}{\Delta V_{RCS(MAX)}}$$

where $\Delta V_{RCS(MIN)}$ and $\Delta V_{RCS(MAX)}$ correspond to the minimum current-limit threshold (20mV) and the maximum current-limit threshold (100mV) of the MAX17690, respectively. So, for $V_{IN(MIN)}$ = 30V, $V_{IN(MAX)}$ = 60V, and D_{MAX} = 0.44, we have:

$$D_{MIN} \approx 0.063$$

Step 3: Calculate the Maximum Allowable Switching Frequency

The isolated no-opto flyback topology requires the primary-side MOSFET to constantly maintain switching, otherwise there is no way to sense the reflected secondary-side voltage at the drain of the primary-side MOSFET. The MAX17690 achieves this by having a critical minimum on-time, $t_{ON(CRIT)}$, for which it drives the MOSFET. At a given switching frequency, $t_{ON(MIN)}$ corresponds to D_{MIN}. From the MAX17690 data sheet, the critical minimum on-time $t_{ON(CRIT)}$ for the NDRV pin is 235ns. We can therefore calculate the maximum allowable switching frequency to ensure that $t_{ON(CRIT)} > t_{ON(CRIT)}$ as follows:

$$f_{SW(MAX)} = \frac{D_{MIN}}{t_{ON(CRIT)}} \approx 269.7kHz$$

Because D_{MIN} is fixed by $\Delta V_{RCS(MIN)}$, $\Delta V_{RCS(MAX)}$, D_{MAX}, $V_{IN(MIN)}$, and $V_{IN(MAX)}$, then $t_{ON(MIN)}$ can be chosen arbitrarily larger than $t_{ON(CRIT)}$ so that f_{SW} is less than $f_{SW(MAX)}$. With $t_{ON(MIN)}$ = 442ns, the switching frequency is:

$$f_{SW} = \frac{D_{MIN}}{t_{ON(MIN)}} \approx 143.41kHz$$

Note that the MAX17690 should always be operated in the switching frequency range from 50kHz to 250kHz and $t_{ON(MIN)}$ must be chosen accordingly to ensure that this constraint is met.

Step 4: Calculate Primary Magnetizing Inductance

Maximum input power is given by:

$$P_{IN(MAX)} = \frac{P_{OUT(MAX)}}{\eta_{MAX}} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX}}$$

For the DCM flyback converter, all the energy stored in the primary magnetizing inductance, L_P, during the primary-side MOSFET on-time is transferred to the output during the primary-side MOSFET off-time, i.e., the full power transfer occurs during one switching cycle, and since E = P × t:

$$E_{IN(MAX)} = P_{IN(MAX)} \times \tau_{SW} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

The maximum input energy must be stored in L_P during the on-time of the primary-side MOSFET, so:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \Delta I^2_{LP(MAX)}$$

The peak current in L_P, $\Delta I_{LP(MAX)}$, occurs at $V_{IN(MIN)}$ and $t_{ON(MAX)}$, so:

$$\Delta I^2_{LP(MAX)} = \frac{V^2_{IN(MIN)} \times t^2_{ON(MAX)}}{L^2_P}$$

and substituting:

$$E_{IN(MAX)} = \frac{V^2_{IN(MIN)} \times t^2_{ON(MAX)}}{2 \times L_P}$$

combining with the original P × t equation gives:

$$\frac{V^2_{IN(MIN)} \times t^2_{ON(MAX)}}{L^2_P} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

Finally, rearranging gives an expression for the primary magnetizing inductance, L_P:

$$L_P = \frac{\eta_{MAX} \times V^2_{IN(MIN)} \times D^2_{MAX}}{2 \times V_{OUT} \times I_{OUT} \times f_{SW}}$$

Estimating the converter efficiency at 90% and with $V_{IN(MIN)}$ = 30V, D_{MAX} = 0.44, V_{OUT} = 12V, and f_{SW} = 143.41kHz, then:

$$L_{P(MAX)} \approx 67\mu H$$

This inductance represents the maximum primary inductance, since it sets the current-limit threshold. Choosing a larger inductance sets the current-limit threshold at a lower value and could cause the converter to go into current limit at a value lower than I_{OUT}, which would be undesirable. Assuming a ±10% tolerance for the primary magnetizing inductance gives:

$$L_P \approx 42\mu H \pm 10\%$$

Step 5: Recalculate D_{MAX}, D_{MIN}, and $t_{ON(MIN)}$ Based on Selected Value for L_P

Rearranging the L_P equation in Step 4 gives an expression for D_{MAX} as follows:

$$D_{MAX} = \sqrt{\frac{2 \times L_P \times V_{OUT} \times I_{OUT} \times f_{SW}}{\eta_{MAX} \times V^2_{IN(MIN)}}} = 0.327$$

Referring to Step 2:

$$D_{MIN} = D_{MAX} \times \frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \times \frac{\Delta V_{RCS(MIN)}}{\Delta V_{RCS(MAX)}} = 0.049$$

and:

$$t_{ON(MIN)} = \frac{D_{MIN}}{f_{SW}} = 342ns$$

Step 6: Calculate the Peak and RMS Currents in the Primary Winding of the Flyback Transformer

The peak primary winding current occurs at $V_{IN(MIN)}$ and D_{MAX} according to the following equation:

$$\Delta I_{LP(MAX)} = \frac{V_{IN(MIN)} \times D_{MAX}}{L_P \times f_{SW}} \approx 1.63A$$

The RMS primary winding current can be calculated from $\Delta I_{LP(MAX)}$ and D_{MAX} as follows:

$$I_{LP(RMS)} = \Delta I_{LP(MAX)} \times \sqrt{\frac{D_{MAX}}{3}} \approx 0.54A$$

Step 7: Calculate the Peak and RMS Currents in the Secondary Winding of the Flyback Transformer

The peak current in the secondary-side winding of the flyback transformer can be established by considering that the entire energy transferred from the primary-side winding to the secondary-side winding is delivered to the load during one switching period. Again, because E = P × t:

$$E_{OUT} = \frac{1}{2} \times L_S \times \Delta I^2_{LS(MAX)} = P_{OUT} \times \tau_{SW}$$

substituting:

$$P_{OUT} \times \tau_{SW} = \frac{V_{OUT} \times I_{OUT}}{f_{SW}}$$

and rearranging:

$$\Delta I_{LS(MAX)} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{f_{SW} \times L_P \times n^2_{SP}}} = 3.09A$$

Current flows in the secondary-side winding of the flyback transformer during the time the secondary-side rectifying device is conducting. This conduction time, $t_{ON(SEC)}$, is calculated using the inductor volt-second equation:

$$V = L \times \frac{dI}{dt}$$

where V = V_{OUT}, L = L_S, dI = $\Delta I_{LS(MAX)}$, and dt = $t_{ON(SEC)}$, so:

$$t_{ON(SEC)} = L_S \times \frac{\Delta I_{LS(MAX)}}{V_{OUT}} = L_P \times n^2_{SP} \times \frac{\Delta I_{LS(MAX)}}{V_{OUT}}$$

The maximum duty cycle of the secondary-side rectifying device, $D_{S(MAX)}$, can now be calculated:

$$D_{S(MAX)} = \frac{t_{ON(SEC)}}{\tau_{SW}} = t_{ON(SEC)} \times f_{SW} = 0.38$$

Finally, the RMS secondary winding current can be calculated from $\Delta I_{LS(MAX)}$ and $D_{S(MAX)}$ as follows:

$$I_{LS(RMS)} = \Delta I_{LS(MAX)} \times \sqrt{\frac{1 - D_{S(MAX)}}{3}} = 1.41A$$

Step 8: Summarize the Flyback Transformer Specification

All the critical parameters for the flyback transformer have been calculated and are summarized below. Using these parameters, a suitable transformer can be designed.

PARAMETER	SYMBOL	VALUE
Primary Magnetizing Inductance	L_P	42µH ±10%
Primary Peak Current	$\Delta I_{LP(MAX)}$	1.63A
Primary RMS Current	$I_{LP(RMS)}$	0.54A
Turns Ratio (N_S/N_P)	n_{SP}	0.50
Secondary Peak Current	$\Delta I_{LS(MAX)}$	3.09A
Secondary RMS Current	$I_{LS(RMS)}$	1.41A

Step 9: Calculate Design Parameters for Secondary-Side Rectifying Device

Depending on the output voltage and current, a choice can be made for the secondary-side rectifying device. Generally, for output voltages above 12V at low currents (less than 1A) Schottky diodes are used, and for voltages less than 12V synchronous rectification (MOSFET) is used. The current design is a 12V/600mA output converter, but since this is a non-synchronous design, a procedure for selecting a suitable Schottky diode is outlined.

Figure 7 shows a simplified schematic with the Schottky diode DFR.

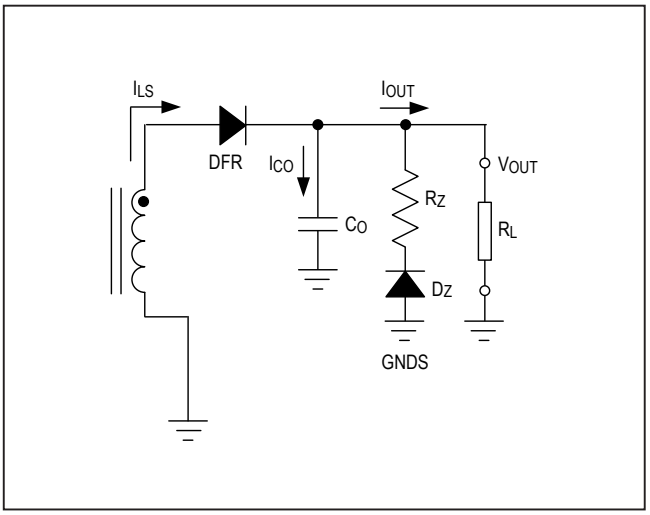

Figure 7. Simplified no-opto flyback schematic with Schottky diode.

The important parameters to consider for the Schottky diode are peak instantaneous current, RMS current, voltage stress, and power losses. Because DFR and L_S are in series, they experience the same peak and RMS currents, so:

$$I_{DFR(RMS)} = I_{LS(RMS)} = 1.41A$$

and:

$$I_{DFR(MAX)} = \Delta I_{LS(MAX)} = 3.09A$$

When DFR is reversed-biased, V_{IN} reflected to the secondary-side of the flyback transformer plus V_{OUT} is applied across the cathode-anode of DFR, so:

$$V_{DFR(REV)} = n_{SP} \times V_{IN(MAX)} + V_{OUT}$$
$$= 0.5 \times 60V + 12V$$
$$\approx 42V$$

DFR has both forward conduction losses and reverse bias losses. Allowing for reasonable design margin, the Diodes Incorporated SBR8U60P5 was chosen for this design with the following specifications:

PARAMETER	VALUE
Forward Voltage Drop	0.35V
Reverse Breakdown Voltage	60V
Maximum Average Forward Current	8A
Maximum Reverse Leakage Current	2000µA

The power losses in the DFR can be approximated as follows:

$$P_{TOT} = P_{FRWD} + P_{REV} \approx 578mW$$

where:

P_{FRWD} is the loss due to $I_{DFR(RMS)}$ flowing through the forward-biased junction of DFR:

$$P_{FRWD} = V_{DFR(FRWD)} \times I_{DFR(RMS)} \approx 493mW$$

P_{REV} is the loss due to the reverse-leakage current flowing through the reversed biased junction of DFR:

$$P_{REV} = V_{DFR(REV)} \times I_{DFR(REV)} \approx 85mW$$

Step 10: Calculate Design Parameters for Primary-Side MOSFET

The important parameters to consider for the primary-side MOSFET (Q_P) are peak instantaneous current, RMS current, voltage stress, and power losses. Because Q_P and L_P are in series they experience the same peak and RMS currents, so from Step 6:

$$I_{QP(MAX)} = \Delta I_{LP(MAX)} \approx 1.63A$$

and:

$$I_{QP(RMS)} = I_{LP(RMS)} \approx 0.54A$$

When Q_P turns off, V_{OUT} reflected to the primary side of the flyback transformer plus $V_{IN(MAX)}$ is applied across the drain-source of Q_P. In addition, until Q_S starts to conduct, there is no path for the leakage inductance energy to flow through. This causes the drain-source voltage of Q_P to rise even further. The factor of 1.5 in the equation below represents this additional voltage rise; however, this factor can be higher or lower depending on the transformer and PCB leakage inductances:

$$V_{QP(MAX)} \approx 1.5 \times \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right) + V_{IN(MAX)} \approx 98V$$

Allowing for reasonable design margin, the Fairchild™ FDMS86252 was chosen for this design with the following specifications:

PARAMETER	VALUE
Maximum Drain-Source Voltage	150V
Continuous Drain Current	16A
Drain-Source Resistance	98mΩ
Minimum V_{GS} Threshold V_{GSTH}	2.0V
Typical V_{GS} Plateau V_{GSPL}	4.0V
Maximum $Q_{G(T)}$	15.0nC
Typical Q_{GD}	2.4nC
Total Output Capacitance C_{OSS}	115pF

The power losses in the Q_P can be approximated as follows:

$$P_{TOT} = P_{CON} + P_{CDS} + P_{SW} \approx 108mW$$

where:

P_{CON} is the loss due to $I_{QP(RMS)}$ flowing through the drain-source on resistance of Q_P:

$$P_{CON} = I^2_{QP(RMS)} \times R_{DS(ON)} \approx 28mW$$

P_{CDS} is the loss due to the energy in the drain-source output capacitance being dissipated in Q_P at turn-on:

$$P_{CDS} = \frac{1}{2} \times f_{SW} \times C_{OSS} \times V^2_{QP(MAX)} \approx 79mW$$

P_{SW} is the turn-on voltage-current transition loss that occurs as the drain-source voltage decreases and the drain current increases during the turn-on transition:

$$P_{SW} = \frac{1}{2} \times f_{SW} \times I_{QP(t-ON)} \times \left\{ \frac{V_{GS(PL)} - V_{GS(TH)}}{V_{GS(PL)}} \times \left(\frac{Q_{G(T)} + Q_{GD}}{I_{DRV}} \right) \right\} \approx 0mW$$

where I_{DRV} is the maximum drive current capability of the MAX17690's NDRV pin and $I_{QP(t-ON)}$ is the instantaneous current in Q_P at turn-on. Because the flyback converter is operating in DCM, $I_{QP(t-ON)}$ is zero and so is P_{SW}.

Step 11: Select the RCD Snubber Components

Referring to Figure 8, when Q_P turns off, I_{LP} charges the output capacitance, C_{OSS}, of QP. When the voltage across C_{OSS} exceeds the input voltage plus the reflected secondary to primary voltage, the secondary-side diode (or synchronous MOSFET) turns on. Because the diode (or synchronous MOSFET) is now on, the energy stored in the primary magnetizing inductance is transferred to the secondary; however, the energy stored in the leakage inductance continues to charge C_{OSS} since there is nowhere else for it to go. Because the voltage across C_{OSS} is the same as the voltage across Q_P, if the energy stored in the leakage inductance charges C_{OSS} to a voltage level greater than the maximum allowable drain-source voltage of Q_P, the MOSFET Q_P can fail.

One way to keep this situation from arising is to add a suitable RCD snubber across the transformer's primary winding. In Figure 8, the RCD snubber is labeled R_{SN}, C_{SN}, and D_{SN}.

In this situation, when Q_P turns off, the voltage at Node A is:

$$V_{NODEA} = V_{CSN} + V_{IN}$$

When the secondary-side diode (or synchronous MOSFET) turns on, the voltage at Node B is:

$$V_{NODEB} = V_{IN} + \frac{V_{OUT} + V_{DFR}}{n_{SP}}$$

So, the voltage across the leakage inductance is:

$$V_{L_{LK}} = V_{CSN} + V_{IN} - \left(V_{IN} + \frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)$$

$$= V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right) = L_{LK} \times \frac{\Delta I_{SN}}{\Delta t_{SN}}$$

So:

$$\Delta t_{SN} = \frac{L_{LK} \times \Delta I_{SN}}{V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)}$$

The average power dissipated in the snubber network is:

$$P_{SN} = V_{CSN} \times \frac{\Delta I_{SN} \times \Delta t_{SN}}{2 \times \tau_{SW}}$$

Substituting Δt_{SN} into this expression gives:

$$P_{SN} = \frac{1}{2} \times L_{LK} \times \Delta I_{SN}^2 \times \frac{V_{CSN}}{V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)} \times f_{SW}$$

The leakage inductance energy is dissipated in R_{SN}, so from:

$$P_{SN} = \frac{V_{CSN}^2}{R_{SN}}$$

We can calculate the required R_{SN} as follows:

$$R_{SN} = \frac{V_{CSN}^2}{\frac{1}{2} \times L_{LK} \times \Delta I_{SN}^2 \times \frac{V_{CSN}}{V_{CSN} - \left(\frac{V_{OUT} + V_{DFR}}{n_{SP}} \right)} \times f_{SW}}$$

Over one switching cycle we must have:

$$I_{SN} = \frac{V_{CSN}}{R_{SN}} = C_{SN} \times \frac{\Delta V_{SN}}{\tau_{SW}}$$

So, we can calculate the required C_{SN} as follows:

$$C_{SN} = \frac{V_{CSN}}{\Delta V_{CSN} \times R_{SN} \times f_{SW}}$$

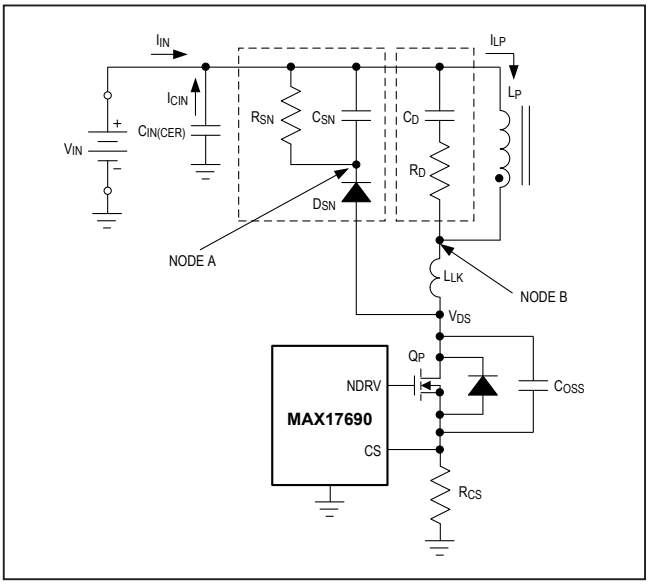

Figure 8. RCD snubber circuit.

Generally, ΔV_{CSN} should be kept to approximately 10% to 30% of V_{CSN}. Figure 9 illustrates V_{CSN}, ΔI_{SN}, and Δt_{SN}. The voltage across the snubber capacitor, V_{CSN}, should be selected so that:

$$V_{CSN} < V_{DS(MAX)(QP)} - V_{IN(MAX)}$$

Choosing too large a value for V_{CSN} causes the voltage on the drain of Q_P to get too close its maximum allowable drain-source voltage, while choosing too small a value results in higher power losses in the snubber resistor. A reasonable value should result in a maximum drain-source voltage for Q_P that is approximately 75% of its maximum allowable value. The worst-case condition for the snubber circuit occurs at maximum output power when:

$$\Delta I_{SN} = \Delta I_{LP(MAX)}$$

Assuming the leakage inductance is 1.5% of the primary inductance, then choosing V_{CSN} = 52V and ΔV_{CSN} = 7.7V, we get the following approximate values:

$$P_{SN} = 241mW$$

$$R_{SN} = 11.5k\Omega$$

$$C_{SN} = 4.7nF$$

Finally, we consider the snubber diode, D_{SN}. This diode should have at least the same voltage rating as the MOSFET, Q_P. Although the average forward current is very low, it must have a peak repetitive current rating greater than $\Delta I_{LP(MAX)}$.

Step 12: Calculate the Required Current-Sense Resistor

From Step 4 we have the maximum input power given by:

$$P_{IN(MAX)} = \frac{P_{OUT(MAX)}}{\eta_{MAX}} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX}}$$

For the DCM flyback converter all the energy stored in the primary magnetizing inductance, L_P, during the MOSFET on-time is transferred to the output during the MOSFET off-time, i.e., the full power transfer occurs during one switching cycle. Therefore, since E = P × t, we have:

$$E_{IN(MAX)} = P_{IN(MAX)} \times \tau_{SW} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

The maximum input energy must be stored in L_P during the on-time of the primary-side MOSFET, so:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}^2$$

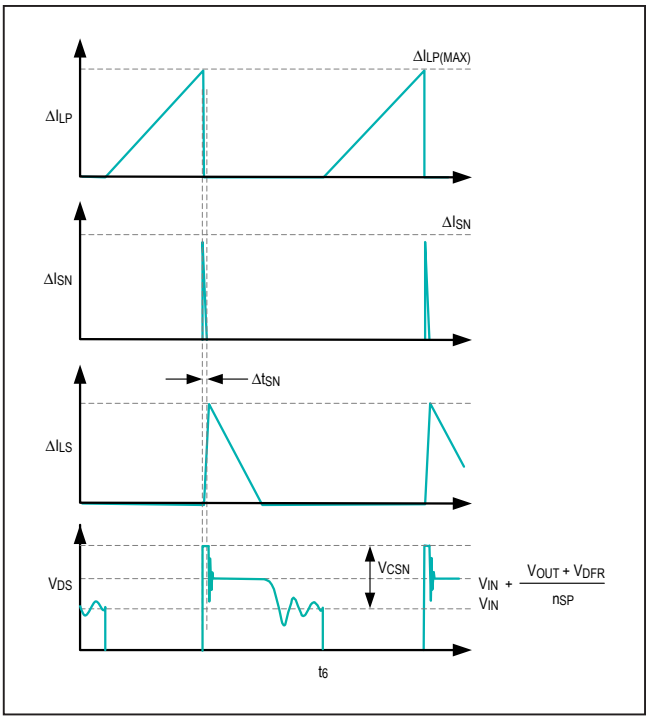

Figure 9. RCD snubber circuit waveforms.

Substituting the equations above:

$$\frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}^2 = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}$$

and:

$$\Delta I_{LP} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta_{MAX} \times L_P \times f_{SW}}}$$

From Step 2 we have:

$$\Delta I_{LP} = \frac{\Delta V_{RCS}}{R_{CS}}$$

so:

$$R_{CS} = \Delta V_{RCS} \times \sqrt{\frac{\eta_{MAX} \times L_P \times f_{SW}}{2 \times V_{OUT} \times I_{OUT}}} = 61m\Omega$$

A standard 60mΩ resistor was chosen for R_{CS}.

Step 13: Calculate and Select the Input Capacitors

Figure 10 shows a simplified schematic of the primary side of the flyback converter and the associated current waveforms. In steady-state operation, the converter draws a pulsed high-frequency current from the input capacitor, C_{IN}. This current leads to a high-frequency ripple voltage across the capacitor according to the following expression:

$$I_{CIN} = C_{IN} \times \frac{\Delta V_{CIN}}{\Delta t}$$

It is the ripple voltage arising from the amp-second product through the input capacitor.

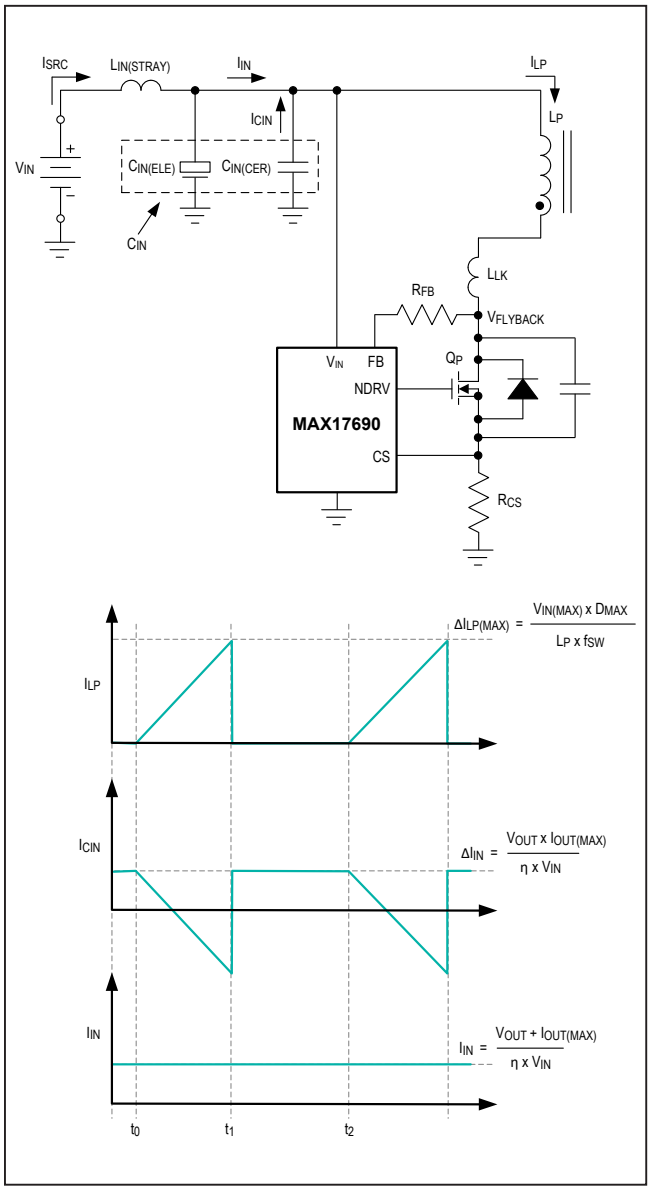

Figure 10. Primary-side circuit and currents.

During the Q_P on-time interval from t_0 to t_1, the capacitor is supplying current to the primary inductance L_P of the flyback transformer and its voltage is decreasing. During the Q_P off-time time interval from t_1 to t_2, no current is flowing in L_P, and current is being supplied to the capacitor from the input voltage source. According to the charge balance law, the decrease in capacitor voltage during time t_0 to t_1 must equal the increase in capacitor voltage during time t_1 to t_2. So:

$$I_{CIN[t_1-t_2]} = C_{IN} \times \frac{\Delta V_{CIN}}{(t_2 - t_1)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

And finally, since:

$$\frac{1}{(t_2 - t_1)} = \frac{f_{SW}}{(1 - D_{MAX})}$$

we have:

$$C_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}} \times \frac{1}{\Delta V_{CIN}} \times \frac{(1 - D_{MAX})}{f_{SW}}$$

For maximum high-frequency ripple voltage requirement ΔV_{CIN}, we can now calculate the required minimum C_{IN}.

There is high-frequency AC current flowing in C_{IN}, as shown in the center waveform of Figure 10. The selected capacitor must be specified to tolerate the maximum RMS current, $I_{CIN(RMS)}$. From the simplified schematic:

$$I_{LP} = I_{IN} + I_{CIN}$$

Therefore:

$$I_{CIN(RMS)} = \sqrt{I^2_{LP(RMS)} - I^2_{IN(RMS)}}$$

where:

$$I_{IN(RMS)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

and from Step 6:

$$I_{LP(RMS)} = \Delta I_{LP(MAX)} \times \sqrt{\frac{D_{MAX}}{3}}$$

So:

$$I_{CIN(RMS)} = \sqrt{\frac{D_{MAX}}{3} \times \Delta I^2_{LP(MAX)} - \frac{V^2_{OUT} \times I^2_{OUT}}{\eta^2_{MAX} \times V^2_{IN(MIN)}}} \approx 0.47A_{RMS}$$

An additional high-frequency ripple voltage is present due to this RMS current flowing through the ESR of the capacitor. Ceramic capacitors are generally used for limiting high-frequency ripple due to their high AC current capability and low ESR.

In addition to using a ceramic capacitor for high-frequency input ripple-voltage control as previously described, an electrolytic capacitor is sometimes inserted at the input of a flyback converter to limit the input voltage deviation when there is a rapid output load change. A 100% load change gives rise to an input current transient of:

$$\Delta I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

During this transient, there is a voltage drop across any series stray inductance, $L_{IN(STRAY)}$, that exists between the input voltage source and the input capacitor of the power supply. So from:

$$\frac{1}{2} \times C_{IN} \times \Delta V_{CIN}^2 = \frac{1}{2} \times L_{IN(STRAY)} \times \Delta I_{IN}^2$$

we have:

$$C_{IN} = L_{IN(STRAY)} \times \frac{\Delta I_{IN(MAX)}^2}{\Delta V_{CIN}^2}$$

We now have two values for C_{IN}. One for input high-frequency ripple-voltage control:

$$C_{IN(CER)} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}} \times \frac{1}{\Delta V_{CIN}} \times \frac{(1 - D_{MAX})}{f_{SW}}$$

and a second for transient input voltage control:

$$C_{IN(ELE)} = L_{IN(STRAY)} \times \frac{\Delta I_{IN(MAX)}^2}{\Delta V_{CIN}^2}$$

If $C_{IN(ELE)} > C_{IN(CER)}$, both ceramic and electrolytic capacitors must be used at the input of the power supply and ΔV_{CIN} should be limited to approximately 75mV to keep the AC current in the ESR of the electrolytic capacitor within acceptable limits. Otherwise, $C_{IN(ELE)}$ is not required. In this case, the value of $C_{IN(CER)}$ can be significantly reduced because there is no longer any requirement to limit ΔV_{CIN} to less than 75mV. Based on the current design specification with $L_{IN(STRAY)}$ approximated at 50nH:

$$C_{IN(CER)} \approx 16.7\mu F$$

and:

$$C_{IN(ELE)} \approx 0.7\mu F$$

Since $C_{IN(ELE)} < C_{IN(CER)}$, an electrolytic capacitor is not required. We can now recalculate $C_{IN(CER)}$ based on a ΔV_{CIN} = 600mV:

$$C_{IN(CER)} \approx 2.1\mu F$$

Allowing for a capacitor tolerance of ±10% and a further reduction of capacitance of 75% due to the DC bias effect (operating an 80V ceramic capacitor at 50V), the final nominal value of input capacitance required is:

$$C_{IN(CER)} = \frac{2\mu F}{90\% \times 25\%} \approx 9.3\mu F$$

This is achieved using two 4.7µF ceramic capacitors (Murata® GRM32ER71K475KE14) in parallel. The AC current in each capacitor is:

$$\frac{I_{CIN(RMS)}}{2} \approx 0.23A_{RMS}$$

which is well within specification for the selected capacitor.

Step 14: Calculate and Select the Output Capacitor

High-frequency ripple voltage requirements are also used to determine the value of the output capacitor in a flyback converter.

Figure 11 shows a simplified schematic of the secondary side of the flyback converter and the associated current waveforms.

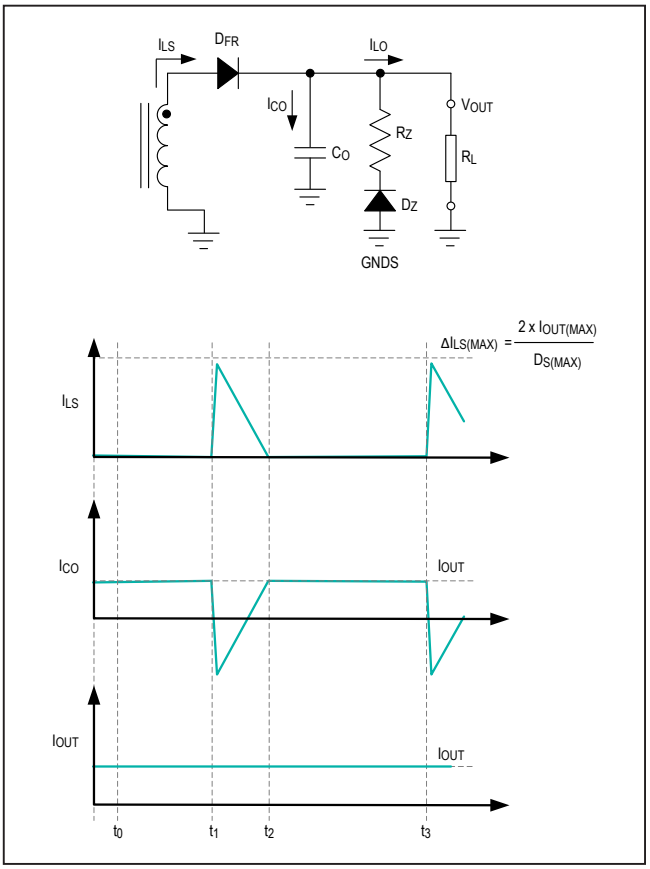

Figure 11. Secondary-side circuit and currents.

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In steady-state operation, the load draws a DC current from the secondary side of the flyback converter. By examining the secondary current waveforms, we see that C_O is supplying the full output current I_{OUT} to the load during the time interval from t_2 to t_3. During this time interval, the voltage across C_O decreases. At time t_3, Q_P has just turned off and the secondary rectifying diode DFR (or the secondary synchronous MOSFET Q_S) starts to conduct supplying current to the load and to C_O. The charging and discharging of C_O leads to a high-frequency ripple voltage at the output according to the following expression:

$$I_{CO} = C_O \times \frac{\Delta V_{CO}}{\Delta t}$$

Again, as with the input capacitor, this is the ripple voltage arising from the amp-second product through the output capacitor.

By the capacitor charge balance law, the decrease in capacitor voltage during time t_2 to t_3 must equal the increase in capacitor voltage during time t_1 to t_2. When the capacitor is discharging, we have:

$$I_{CO[t_2-t_3]} = C_O \times \frac{\Delta V_{CO}}{(t_3 - t_2)} = I_{OUT}$$

Finally, since:

$$\frac{1}{(t_3 - t_2)} = \frac{f_{SW}}{\left(1 - D_{S(MAX)}\right)}$$

We have:

$$C_O = I_{OUT} \times \frac{1}{\Delta V_{CO}} \times \frac{\left(1 - D_{S(MAX)}\right)}{f_{SW}}$$

For maximum high-frequency ripple voltage requirement ΔV_{CO}, we can now calculate the required minimum C_O.

$$C_O \approx 21.2\mu F$$

As with the input capacitor, an additional high-frequency ripple voltage occurs at the output due to the output capacitor's ESR and can be minimized by choosing a capacitor with low ESR. Also, as with the input capacitor, there is high-frequency AC current flowing in C_O as shown in the center waveform of Figure 11. The selected capacitor must be specified to tolerate this maximum RMS current, $I_{CO(RMS)}$. From the simplified schematic:

$$I_{LS} = I_{OUT} + I_{CO}$$

Therefore:

$$I_{CO(RMS)} = \sqrt{I^2_{LS(RMS)} - I^2_{OUT(RMS)}}$$

where:

$$I_{OUT(RMS)} = I_{OUT}$$

and from Step 7:

$$I_{LS(RMS)} = \Delta I_{LS(MAX)} \times \sqrt{\frac{1 - D_{S(MAX)}}{3}}$$

POWER COMPONENT	QTY	DESCRIPTION
Flyback Transformer	1	PRI. INDUCTANCE = 42µH SEC-PRI TURNS RATIO = 0.50 PEAK. PRI CURRENT = 1.63A PRI. RMS CURRENT = 0.54A PEAK SEC. CURRENT = 3.09A SEC. RMS CURRENT = 1.41A SWITCHING FREQ. = 143.41kHz
Input Capacitors	2	CAPACITOR; SMT (1210); CERAMIC CHIP 4.7µF; 80V; 10%; X7R Murata GRM32ER71K475KE14
Output Capacitors	3	CAPACITOR; SMT (1210); CERAMIC CHIP 22µF; 25V; 20%; X7R Murata GRM32ER71E226M
Primary MOSFET	1	MOSFET; NCH; I-(16A); V-(150V) Fairchild FDMS86252
Schottky Diode	1	DIODE; RECT; PIV=60V; IF=8A Diodes Inc. SBR8U60P5

so:

$$I_{CO(RMS)} = \sqrt{\frac{1 - D_{S(MAX)}}{3} \times \Delta I^2_{LS(MAX)} - I^2_{OUT}} \approx 1.28A_{RMS}$$

If we allow for a capacitor tolerance of ±20% and a further reduction of capacitance of 57% due to the DC bias effect (operating a 25V ceramic capacitor at 12V), our final nominal value is:

$$C_O = \frac{21.2\mu F}{80\% \times 40\%} \approx 66.25\mu F$$

We can achieve this by placing three 22µF ceramic capacitors (Murata GRM32ER71E226M) in parallel. The minimum output capacitance using the above combination is 21.6µF. The AC current in each capacitor is therefore:

$$\frac{I_{CO(RMS)}}{3} \approx 0.426A_{RMS}$$

which is well within specification for the selected capacitor.

Step 15: Summarize the Power Component Design

A first pass at calculating the power components in the no-opto flyback converter using MAX17690 has been completed. Referring to the schematic, a summary of the power components is listed below:

Part II: Setting Up the MAX17690 No-Opto Flyback Controller

Step 16: Setting Up the Switching Frequency

The MAX17690 can operate at switching frequencies between 50kHz and 250kHz (subject to the considerations in Step 3). A lower switching frequency optimizes the design for efficiency, whereas increasing the switching frequency allows for smaller inductive and capacitive components sizes and costs. A switching frequency of 143.5kHz was chosen in Step 3. R9 sets the switching frequency according to the following expression:

$$R9 = \frac{5 \times 10^6}{f_{SW}} \approx 34.8k\Omega$$

where R9 is in kΩ and f_{SW} is in Hz.

Step 17: Setting Up the Soft-Start Time

The capacitor C6 connected between the SS pin and SGND programs the soft-start time. A precision internal 5µA current source charges the soft-start capacitor C6. During the soft-start time, the voltage at the SS pin is used as a reference for the internal error amplifier during startup. The soft-start feature reduces inrush current during startup. Since the reference voltage for the internal error amplifier is ramping up linearly, so too is the output voltage during soft-start. The soft-start capacitor is chosen based on the required soft-start time (20ms) as follows:

$$C6 = 5 \times t_{SS} \approx 100nF$$

where C6 is in nF and t_{SS} is in ms. A standard 100nF capacitor was chosen.

Step 18: Setting Up the UVLO and OVI Resistors

A resistor-divider network of R1, R3, and R2 from V_{IN} to SGND sets the input undervoltage lockout threshold and the output overvoltage inhibit threshold. The MAX17690 does not commence its startup operation until the voltage on the EN/UVLO pin (R3/R2 node) exceeds 1.215V (typical). When the voltage on the OVI pin (R1/R3 node) exceeds 1.215V (typical), the MAX17690 stops switching, thus inhibiting the output. Both pins have hysteresis built in to avoid unstable turn-on/turn-off at the UVLO/EN and OVI thresholds. After the device is enabled, if the voltage on the UVLO/EN pin drops below 1.1V (typical), the controller turns off; after the device is OVI inhibited, it turns back on when the voltage at the OVI pin drops below 1.1V (typical). Whenever the controller turns on, it goes through the soft-start sequence. For the current design R1 = 10kΩ, R2 = 487kΩ, and R3 = 11kΩ give rise to an UVLO/EN threshold of 29V and an OVI threshold of 61V.

Step 19: Placing Decoupling Capacitors on V_{IN} and INTVCC

As previously discussed, the MAX17690 no-opto flyback controller compares the voltage $V_{FLYBACK}$ to V_{IN}. This voltage difference is converted to a proportional current that flows in R5. The voltage across R5 is sampled and compared to an internal reference by the error amplifier. The output of the error amplifier is used to regulate the output voltage. The V_{IN} pin should be directly connected to the input voltage supply. For robust and accurate operation, a ceramic capacitor (C2 = 1µF) should be placed between V_{IN} and SGND as close as possible to the IC.

V_{IN} powers the MAX17690's internal low dropout regulator. The LDO's regulated output is connected to the INTVCC pin. A ceramic capacitor (C3 = 2.2µF min) should be connected between the INTVCC and PGND pins for stable operation over the full temperature range. Place this capacitor as close as possible to the IC.

Step 20: Setting Up the Feedback Components

R_{SET} (R5), R_{FB} (R4, R110), R_{RIN} (R8), R_{VCM} (R6), and R_{TC} (R105) are all critically important to achieving optimum output voltage regulation across all specified line, load and temperature ranges.

R_{SET} resistor (R5): This resistor value is optimized based on the IC's internal voltage to current amplifier and should not be changed.

$$R5 = R_{SET} = 10k\Omega$$

R_{FB} resistor (R4, R110): The feedback resistor is calculated according to the previous equation, restated below:

$$R_{FB} = \frac{R_{SET}}{n_{SP} \times V_{SET}} \times \left(V_{OUT} + V_{DFR} + V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}} \right)$$

$$\approx 258.8k\Omega$$

From the MAX17690 data sheet, V_{SET} = 1V. The two resistors R4 = 182kΩ and R110 = 76.8kΩ form R_{FB}. Using one high value resistor and one low value resistor in series allows slight adjustment to the series resistance combination so that the output voltage can be fine-tuned to its required value, if necessary.

R_{RIN} resistor (R8): The internal temperature compensation circuitry requires a current proportional to V_{IN} to operate correctly. R_{RIN} establishes this current. R_{RIN} is calculated according to the following equation:

$$R_{RIN} \approx 0.6 \times R_{FB}$$

R_{VCM} resistor (R6): The MAX17690 generates an internal voltage proportional to the on-time volt-second product. This enables the device to determine the correct sampling instant for $V_{FLYBACK}$ during the Q_P off-time. Resistor R6 is used to scale this internal voltage to an acceptable internal voltage limit in the device. To calculate the resistor, we must first calculate a scaling constant as follows:

$$K_C = \frac{(1 - D_{MAX}) \times 10^8}{3 \times f_{SW}} = 158$$

After K_C is calculated, the R6 value can be selected from the following table by choosing the resistance value that corresponds to the next largest K_C:

K_C	R6
640	0Ω
320	75kΩ
160	121kΩ
80	220Ω
40	Open

In the present case, R6 = 121kΩ.

R_{TC} resistor (R105): The value of R_{TC} can then be calculated using the previous expression, restated by the following:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T} \approx 121k\Omega$$

This completes the setup of the MAX17690 no-opto flyback controller.

Part III: Closing the Control Loop

Step 21: Determine the Required Bandwidth

The bandwidth of the control loop determines how quickly the converter can respond to changes at its input and output. If we have a step change in output current, the voltage across the output capacitor decreases as shown in Figure 12.

The control loop detects this reduction in output voltage and increases the duty cycle of Q_P to supply more current to the output capacitor. The amount of time required by the control loop to increase the duty cycle from its minimum value to its maximum value is the response time, τ_{RES}, of the control loop. For the MAX17690 we have:

$$\tau_{RES} \approx \left\{ \frac{1}{3 \times f_C} + \frac{1}{f_{SW}} \right\}$$

where f_C is the bandwidth of the power converter. If we apply a switching load step of amplitude ΔI_{STEP} at a frequency of $(1/\tau_{RES})$ and a 50% duty cycle, then to limit the output voltage deviation to $\pm\Delta V_{OUT(STEP)}$ we must have a minimum output capacitance of:

$$C_{O(MIN)} = \frac{\Delta I_{OUT(STEP)} \times \left(\frac{\tau_{RES}}{2} \right)}{\Delta V_{OUT(STEP)}}$$

Combining the two previous equations, we have:

$$f_C = \frac{\frac{1}{3} \times f_{SW} \times \Delta I_{OUT(STEP)}}{2 \times f_{SW} \times C_{O(MIN)} \times \Delta V_{OUT(STEP)} - \Delta I_{OUT(STEP)}}$$

It is normal to specify $\Delta V_{OUT(STEP)}$ for a load step from 50% to 100% of the maximum output current. We have already calculated $C_{O(MIN)}$ = 21.2µF in Step 14, f_{SW} = 143.41kHz, so based on a 3% maximum $\Delta V_{OUT(STEP)}$:

$$f_C \approx 7.4kHz$$

Step 22: Calculate the Loop Compensation

The MAX17690 uses peak current-mode control and an internal transconductance error amplifier to compensate the control loop. The control loop is modeled, as shown in Figure 13, by a power modulator transfer function $G_{MOD(s)}$, an output-voltage feedback transfer function $G_{FB(s)}$, and an error amplifier transfer function $G_{EA(s)}$.

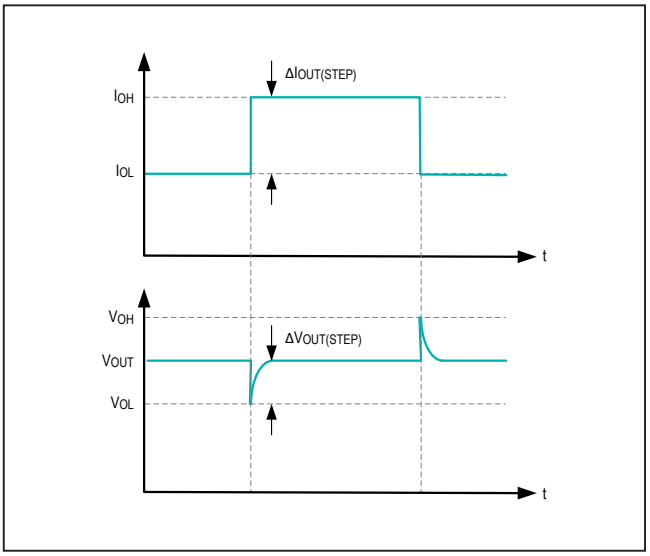

Figure 12. Output load step response.

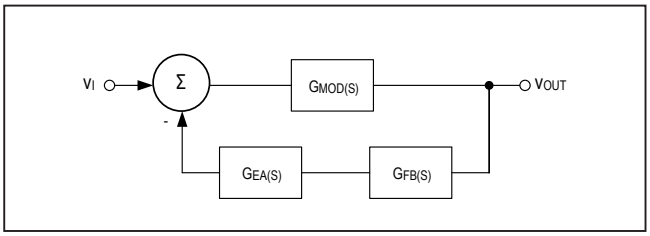

Figure 13. Simplified model of control loop.

The power modulator has a pole located at $f_{P(MOD)}$ determined by the impedance of the output capacitor C_O and the load impedance R_L. It also has a zero at $f_{Z(MOD)}$ determined by the impedance of C_O and the ESR of C_O. The DC gain of the power modulator is determined by the peak primary current ΔI_{LP} and the current-sense resistor R_{CS}. So:

$$G_{MOD(DC)} = \frac{1}{\Delta I_{LP} \times R_{CS}}$$

$$f_{P(MOD)} = \frac{1}{2\pi \times C_O \times R_L} = \frac{I_{OUT}}{2\pi \times C_O \times V_{OUT}}$$

and:

$$f_{Z(MOD)} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

The output voltage feedback transfer function $G_{FB(s)}$ is independent of frequency and has a DC gain determined by V_{IN}, $V_{FLYBACK}$, and V_{SET} as follows:

$$G_{FB(DC)} = \frac{V_{SET}}{V_{FLYBACK} - V_{IN}} = \frac{V_{SET} \times n_{SP}}{V_{OUT} + V_{DFR}}$$

The MAX17690's transconductance error amplifier should be set up in a configuration to compensate for the pole at $f_{P(MOD)}$ and the zero at $f_{Z(MOD)}$ of the modulator. This can be achieved by Type II transconductance error amplifier compensation shown in Figure 14.

This type of compensation scheme has a low frequency pole at $f_{P-LF(EA)}$ due to the very large output resistance R_O (30MΩ - 50MΩ) of the operational transconductance amplifier (OTA). It has a zero at $f_{Z(EA)}$ determined by C_Z and R_Z of the compensation network, and it has an additional pole at $f_{P(EA)}$ determined by C_P and R_Z of the compensation network. So:

$$f_{P-LF(EA)} = \frac{1}{2\pi \times C_Z \times (R_O + R_Z)}$$

and:

$$f_{Z(EA)} = \frac{1}{2\pi \times C_Z \times R_Z}$$

$$f_{P(EA)} = \frac{1}{2\pi \times C_P \times R_Z}$$

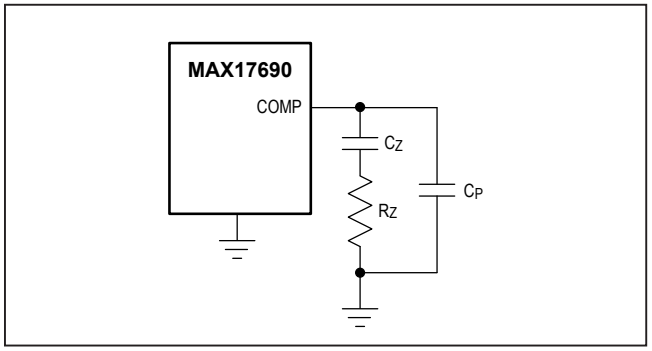

Figure 14. Type II compensation for OTA.

To achieve stable operation, we must ensure that:

$$f_{P(MOD)} \ll f_C < \frac{f_{SW}}{20}$$

Set the closed loop gain at f_C equal to 1:

$$G_{MOD(f_C)} \times G_{FB(f_C)} \times G_{EA(f_C)} = 1$$

Place the zero in the error amplifier network at the same frequency as the pole in the power modulator transfer function:

$$f_{Z(EA)} = f_{P(MOD)}$$

$$\frac{1}{2\pi \times C_Z \times R_Z} = \frac{I_{OUT(MAX)}}{2\pi \times C_O \times V_{OUT}}$$

The frequency $f_{Z(MOD)}$ at which the zero occurs in the power modulator transfer function depends on the ESR of C_O. If ceramic capacitors are used for C_O, $f_{Z(MOD)}$ will generally be much higher than f_C. However, if the ESR of C_O is large, $f_{Z(MOD)}$ could be lower than f_C. This is a very important point since both the gain of the power modulator at f_C, and the gain of the error amplifier at f_C depend on whether $f_{Z(MOD)}$ is greater than or less than f_C. This is illustrated in Figure 15.

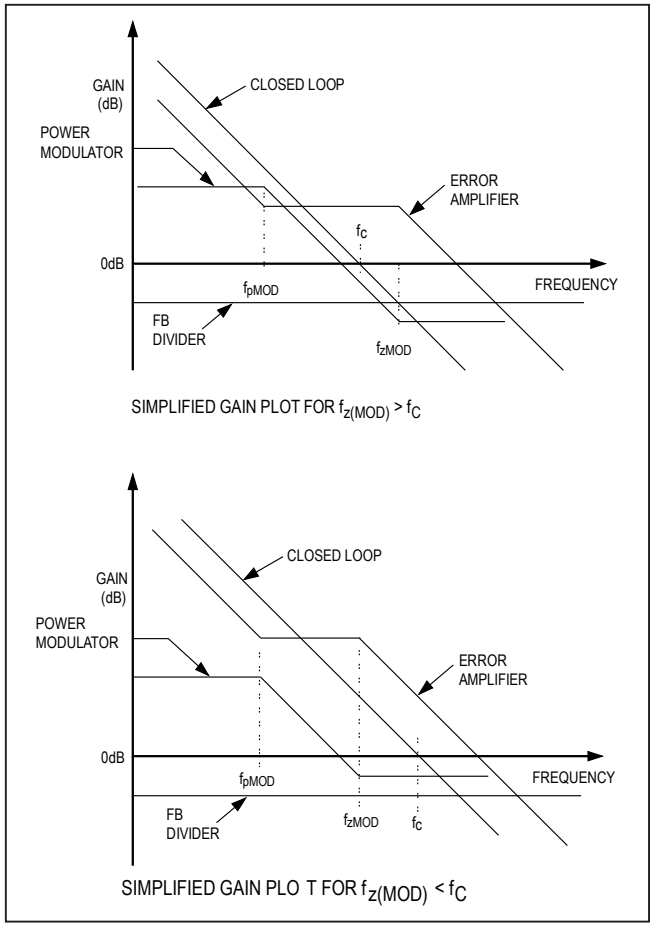

Figure 15. Simplified gain plot.

By examining the gain plots in Figure 15, we see that for $f_{Z(MOD)} > f_C$:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \left(\frac{f_{P(MOD)}}{f_C} \right)$$

$$G_{EA(f_C)} = g_{m(EA)} \times R_Z$$

and for $f_{Z(MOD)} < f_C$:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \left(\frac{f_{P(MOD)}}{f_{Z(MOD)}} \right)$$

$$G_{EA(f_C)} = g_{m(EA)} \times \left(\frac{f_{Z(MOD)}}{f_C} \right) \times R_Z$$

For the current design, we have:

$$f_{P(MOD)} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_O} \approx 368Hz$$

and:

$$f_{Z(MOD)} = \frac{1}{2\pi \times ESR_{CO} \times C_O} \approx 7.352MHz$$

Since $f_{Z(MOD)} > f_C$:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \left(\frac{f_{P(MOD)}}{f_C} \right) = \frac{1}{\Delta I_{LP} \times R_{CS}} \times \left(\frac{f_{P(MOD)}}{f_C} \right)$$

$$G_{EA(f_C)} = g_{m(EA)} \times R_Z$$

and since G_{FB} is independent of frequency, we have:

$$G_{FB(f_C)} = G_{FB(DC)} = \frac{V_{SET} \times n_{SP}}{V_{OUT} + V_{DFR}}$$

We can now set the closed-loop gain equal to 1 as follows:

$$G_{MOD(f_C)} \times G_{FB(DC)} \times G_{EA(f_C)} = 1$$

$$\frac{1}{\Delta I_{LP} \times R_{CS}} \times \left(\frac{f_{P(MOD)}}{f_C} \right) \times \frac{V_{SET} \times n_{SP}}{V_{OUT} + V_{DFR}} \times g_{m(EA)} \times R_Z = 1$$

Rearranging we can calculate:

$$R_Z = \frac{1}{g_{m(EA)}} \times \frac{(V_{OUT} + V_{DFR})}{V_{SET} \times n_{SP}} \times \left(\frac{f_C}{f_{P(MOD)}} \right) \times R_{CS} \times \Delta I_{LP}$$

Substituting ΔI_{LP} from Step 12:

$$R_Z = \frac{1}{g_{m(EA)}} \times \frac{(V_{OUT} + V_{DFR})}{V_{SET} \times n_{SP}} \times \left(\frac{f_C}{f_{P(MOD)}} \right) \times R_{CS} \times \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{\eta_{MAX} \times L_P \times f_{SW}}} = 20k\Omega$$

Finally, we can calculate the remaining components, C_Z and C_P, in the error amplifier compensation network as follows:

$$C_Z = \frac{1}{2\pi \times f_{P(MOD)} \times R_Z} = 22nF$$

and:

$$C_P = \frac{1}{2\pi \times f_{Z(MOD)} \times R_Z} = 5pF$$

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/18	Initial release	—