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AN-6104

LLC Resonant Converter Design using FAN7688

Introduction

Among many resonant converters, LLC resonant converter has been the most popular topology for high power density applications since this topology has many advantages over other resonant topologies; it can regulate the output over entire load variation with a relatively small variation of switching frequency, it can achieve Zero Voltage Switching (ZVS) for the primary side switches and zero current switching (ZCS) for the secondary side rectifiers and the resonant inductor can be integrated into a transformer. FAN7688 is an advanced Pulse Frequency Modulated (PFM) controller for LLC resonant converters with Synchronous Rectification (SR) that offers best in class efficiency for isolated DC/DC converters. Compared to the conventional PFM controllers in the market, FAN7688 offers several unique features that can maximize the efficiency, reliability and performance.

1. Charge Current Control: Voltage mode control has been typically used for LLC resonant converter where the error amplifier output voltage directly controls the switching frequency. However, the compensation network design of LLC resonant converter is relatively challenging since the frequency response of the LLC resonant converter with voltage mode control has very complicated characteristics with four poles where the location of the poles changes with input voltage and load condition. FAN7688 employs a current mode control technique based on a charge control, which provides a better control-to-output transfer function of the power stage simplifying the feedback loop design while allowing true input power limit capability and inherent line feed-forward.

2. Dual Edge Tracking SR Control: FAN7688 uses a dual edge tracking adaptive gate drive method that anticipates the SR current zero crossing instant with respect to two different time references. This technique not only minimizes the dead time during the normal operation but also provides stable SR control during any transient and mode change.

This application note presents design considerations of LLC resonant half-bridge converter employing FAN7688. It includes explanation of LLC resonant converter operation principle, designing the transformer and resonant network, and selecting the components. The step-by-step design procedure explained with a design example helps design the LLC resonant converter.

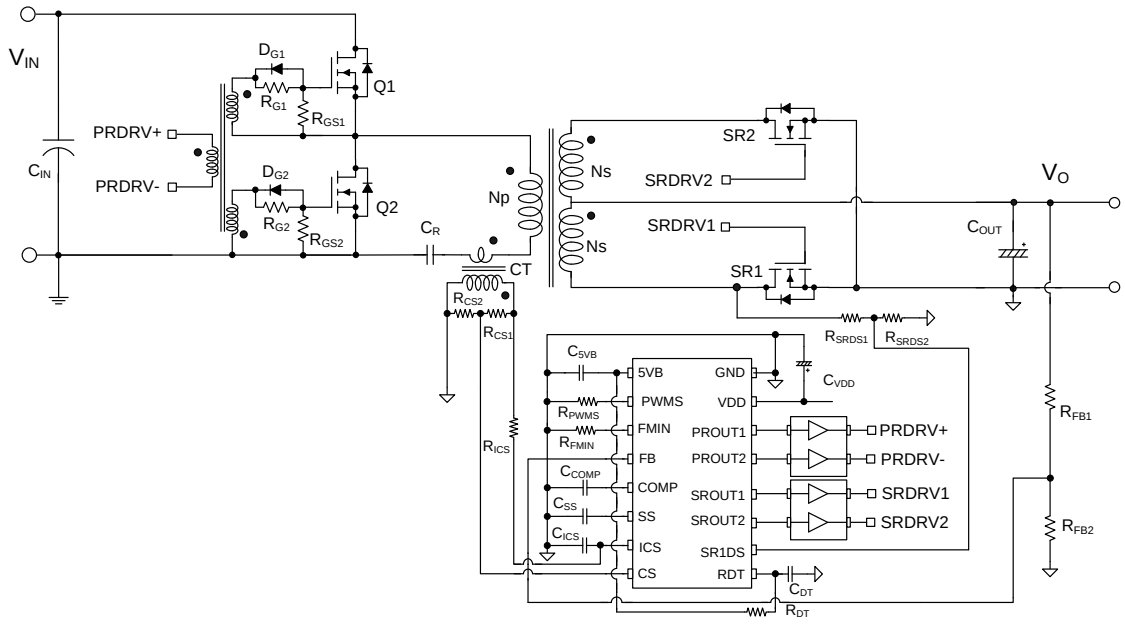


Figure 1. Schematic of Half-bridge LLC Resonant Converter

LLC Resonant Converter and Fundamental Approximation

Figure 2 shows the simplified schematic of a half-bridge LLC resonant converter, where Lm is the magnetizing inductance that acts as a shunt inductor, Lr is the series resonant inductor, and Cr is the resonant capacitor. Figure 3 illustrates the typical waveforms of the LLC resonant converter. It is assumed that the operation frequency is same as the resonance frequency, determined by the resonance between Lr and Cr. Since the magnetizing inductor is relatively small, there exists considerable amount of magnetizing current (Im), which freewheels in the primary side without being involved in the power transfer. The primary-side current (Ip) is sum of the magnetizing current and the secondary-side current referred to the primary.

In general, the LLC resonant topology consists of three stages shown in Figure 2; square wave generator, resonant network, and rectifier network.

1. The square wave generator produces a square wave voltage, V_d, by driving switches Q_1 and Q_2 alternately with 50% duty cycle for each switch. A small dead time is usually introduced between the consecutive transitions. The square wave generator stage can be built as a full-bridge or half-bridge type.
2. The resonant network consists of a capacitor, leakage inductances, and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Essentially, only sinusoidal current is allowed to flow through the resonant network even though a square wave voltage is applied to the resonant network. The current (I_p) lags the voltage applied to the resonant network (that is, the fundamental component of the square wave voltage (V_d) applied to the half-bridge totem pole), which allows the MOSFETs to be turned on with zero voltage. As shown in Figure 3, the MOSFET turns on while the voltage across the MOSFET is zero by flowing current through the anti-parallel diode.
3. The rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and capacitor. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration with capacitive output filter.

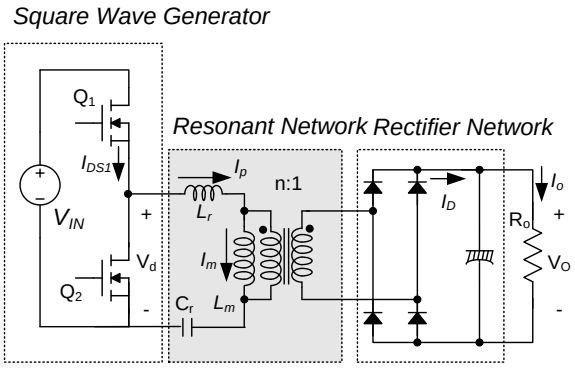


Figure 2. Schematic of Half-bridge LLC Resonant Converter

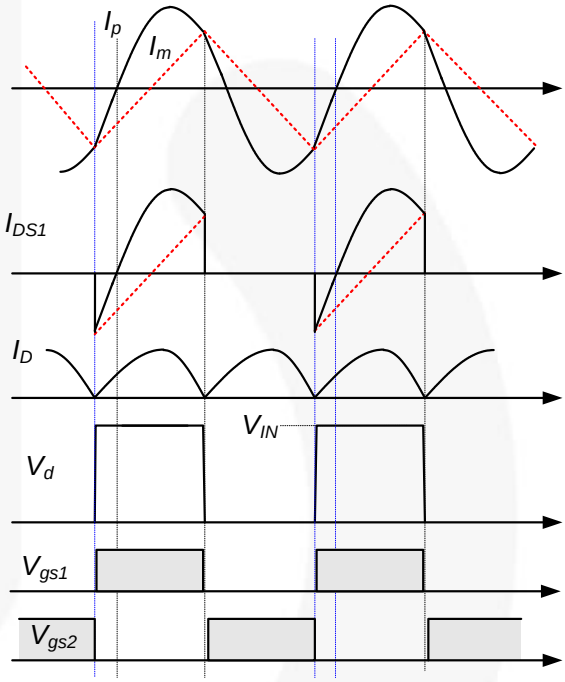


Figure 3. Typical Waveforms of Half-bridge LLC Resonant Converter

The filtering action of the resonant network allows use of the fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Figure 4 shows how this equivalent load resistance is derived. The primary-side circuit is replaced by a sinusoidal current source, I_{ac}, and a square wave voltage, V_{RI}, appears at the input to the rectifier. Since the average of $|I_{ac}|$ is the output current, I_o, I_{ac}, is obtained as:

$$I_{ac} = \frac{\pi \cdot I_o}{2} \sin(\omega t) \quad (1)$$

and V_{RI} is given as:

$$V_{RI} = +V_o \quad if\ \sin(\omega t) > 0$$
$$V_{RI} = -V_o \quad if\ \sin(\omega t) < 0 \tag{2}$$

where V_o is the output voltage.

The fundamental component of V_{RI} is given as:

$$V_{RI}^{\ F} = \frac{4V_o}{\pi}\sin(\omega t) \tag{3}$$

Since harmonic components of V_{RI} are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing $V_{RI}^{\ F}$ by I_{ac} as:

$$V_{RI}^{\ F} = \frac{4V_o}{\pi}\sin(\omega t) \tag{4}$$

Considering the transformer turns ratio ($n=N_p/N_s$), the equivalent load resistance shown in the primary side is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2}R_o \tag{5}$$

By using the equivalent load resistance, the AC equivalent circuit is obtained, as illustrated in Figure 5, where $V_d^{\ F}$ and $V_{RO}^{\ F}$ are the fundamental components of the driving voltage, V_d and reflected output voltage, V_{RO} (nV_{RI}), respectively.

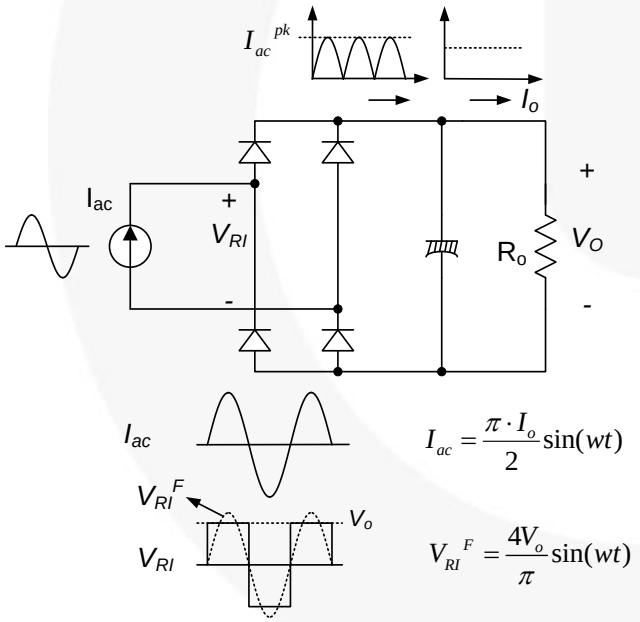


Figure 4. Derivation of Equivalent Load Resistance R_{ac}

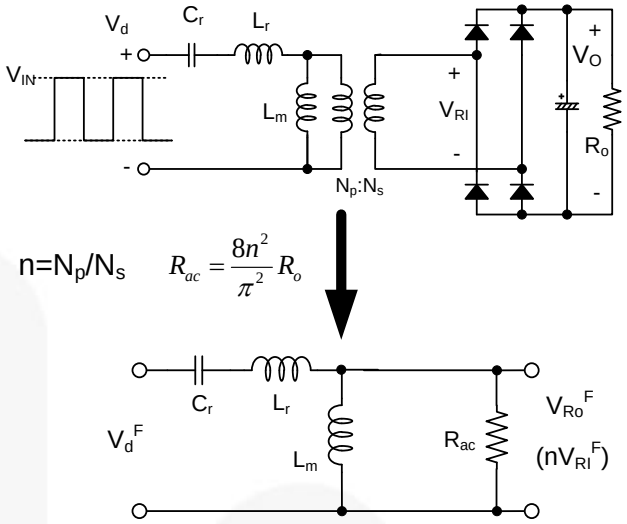


Figure 5. AC Equivalent Circuit for LLC Resonant Converter

With the equivalent load resistance obtained in Equation 5, the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Figure 5, the voltage gain, M, is obtained as:

$$M = \frac{V_{RO}^{\ F}}{V_d^{\ F}} = \frac{n \cdot V_{RI}^{\ F}}{V_d^{\ F}} = \frac{\frac{4n \cdot V_o}{\pi}\sin(\omega t)}{\frac{4}{\pi}\frac{V_{in}}{2}\sin(\omega t)} = \frac{2n \cdot V_o}{V_{in}}$$
$$= \left| \frac{(\frac{\omega}{\omega_o})^2 (m-1)}{(\frac{\omega^2}{\omega_p^{\ 2}} - 1) + j\frac{\omega}{\omega_o}(\frac{\omega^2}{\omega_o^{\ 2}} - 1)(m-1)Q} \right| \tag{6}$$

where:

$$L_p = L_m + L_r\ ,\ R_{ac} = \frac{8n^2}{\pi^2}R_o\ ,\ m = \frac{L_p}{L_r}$$
$$Q = \sqrt{\frac{L_r}{C_r}}\frac{1}{R_{ac}}\ ,\ \omega_o = \frac{1}{\sqrt{L_r C_r}}\ ,\ \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

As can be seen in Equation (6), there are two resonant frequencies. One is determined by L_r and C_r, while the other is determined by L_p and C_r.

Equation (6) shows the gain is unity at resonant frequency (ω_o), regardless of the load variation, which is given as:

$$M = \frac{2n \cdot V_o}{V_{in}} = \frac{(m-1)\cdot \omega_p^{\ 2}}{\omega_o^{\ 2} - \omega_p^{\ 2}} = 1 \quad at\ \omega = \omega_o \tag{7}$$

The gain of Equation (6) is plotted in Figure 6 for different Q values with m=3, f_o=100kHz, and f_p=57kHz. As observed in Figure 6, the LLC resonant converter shows gain characteristics that are almost independent of the load when the switching frequency is around the resonant frequency, f_o. This is a distinct advantage of LLC-type resonant converter over the conventional series resonant converter. Therefore,

it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation.

The operating range of the LLC resonant converter is limited by the peak gain (attainable maximum gain), which is indicated with '*' in Figure 6. It should be noted that the peak voltage gain does not occur at f_o or f_p. The peak gain frequency where the peak gain is obtained exists between f_p and f_o, as shown in Figure 6. As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to f_o and the peak gain drops; thus, the full load condition should be the worst case for the resonant network design.

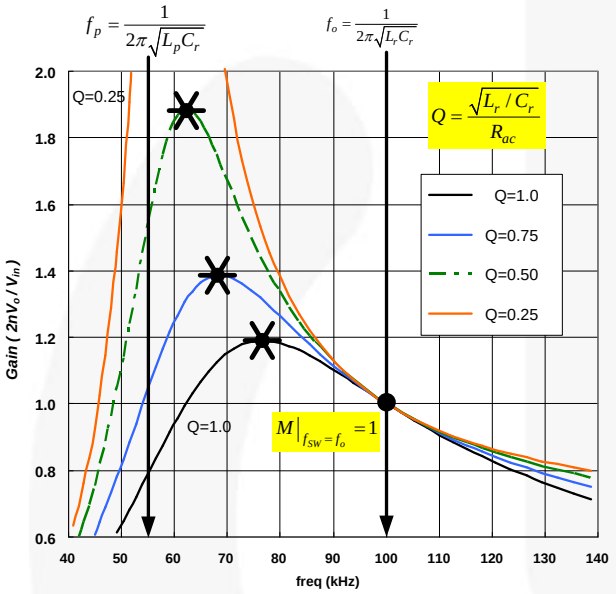


Figure 6. Typical Gain Curves of LLC Resonant Converter (*m*=3)

Consideration for Integrated Transformer

For practical design, it is common to implement the magnetic components (series inductor and shunt inductor) using an integrated transformer; where the leakage inductance is used as a series inductor, while the magnetizing inductor is used as a shunt inductor. When building the magnetizing components in this way, the equivalent circuit in Figure 5 should be modified as shown in Figure 7 because the leakage inductance exists, not only in the primary side, but also in the secondary side. Not considering the leakage inductance in the transformer secondary side generally results in an incorrect design.

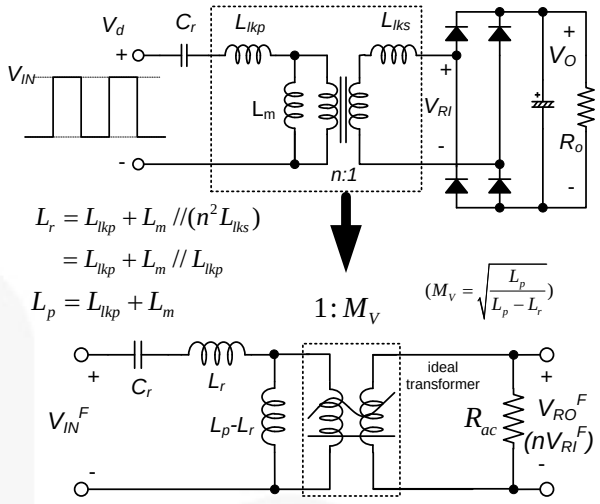


Figure 7. Modified Equivalent Circuit to Accommodate the Secondary-Side Leakage Inductance

In Figure 8, the effective series inductor (L_p) and shunt inductor (L_p-L_r) are obtained by assuming $n^2L_{lks}=L_{lkp}$ and referring the secondary side leakage inductance to the primary side as:

$$L_p = L_m + L_{lkp}$$
$$L_r = L_{lkp} + L_m // (n^2 L_{lks}) = L_{lkp} + L_m // L_{lkp} \quad (8)$$

When handling an actual transformer, equivalent circuit with L_p and L_r is preferred since these values can be easily measured with a given transformer. In an actual transformer, L_p and L_r can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively.

In Figure 8, notice that a virtual gain M_V is introduced, which is caused by the secondary-side leakage inductance. By adjusting the gain equation of Equation (6) using the modified equivalent circuit of Figure 8, the gain equation for integrated transformer is obtained:

$$M = \frac{2n \cdot V_O}{V_{IN}} = \left| \frac{(\frac{\omega}{\omega_o})^2 \cdot (m-1) \cdot M_V}{(\frac{\omega^2}{\omega_p^2} - 1) + j(\frac{\omega}{\omega_o}) \cdot (\frac{\omega^2}{\omega_o^2} - 1) \cdot (m-1) Q^e} \right| = \left| \frac{(\frac{\omega^2}{\omega_o^2}) \sqrt{m(m-1)}}{(\frac{\omega^2}{\omega_p^2} - 1) + j(\frac{\omega}{\omega_o}) \cdot (\frac{\omega^2}{\omega_o^2} - 1) \cdot (m-1) \cdot Q^e} \right| \quad (9)$$

where: $R_{ac}^{\ e} = \frac{8n^2}{\pi^2} \frac{R_o}{M_V^{\ 2}}$, $m = \frac{L_p}{L_r}$

$$Q^e = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{ac}^{\ e}}, \omega_o = \frac{1}{\sqrt{L_r C_r}}, \quad \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

The gain at the resonant frequency (ω_o) is fixed regardless of the load variation, which is given as:

$$M = M_V = \sqrt{\frac{L_p}{L_p - L_r}} = \sqrt{\frac{m}{m-1}} \quad at\ \omega = \omega_o \qquad (10)$$

The gain at the resonant frequency (ω_o) is unity when using individual core for series inductor, as shown in Equation (7). However, when implementing the magnetic components with integrated transformer, the gain at the resonant frequency (ω_o) is larger than unity due to the virtual gain caused by the leakage inductance in the transformer secondary side.

The gain of Equation (9) is plotted in Figure 8 for different Q^e values with m=3, f_o=100 kHz, and f_p=57 kHz. As observed in Figure 8, the LLC resonant converter shows gain characteristics almost independent of the load when the switching frequency is around the resonant frequency, f_o.

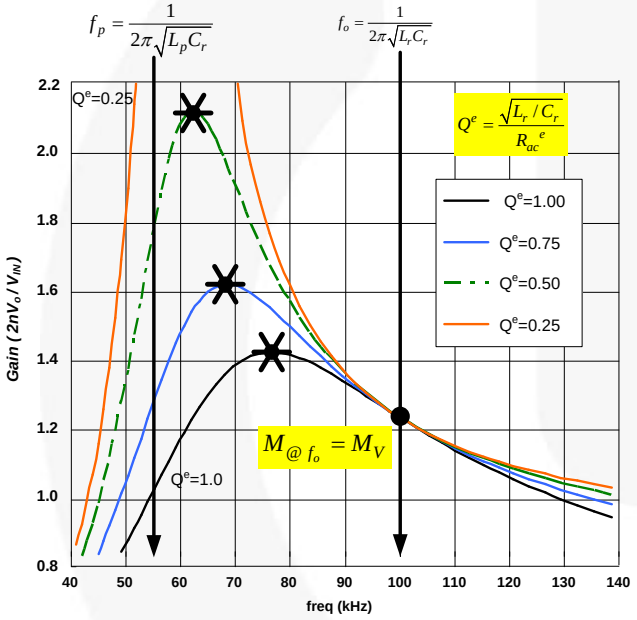


Figure 8. Typical Gain Curves of LLC Resonant Converter (*m*=3) Using an Integrated Transformer

Above the peak gain frequency, the input impedance of the resonant network is inductive and the input current of the resonant network (I_p) lags the voltage applied to the resonant network (V_d). This permits the MOSFETs to turn on with zero voltage (ZVS), as illustrated in Figure 10. Meanwhile, the input impedance of the resonant network becomes capacitive and I_p leads V_d below the peak gain frequency. When operating in capacitive region, the MOSFET body diode is reverse recovered during the switching transition, which results in severe noise. Another problem of entering into the capacitive region is that the output voltage becomes out of control since the slope of the gain is reversed. The minimum switching frequency should be well limited above the peak gain frequency.

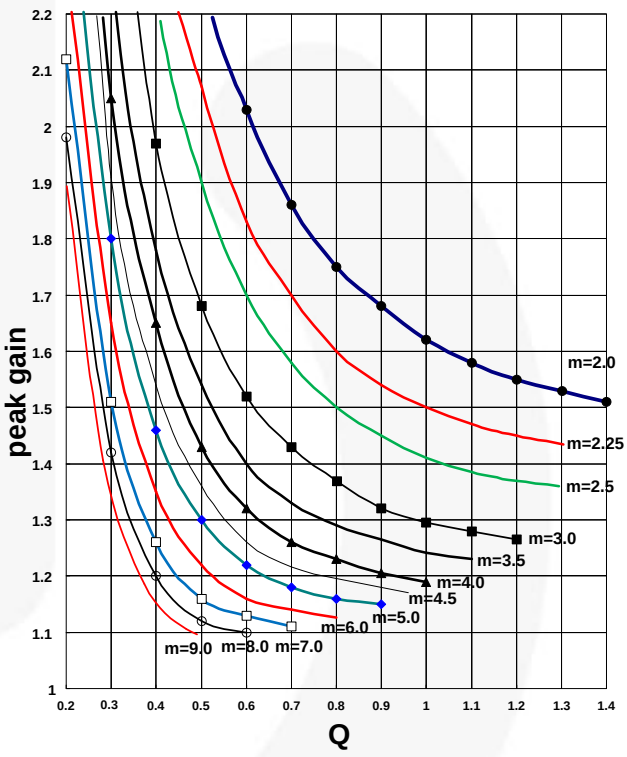


Figure 9. Peak Gain (Attainable Maximum Gain) vs. *Q* for Different *m* Values

Attainable Maximum Gain

Even though the peak gain at a given condition can be obtained by using the gain in Equation (6), it is difficult to express the peak gain in explicit form. To simplify the analysis and design, the peak gains are obtained using simulation tools and depicted in Figure 9, which shows how the peak gain (attainable maximum gain) varies with *Q* for different m values. It appears that higher peak gain can be obtained by reducing *m* or *Q* values. With a given resonant frequency (f_o) and *Q* value, decreasing *m* means reducing the magnetizing inductance, which results in increased circulating current. Accordingly, there is a trade-off between the available gain range and conduction loss.

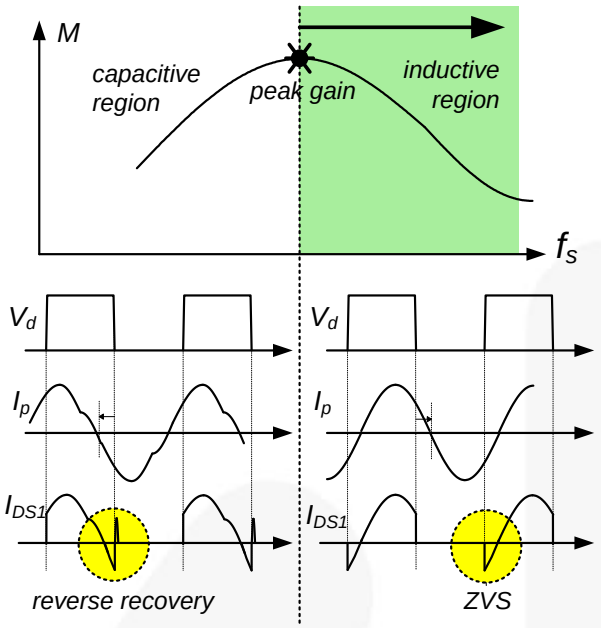


Figure 10. Operation Waveforms for Capacitive and Inductive Regions

Features of FAN7688

The FAN7688 is an advanced pulse frequency modulated (PFM) controller for LLC resonant converters with synchronous rectification (SR) that offers best in class efficiency for isolated DC/DC converters. It employs a current mode control technique based on a charge control, where the triangular waveform from the oscillator is combined with the integrated switch current information to determine the switching frequency. This provides a better control-to-output transfer function of the power stage simplifying the feedback loop design while allowing true input power limit capability. Closed loop soft-start prevents saturation of the error amplifier and allows monotonic rising of the output voltage regardless of load condition. A dual edge tracking adaptive dead time control minimizes the body diode conduction time thus maximizing efficiency.

Table 1 shows the pin description of FAN7688 and Figure 11 shows the typical application schematic of LLC resonant converter using FAN7688.

Table 1. Pin Description of FAN7688

Pin#	Name	Pin Description
1	5VB	5 V REF
2	PWMS	PWM mode entry level setting
3	FMIN	Minimum frequency setting pin
4	FB	Output voltage sensing for feedback control
5	COMP	Output of error amplifier
6	SS	Soft-start time programming pin
7	ICS	Current information integration pin for current mode control
8	CS	Current sensing for over-current protection
9	RDT	Dead time programming pin for the primary side switches and secondary side SR switches
10	SR1DS	SR1 Drain-to-source voltage detection
11	SROUT2	Gate drive output for the secondary side SR MOSFET 2
12	SROUT1	Gate drive output for the secondary side SR MOSFET 1
13	PROUT2	Gate drive output 2 for the primary side switch
14	PROUT1	Gate drive output 1 for the primary side switch
15	VDD	IC Supply voltage
16	GND	Ground

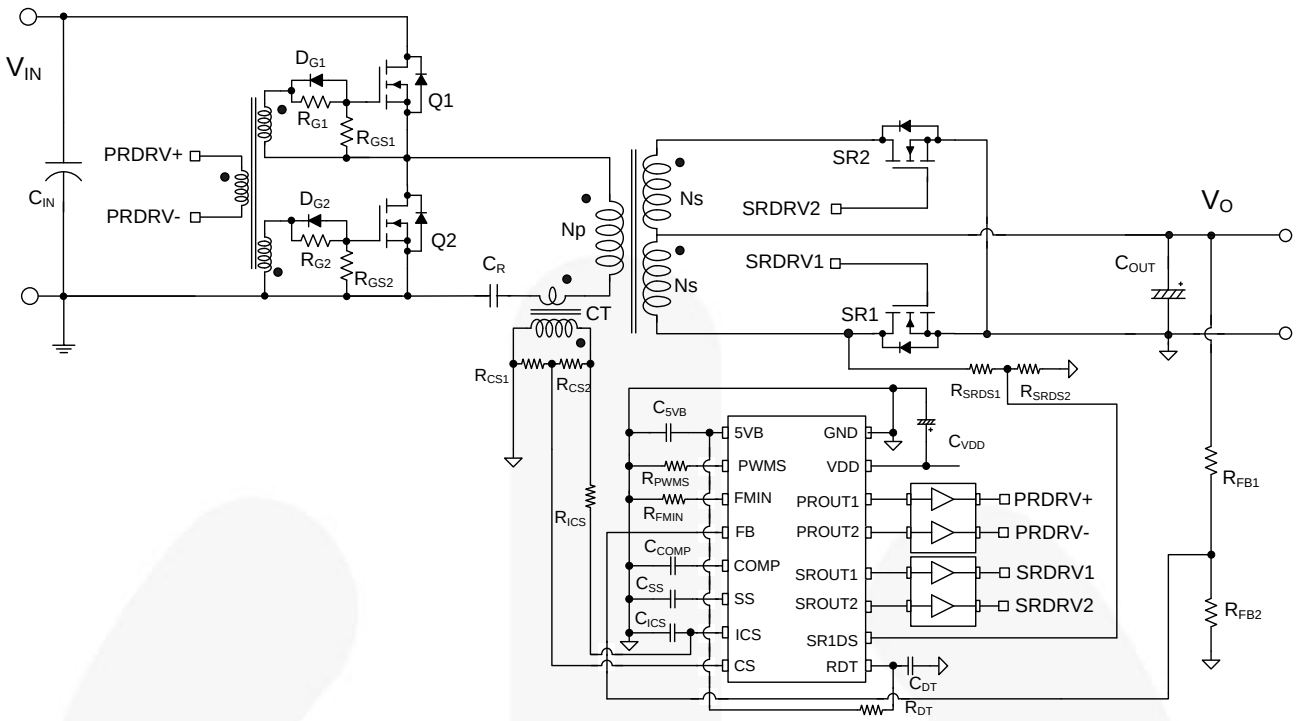


Figure 11. Schematic of Half-bridge LLC Resonant Converter

Design Procedure

In this section, a design procedure is presented using the schematic in Figure 11 as a reference where the resonant inductor is implemented using leakage inductance. A DC-DC converter with 250 W / 12.5 V output has been selected as a design example. The design specifications are as follows:

- Nominal Input Voltage: 400 V_{DC} (Output of PFC Stage)
- Output: 12.5 V / 20 A (250 W)
- Hold-up Time Requirement: 20 ms
- DC Link Capacitor of PFC Output: 150 µF

[STEP-1] Define the System Specifications

As a first step, define the following specification.

Estimated efficiency (E_{ff}): The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. With the estimated efficiency, the maximum input power is given as:

$$P_{IN} = \frac{P_{OUT}}{E_{ff}} \tag{11}$$

Minimum input voltage during holdup time: The maximum input voltage would be the nominal PFC output voltage as:

$$V_{IN}^{\max} = V_{O.PFC} \tag{12}$$

Even though the input voltage is regulated as constant by PFC pre-regulator, it drops during the hold-up time. The minimum input voltage considering the hold-up time requirement is given as:

$$V_{IN}^{\min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{IN}T_{HLD}}{C_{BLK}}} \tag{13}$$

where $V_{O.PFC}$ is the nominal PFC output voltage, T_{HLD} is a hold-up time, and C_{BLK} is the DC link bulk capacitor.

(Design Example) Assuming the efficiency is 96%,

$$P_{IN} = \frac{P_{OUT}}{E_{ff}} = \frac{250}{0.96} = 260.4W$$

$$V_{IN}^{\max} = V_{O.PFC} = 400V$$

With 20 ms holdup time, the minimum input voltage is obtained as:

$$V_{IN}^{\min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{IN}T_{HLD}}{C_{BLK}}} = 301V$$

[STEP-2] Determine the Voltage Gain Rage of the Resonant Network

Once the minimum and maximum input voltages of LLC resonant converter are determined in [STEP-1], the minimum and maximum gain can be determined.

The minimum gain is required for the nominal input voltage. To minimize the switching frequency variation with load, it is typical to operate the LLC resonant converter around the resonant frequency. The gain ($2nVo/V_{IN}$) at the resonant frequency is obtained as:

$$M_V = \left.\frac{2nV_O}{V_{IN}}\right|_{fsw=f_O} = \sqrt{\frac{m}{m-1}} \tag{14}$$

During the holdup time, the PFC output voltage (input voltage of LLC resonant converter) drops and a higher gain is required to regulate the output voltage. The maximum voltage gain is given as:

$$M^{\max} = \frac{V_{IN}^{\max}}{V_{IN}^{\min}} M^{\min} \tag{15}$$

A peak gain can be obtained with a small *m* value; too small *m* value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set m to be 3~7.

(Design Example) The ratio (m) between L_p and L_r is chosen as 4.75. The minimum gain is obtained as:

$$M_{@f_O} = \sqrt{\frac{m}{m-1}} = \sqrt{\frac{4.75}{4.75-1}} = 1.13$$

The minimum gain at the maximum input voltage is selected as 1.1. Then, the maximum gain for minimum input voltage is obtained as:

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min} = \frac{400}{300} \cdot 1.1 = 1.46$$

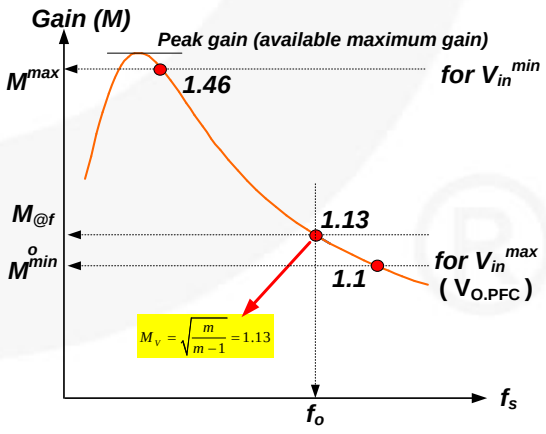


Figure 12. Maximum Gain / Minimum Gain

[STEP-3] Determine the Transformer Turns Ratio ($n=N_p/N_s$)

With the minimum gain (M^{min}) obtained in STEP-2, the transformer turns ratio is given as:

$$n = \frac{N_P}{N_S} = \frac{V_{IN}^{\max}}{2(V_O + V_F)} \cdot M^{\min} \quad (16)$$

where V_F is the secondary-side rectifier diode voltage drop.

(Design Example) Since SR is used in the rectifier, it is assumed that V_F is 0 V with a SR MOSFET with low $R_{DS.ON}$. Then, the transformer turns ratio is obtained as:

$$n = \frac{N_P}{N_S} = \frac{V_{IN}^{\max}}{2(V_O + V_F)} \cdot M^{\min} = 17.6$$

[STEP-4] Calculate the Equivalent Load Resistance

With the transformer turns ratio obtained from Equation (16), the equivalent load resistance is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2}\frac{V_o^2}{P_o} \quad (17)$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2}\frac{V_o^2}{P_o} = 157\Omega$$

[STEP-5] Design the Resonant Network

With m value chosen in STEP-2, read proper Q value from the peak gain curves in Figure 9 that allows required maximum gain. Since the peak gain curve is generated using fundamental approximation, the actual gain at below resonance is about 10~15% higher than that of the prediction using fundamental approximation.

Once the Q value is determined, the resonant parameters are obtained as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} \quad (18)$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} \quad (19)$$

$$L_p = m \cdot L_r \quad (20)$$

(Design Example)

As calculated in STEP-2, the maximum voltage gain (M^{max}) for the minimum input voltage (V_{IN}^{min}) is 1.46. m has been chosen as 4.75 in STEP-2 and Q is obtained as 0.42 from the peak gain curves in Figure 13.

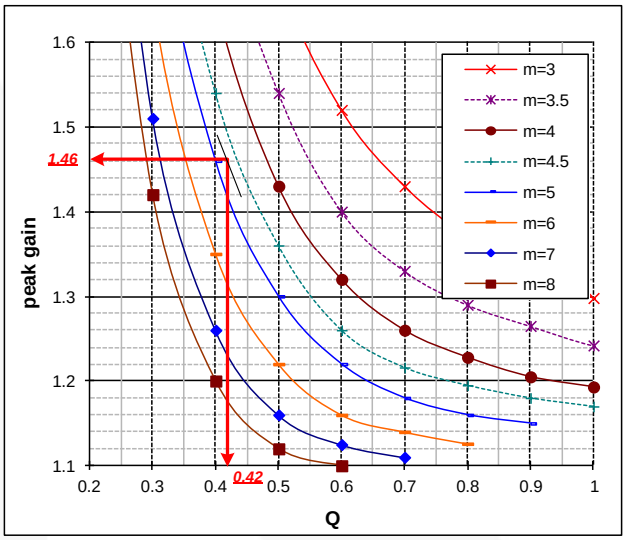


Figure 13. Resonant Network Design Using the Peak Gain (Attainable Maximum Gain)

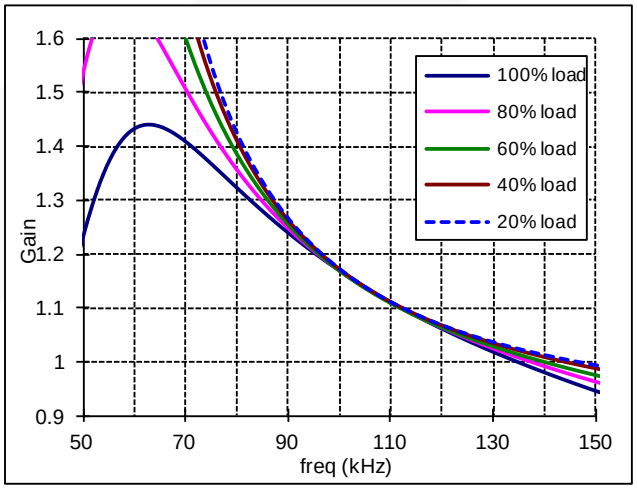
By selecting the resonant frequency as 106 kHz, the resonant components are determined as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} = 22.8nF, \quad L_r = \frac{1}{(2\pi f_o)^2 C_r} = 99\mu H$$

$$L_p = m \cdot L_r = 471\mu H$$

When building the transformer, the actual parameters are adjusted as below to accommodate the standard components value as Cr=22 nF, Lr=100 µH, Lp=475 µH and f_O=107 kHz.

The gain curve of final resonant network design using fundamental approximation is obtained as below.



Since the fundamental approximation yields lower peak gain than actual peak gain by 10~15% at below resonance operation, SIMPLIS simulation has been conducted as below to check the actual gain. The simulation results show that required maximum gain is obtained for 300 V input at 75 kHz. The simulation result also shows that the switching frequency at the nominal input voltage and full load condition is 110 kHz.

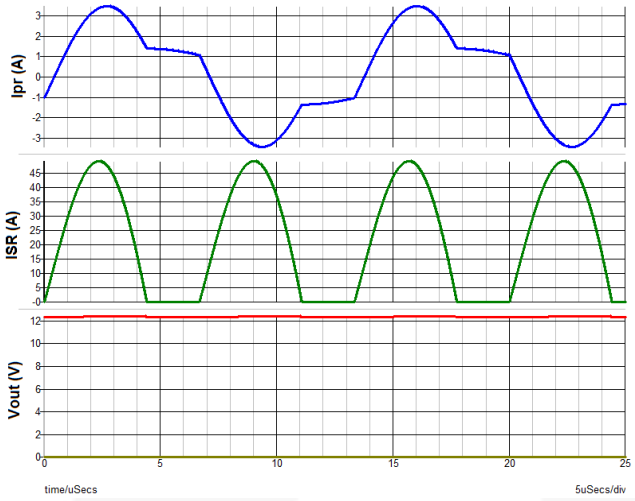


Figure 14. Simulation for V_{IN}=300 V, f_S=75 kHz, P_O=250 W

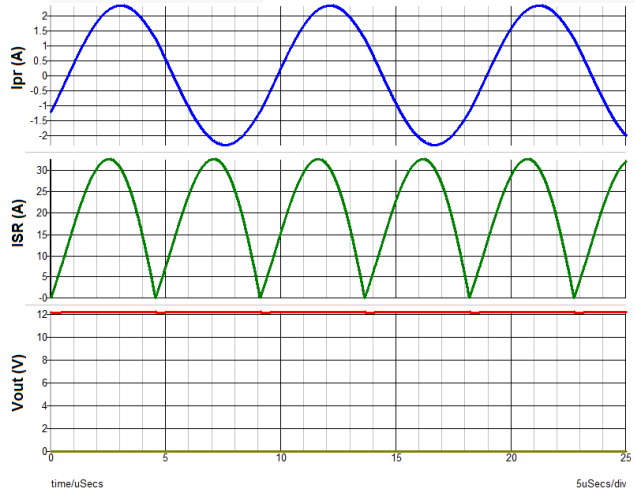


Figure 15. Simulation for V_{IN}=400 V, f_S=110 kHz, P_O=250 W

[STEP-6] Design the Transformer

Figure 16 shows the magnetizing current of transformer in LLC resonant converter. The required minimum number of turns of the primary side winding to limit the maximum flux below B_{max} is obtained as:

$$N_p^{\min} = \frac{n(V_o + V_F)}{4 f_o \cdot M_V \cdot B_{\max} \cdot A_e} \quad (21)$$

where A_e is the cross-sectional area of the transformer core in m^2 and ΔB is the maximum flux density swing in Tesla, as shown in Figure 16. If there is no reference data, use ΔB =0.2~0.3T to reduce the core loss. Notice that a virtual gain M_V is introduced, which is caused by the secondary-side leakage inductance (Refer to Figure 8).

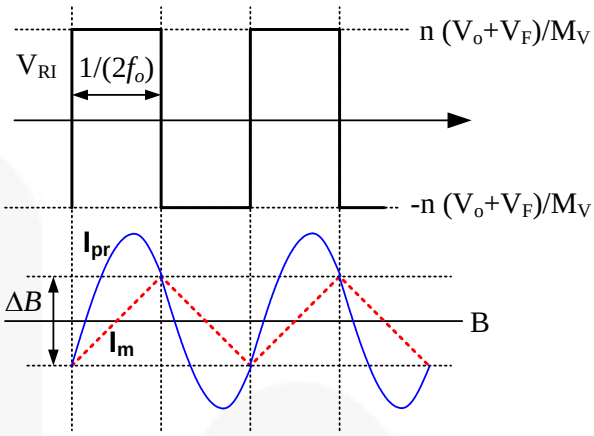


Figure 16. Flux Density Swing

Choose the proper number of turns for the secondary side resulting in primary-side turns larger than $N_p^{\min}$ as:

$$N_p = n \cdot N_s > N_p^{\min} \quad (22)$$

The wire gauge of primary and secondary side winding should be determined based on the RMS currents at nominal input voltage, which are given as:

$$I_{PR}^{RMS} \cong \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n}\right]^2 + \left[\frac{n(V_o + V_F)}{4\sqrt{2} f_o M_V (L_p - L_r)}\right]^2} \quad (23)$$

$$I_{SEC}^{RMS} \cong \frac{\pi I_o}{4} \text{ (each winding)} \quad (24)$$

(Design Example) ETD44 core (A_e=172mm^2) is selected for the transformer. Bmax is selected as 0.1T to reduce the core loss of the transformer. The minimum primary-side turns of the transformer is given as:

$$N_p^{\min} = N_p^{\min} = \frac{n(V_o + V_F)}{4 f_o \cdot M_V \cdot B_{\max} \cdot A_e} = 26.2 \; turns$$

$$N_p = n \cdot N_s = 2 \times 17.5 = 35 > N_p^{\min}$$

The RMS currents of the transformer windings at nominal input voltage are obtained as:

$$I_{PR}^{RMS} \cong \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n}\right]^2 + \left[\frac{n(V_o + V_F)}{4\sqrt{2} f_o M_V (L_p - L_r)}\right]^2} = 1.53A$$

$$I_{SEC}^{RMS} \cong \frac{\pi I_o}{4} = 15.7A$$

[STEP-7] Select the Resonant Capacitor

Figure 17 shows the primary side current (resonant capacitor current) waveforms for different operating conditions. When choosing the resonant capacitor, the current rating should be considered because a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor at nominal input voltage is has been obtained in equation (23).

The maximum resonant capacitor voltage at nominal input voltage and nominal load condition is given as:

$$V_{CR.NRM}{}^{\max} \cong \frac{V_{IN}{}^{\max}}{2} + \frac{I_O}{4 f_{SW} n \cdot C_R} \quad (25)$$

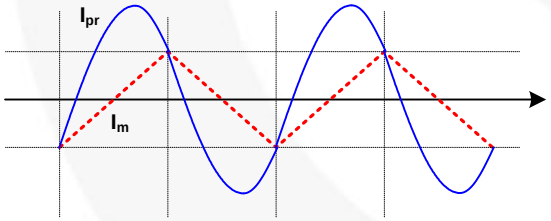
The voltage rating of the resonant capacitor should be determined based on the maximum voltage for each corner condition.

The maximum resonant capacitor voltage at nominal input voltage and output over current condition is given as:

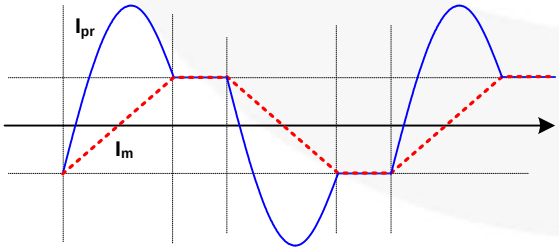
$$V_{CR.OPC}{}^{\max} \cong \frac{V_{IN}{}^{\max}}{2} + \frac{I_{O.OCP}}{4 f_{SW} n \cdot C_R} \quad (26)$$

The maximum resonant capacitor voltage at minimum input voltage and nominal load condition is given as:

$$V_{CR.VINMIN}{}^{\max} \cong \frac{V_{IN}{}^{\min}}{2} + [\frac{I_O}{4 f_{SW} n} + n \frac{(V_O + V_F)}{4 M_V L_m f_O} \cdot (\frac{1}{2 f_{SW}} - \frac{1}{2 f_O})] \frac{1}{C_R} \quad (27)$$



(a) Normal operation with nominal V_{IN}



(b) Below resonance operation with lower V_{IN} during holdup time

Figure 17. Primary Side Current Waveform of LLC Resonant Converter for different Operation Modes

(Design Example)

In [STEP-7], the RMS current of the resonant capacitor is calculated as $I_{PR}{}^{RMS} = 1.53A$

The maximum resonant capacitor voltage at nominal input voltage and nominal load condition is obtained as

$$V_{CR.NRM}{}^{\max} \cong \frac{V_{IN}{}^{\max}}{2} + \frac{I_O}{4 f_{SW} n C_R} = 317V$$

By setting the OCP level at 150% of nominal output current, the maximum resonant capacitor voltage at nominal input voltage and output over current condition is obtained as:

$$V_{CR.OCP}{}^{\max} \cong \frac{V_{IN}{}^{\max}}{2} + \frac{I_{O.OCP}}{4 f_{SW} n} = 376V$$

By setting the minimum frequency as 75kHz, the maximum resonant capacitor voltage at minimum input voltage and nominal load condition is given as:

$$V_{CR}{}^{\max} \cong [\frac{I_O}{2 f_{SW} n} + n \frac{(V_O + V_F)}{4 M_V f_O (L_p - L_r)} \cdot (\frac{1}{2 f_{SW}} - \frac{1}{2 f_O})] \frac{1}{C_R} + \frac{V_{IN}{}^{\min}}{2} = 434V$$

800VDC rated low-ESR film capacitor is selected for the resonant capacitor.

[STEP-8] Rectifier Network Design

When the center tap winding is used in the transformer secondary side, the diode voltage stress is twice the output voltage expressed as:

$$V_D = 2(V_o + V_F) \quad (28)$$

The RMS value of the current flowing through each rectifier diode is given as:

$$I_D{}^{RMS} = \frac{\pi}{4} I_o \quad (29)$$

Meanwhile, the ripple current flowing through output capacitor is given as:

$$I_{Co}{}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o{}^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o \quad (30)$$

The voltage ripple of the output capacitor is obtained as:

$$\Delta V_O \cong \frac{\pi}{2} I_o \cdot R_C + \frac{\frac{\pi}{2} I_o}{f_{SW} C_O} \times 0.067 \quad (31)$$

where R_C is the Effective Series Resistance (ESR) of the output capacitor and the power dissipation is the output capacitor is:

(Design Example) The voltage stress and current stress of the rectifier diode are:

$$V_{DS.SR} = 2(V_o + V_F) = 25V$$

$$I_{DS.SR}^{RMS} = \frac{\pi}{4} I_o = 15.7A$$

The 100 V / 20 A Schottky diode is selected for the rectifier considering the voltage overshoot caused by the stray inductance.

The RMS current of the output capacitor is:

$$I_{Co}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o = 9.64A$$

Four 1800 µF capacitors are use in parallel for the output capacitor. The current rating and ESR for each capacitor is 3.1 Arms and 9 mΩ.

The output capacitor ripple is calculated as:

$$\Delta V_O \cong \frac{\pi}{2} I_o \cdot R_C + \frac{\frac{\pi}{2} I_o}{f_{SW} C_O} \times 0.067 = 73mV$$

[STEP-9] Current Sensing Circuit Configuration

FAN7688 senses instantaneous switch current and the integral of the switch current as illustrated in Figure 18. Since FAN7688 is located in the secondary side, it is typical to use a current transformer for sensing the primary side current. While the PROUT1 is LOW, the ICS pin is clamped at 0 V with an internal reset MOSFET. Conversely, while PROUT1 is high, the ICS pin is not clamped and the integral capacitor (C_{ICS}) is charged and discharged by the voltage difference across R_{ICS} resistor. Since FAN7688 is using quasi-integral using RC filter, the current sensing resistor and current transformer turns ratio should be designed such that the voltage across the current sensing resistor (V_{SENSE}) is always larger than V_{ICS} to guarantee monotonic rising of V_{ICS} as shown in Figure 19. Figure 21 shows how the error of the quasi-integral circuit varies with the ratio between V_{ICS} peak voltage and V_{SENSE} at the falling edge of PROUT1 (V_{CM}). To obtain accurate integral, the current charging C_{ICS} should be proportional to V_{SENSE}, which is possible when V_{SENSE} is much larger than V_{ICS} and entire V_{SENSE} is applied across R_{ICS}. As can be seen, more accurate integral is obtained as the ratio between V_{ICS} peak voltage and V_{SENSE} at the falling edge of PROUT1 (V_{CM}) is smaller.

When the ratio between V_{ICS} peak voltage and V_{CM} is smaller than 0.5, quasi-integral with acceptable error (about 10%) is obtained. Since V_{ICS} peak voltage is below 1.2 V in normal operation, RCS1 and RCS2 should be selected such that VCM is larger than 2.4 V as:

$$V_{CM} = \frac{n(V_O + V_F)}{M_V (L_P - L_r)} \cdot \frac{1}{4 f_O} \cdot \frac{R_{CS1} + R_{CS2}}{n_{CT}} > 2.4V \quad (32)$$

The peak value of primary side current at nominal input voltage and full load is obtained as:

$$I_{PR}^{PK} \cong \sqrt{2} I_{PR}^{RMS} \quad (33)$$

The ration between R_{CS1} and R_{CS2} can be selected according to the primary side Over-Current Protection (OCP) trip point.

$$I_{PR.OCP} \cdot \frac{1}{n_{CT}} \times R_{CS1} = 3.5V \quad (34)$$

Assuming ideal integral, the peak voltage of V_{ICS} at above resonance is obtained as:

$$V_{ICS}^{PK} = [\frac{N_S}{N_P} \cdot \frac{I_O}{2 f_{SW}}] \times \frac{R_{CS1} + R_{CS2}}{n_{CT} \cdot R_{ICS}} \frac{1}{C_{ICS}} \quad (f_{SW} \geq f_O) \quad (35)$$

Assuming ideal integral, the peak voltage of V_{ICS} at below resonance is obtained as:

$$V_{ICS}^{PK} = [\frac{N_S}{N_P} \cdot \frac{I_O}{2 f_{SW}} + n \frac{(V_O + V_F)}{4 M_V L_m f_O} \cdot (\frac{1}{2 f_{SW}} - \frac{1}{2 f_O})] \times \frac{R_{CS1} + R_{CS2}}{n_{CT} \cdot R_{ICS}} \frac{1}{C_{ICS}} \quad (when\ f_{SW} \leq f_O) \quad (36)$$

Considering the internal discharge transistor of the ICS pin, the typical value of C_{ICS} is 1 nF. For accurate integral, 1% tolerance capacitor is recommended.

When, the ratio between V_{ICS} peak voltage and V_{CM} is not smaller enough, the attenuation factor of Figure 21 should be considered in equations (35) and (36).

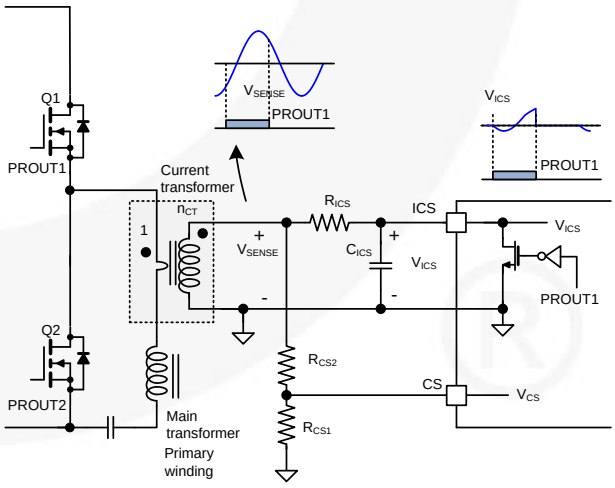
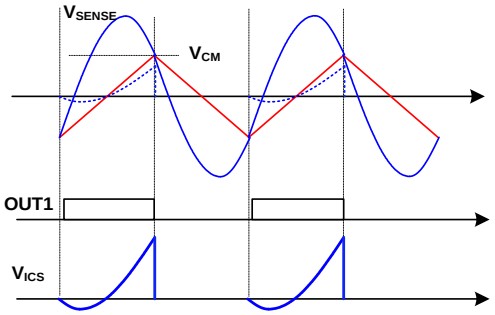
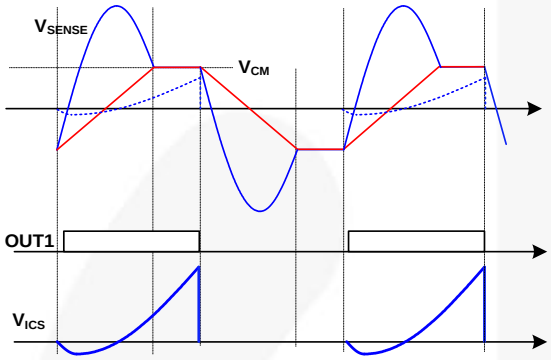


Figure 18. Typical Current Sensing Configuration



(a) Normal operation with nominal V_{IN}



(b) Below resonance operation with lower V_{IN}

Figure 19. ICS Pin Waveforms

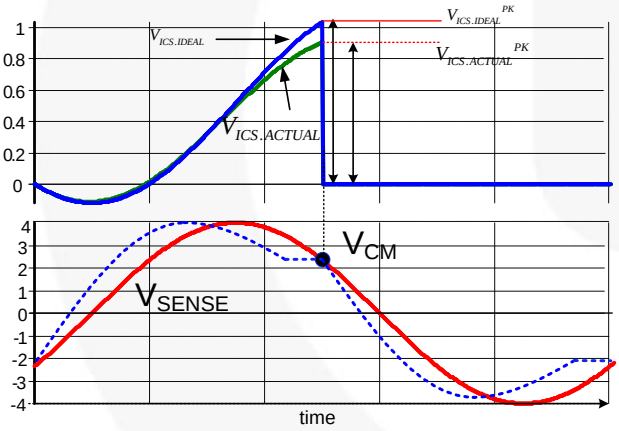


Figure 20. Definition of $V_{ICS.IDEAL}^{PK}$ and $V_{ICS.ACTUAL}^{PK}$

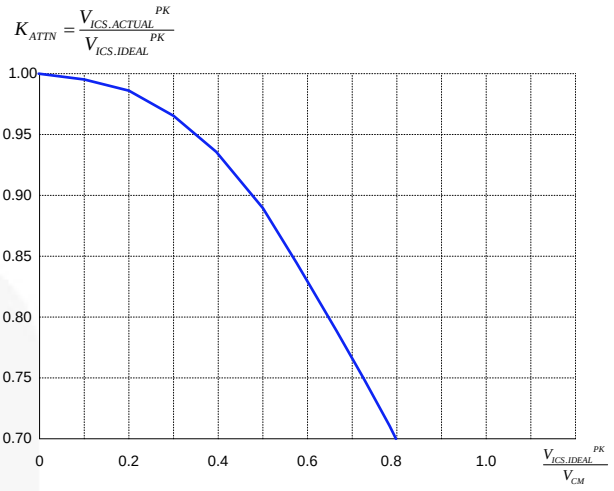


Figure 21. ICS Pin Voltage Attenuation vs. $V_{ICS.IDEAL}^{PK}/V_{CM}$

The peak value of the integral of the current sensing voltage (V_{ICS}) is proportional to the average input current of the LLC resonant converter as shown in Figure 22. Therefore, the load condition for SR enable/disable is determined as a percentage of full load condition according to which percentage of nominal power corresponds to input current limit threshold. Typically, 120% of nominal load condition is used for over current limit trip point; the SR is enabled and disabled at 15% and 7.5% of nominal load, respectively. If 140% of nominal load condition is used for over current limit trip point, the SR is enabled and disabled at 17.5% and 8.75% of nominal load, respectively. Additional slope on ICS pin voltage can be applied to obtain higher over current limit without increasing SR enable/disable points. This technique is typically used for longer holdup time. With a given slope compensation resistor, the additional slope added to ICS pin voltage is given as:

$$V_{ICS.SLP} = \frac{5V}{R_{SLP}C_{ICS}} \cdot \frac{1}{2f_{SW}} \quad (37)$$

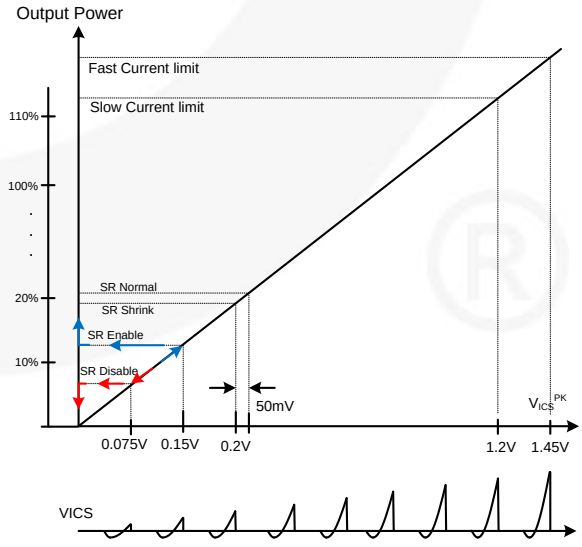


Figure 22. Load Condition and ICS Pin Voltage

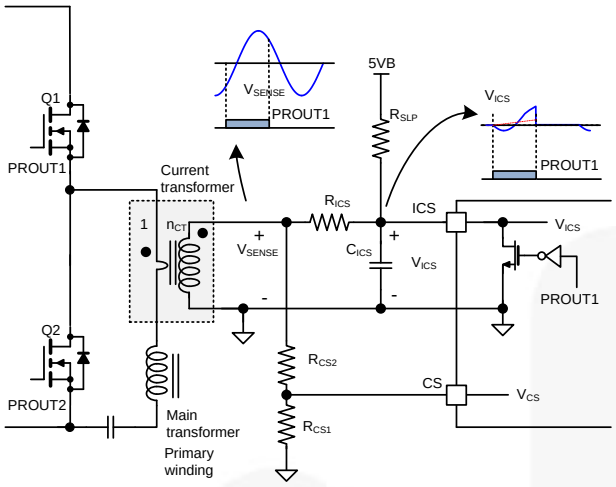


Figure 23. Current Sensing Configuration with Slope Compensation

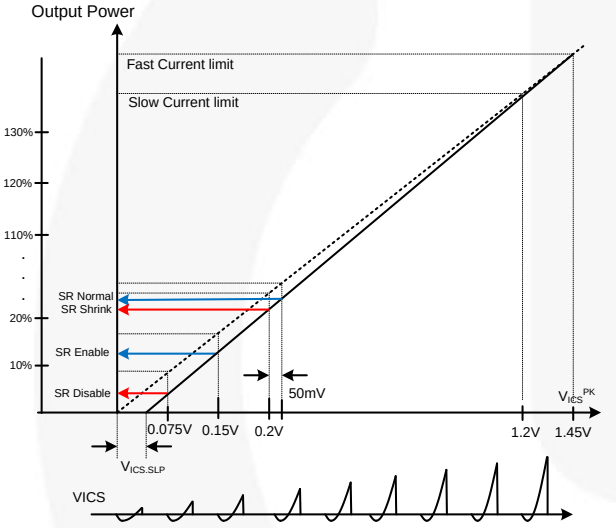


Figure 24. Load Condition and ICS Pin Voltage when Slope Compensation is added

(Design Example) With a current transformer with a turns ratio of 50 (n_{CT}), the recommended minimum value of the sum of R_{CS1} and R_{CS2} is given as

$$R_{CS1}+R_{CS2} > \frac{2.4 \cdot M_V (L_P - L_r) \cdot 4 f_O n_{CT}}{n(V_O + V_F)} = 99\Omega$$

Thus, sum of R_{CS1} and R_{CS2} is selected as 100 Ω.

The peak of primary side current at nominal input voltage and full load condition is given as

$$I_{PR}^{PK} \cong \sqrt{2} I_{PR}^{RMS} = 2.16A$$

By setting the primary side OCP level at 5.5 A,

$$R_{CS1} = 3.5V \frac{n_{CT}}{I_{PR.OCP}} = 31.8\Omega$$

With 200 kΩ slope compensation resistor, the additional slope added to ICS pin voltage is:

$$\frac{5V}{R_{SLP} C_{ICS}} \cdot \frac{1}{2 f_{SW}} \; V_{ICS.SLP} = \frac{5V}{R_{SLP} C_{ICS}} \cdot \frac{1}{2 f_{SW}} = 0.11V$$

Assuming the attenuation factor of V_{ICS} at 1.2 V is 0.9 (reading from Figure 21 at x=1.2/2.43), the proper R_{ICS} resistor to have 30 A overload protection at nominal input voltage is:

$$R_{ICS} = [\frac{N_S}{N_P} \cdot \frac{I_{O.OLP}}{2 f_{SW}}] \times \frac{(R_{CS1} + R_{CS2}) \cdot 0.90}{n_{CT} \cdot (1.2 - V_{ICS.SLP})} \frac{1}{C_{ICS}}$$
$$= 12.8k\Omega$$

Assuming the attenuation factor of VICS at 1.45 V is 0.82 (reading y axis at x=1.45/2.43=0.588 from Figure 21), the V_{ICS} peak voltage at minimum input voltage during holdup time is given as:

$$V_{ICS}^{PK} = [\frac{N_S}{N_P} \cdot \frac{I_O}{2 f_{SW}} + n \frac{(V_O + V_F)}{4 M_V L_m f_O} \cdot (\frac{1}{2 f_{SW}} - \frac{1}{2 f_O})]$$
$$\times \frac{R_{CS1} + R_{CS2}}{n_{CT} \cdot R_{ICS}} \frac{0.82}{C_{ICS}} + \frac{5V}{R_{SLP} C_{ICS}} \cdot \frac{1}{2 f_{SW}} = 1.45V$$

[STEP-10] Soft-Start Capacitor

The soft-start time can be programmed using soft-start capacitor as:

$$T_{SS} = \frac{C_{SS} \times 2.4V}{I_{SS}} \quad (38)$$

Too short soft-start time forces the LLC resonant converter to draw too much current from the input voltage resulting on over load protection during startup. Therefore, the soft-start time should be well matched with the available rising time of the output capacitor as:

$$T_{SS} = \frac{C_{SS} \times 2.4V}{I_{SS}} > \frac{C_{OUT} \cdot V_O}{I_{O.OLP} - I_O} \quad (39)$$

(Design Example) The output capacitor is 7200 μF in total. Then, the soft-start time should be:

$$T_{SS} = \frac{C_{SS} \times 2.4V}{I_{SS}} > \frac{C_{OUT} \cdot V_O}{I_{O.OLP} - I_O} = 9ms$$

Be selecting 50 ms soft-start time, the soft-start capacitor is obtained as:

$$C_{SS} = \frac{T_{SS} I_{SS}}{2.4} = 833nF$$

820 nF standard capacitor value is selected for the final design.

[STEP-11] Minimum Frequency Setting

The minimum switching frequency is limited by comparing the Timing Capacitor Voltage (V_{CT}) with an internal 3 V reference as shown in Figure 25. Since the rising slope of the timing capacitor voltage is determined by the resistor (R_{FMIN}) connected to FMIN pin, the minimum switching frequency is given as:

$$f_{SW.MIN} = 100kHz \times \frac{10k\Omega}{R_{FMIN}} \quad (40)$$

The minimum programmable switching frequency is limited by the digital counter running on an internal 40 MHz clock. Since a 10 bit counter is used, the minimum switching frequency given by the digital oscillator is 39 kHz (40 MHz/1024=39 kHz). Therefore, the maximum allowable value for R_{FMIN} is 25.5 kΩ

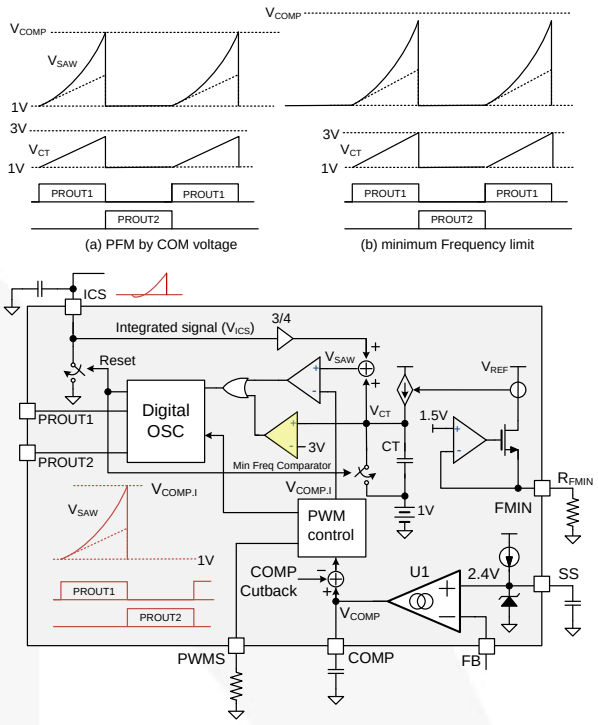


Figure 25. Minimum Switching Frequency Setting

(Design Example) The frequency at minimum input voltage and full load condition during holdup time is 75 kHz by SIMPLIS simulation result in [STEP-5]. With some margin, the minimum frequency of FAN7688 is selected as 67 kHz. Then the RFMIN is obtained as:

$$R_{FMIN} = 100kHz \times \frac{10k\Omega}{f_{SW.MIN}} = 14.9k\Omega$$

15 kΩ standard resistor value is selected for the final design.

[STEP-12] PWM Mode Entry Level Setting

FAN7688 employs hybrid control where the PFM is switched to pulse width modulation (PWM) mode at light load as illustrated in Figure 26. When the error amplifier voltage (V_{COMP}) is below the PWM mode threshold, the internal COMP signal is clamped at the threshold level and the PFM operation switches to PWM mode. In PWM mode, the switching frequency is fixed by the clamped internal COMP voltage and then the duty cycle is determined by the difference between COMP voltage and the PWM mode threshold voltage. Thus, the duty cycle decreases as V_{COMP} drops below the PWM mode threshold, which limits the switching frequency at light load condition as illustrated in Figure 26. The PWM mode threshold ($V_{COMP.PWM}$) can be programmed between 1.5 V and 1.9 V using a resistor on the PWMS pin.

Once the PWM mode threshold voltage is determined, the switching frequency at PWM mode is given as:

$$f_{SW.PWM} \cong \frac{2}{V_{COMP.PWM} - 1} \cdot f_{MIN} \quad (41)$$

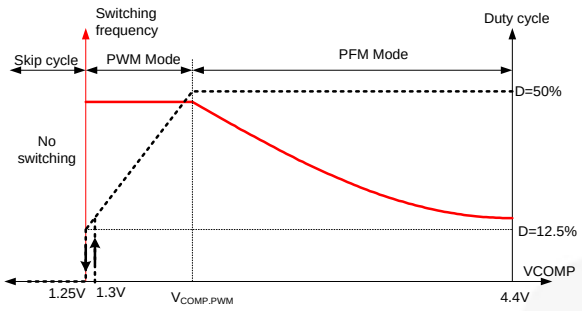


Figure 26. Mode Change with COMP Voltage

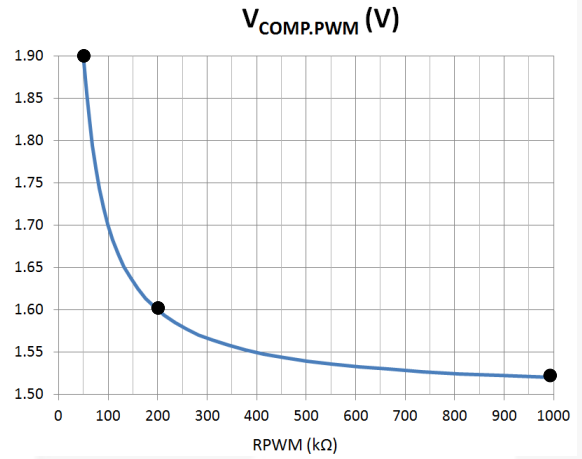


Figure 27. PWM Mode Entry Level Setting

(Design Example) With $V_{COMP.PWM}$=1.5 V, the switching frequency at PWM mode is given as

$$f_{SW.PWM} \cong \frac{2}{V_{COMP.PWM} - 1} \cdot f_{MIN} = 268kHz$$

R_{PWM} is selected as 1 MΩ.

[STEP-13] Dead Time Setting

With a single pin (RDT pin), the dead times between the primary side gate drive signals (PROUT1 and PROUT2) and secondary side SR gate drive signal (SROUT1 and SROUT2) are programmed using a switched current source as shown in Figure 28 and Figure 29. Once the 5 V bias is enabled, the RDT pin voltage is pulled up. When the RDT pin voltage reaches 1.4 V, the voltage across C_{DT} is then discharged down to 1 V by an internal current source I_{DT}. I_{DT} is then disabled and the RDT pin voltage is charged up by the RDT resistor. As highlighted in Figure 29, 1/64 of the time required (T_{SET1}) for RDT pin voltage to rise from 1 V to 3 V determines the dead time between the secondary side SR gate drive signals.

The switched current source I_{DT} is then enabled and the RDT pin voltage is discharged. 1/32 of the time required (T_{SET2}) for the RDT pin voltage to drop from 3 V to 1 V determines the dead time between the primary side gate drive signals. After the RDT voltage drops to 1 V, the current source I_{DT} is disabled a second time, allowing the RDT voltage to be charged up to 5 V.

Table 1 shows the dead times for SROUT and PROUT programmed with recommended R_{DT} and C_{DT} component values. Since the time is measured by an internal 40 MHz clock signal, the resolution of the dead time setting is 25 ns. The minimum and maximum dead times are therefore limited at 75 ns and 375 ns respectively. To assure stable SR operation while taking circuit parameter tolerance into account, less than 75 ns dead time is not recommended especially for the SR dead time.

The required dead time for the primary side MOSFETs can be obtained as:

$$T_{D.PROUT} > \frac{\pi}{2} \cdot \frac{V_{IN}^{max} \cdot 2C_{OSS}}{I_{CM}} \quad (42)$$

where C_{OSS} effective capacitance across drain to source of primary side MOSFET and I_{CM} is the peak of magnetizing current as:

$$I_{CM} = \frac{N_P}{N_S} \cdot \frac{V_O + V_F}{(L_P - L_r)} \frac{1}{4 f_O} \quad (43)$$

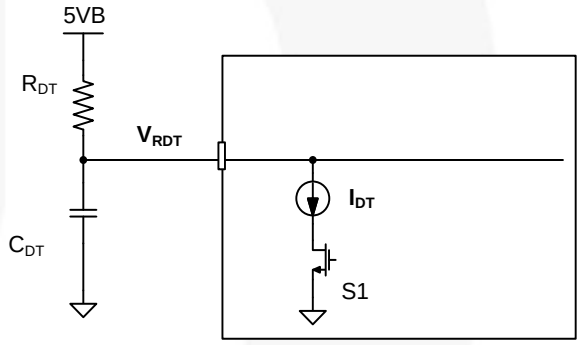


Figure 28. Internal Current Source for of RDT Pin

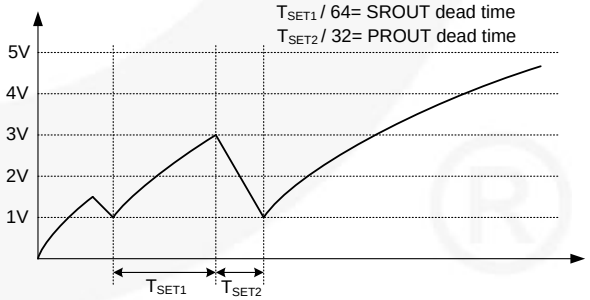


Figure 29. Multi-Function Operation of RDT Pin

Table 2. Dead Time Setting for PROUT and SROUT

	C_{DT}=180 pF		C_{DT}=220 pF		C_{DT}=270 pF		C_{DT}=330 pF		C_{DT}=390 pF		C_{DT}=470 pF		C_{DT}=560 pF	
R_{DT}	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)
28k	~~75~~	375	~~75~~	375	~~75~~	375	100	375	125	375	150	375	175	375
30k	~~75~~	250	~~75~~	325	100	375	100	375	125	375	150	375	175	375
33k	~~75~~	200	~~75~~	250	100	300	125	375	150	375	175	375	200	375
36k	~~75~~	175	~~75~~	200	100	250	125	325	150	375	175	375	225	375
40k	~~75~~	150	100	175	125	225	150	275	175	325	200	375	250	375
44k	~~75~~	125	100	150	125	200	150	250	175	300	225	350	275	375
48k	100	125	125	150	150	175	175	225	200	275	250	325	300	375
53k	100	100	125	125	150	175	200	200	225	250	275	300	325	375
58k	125	100	150	125	175	150	200	200	250	250	300	300	350	350
64k	125	100	150	125	175	150	225	200	275	225	325	275	375	325
71k	150	100	175	125	200	150	250	175	300	225	350	250	375	325
78k	150	100	175	100	225	150	275	175	325	200	375	250	375	300
86k	175	~~75~~	200	100	250	125	300	175	375	200	375	250	375	300
94k	175	~~75~~	225	100	275	125	325	175	375	200	375	225	375	275
104k	200	~~75~~	250	100	300	125	375	150	375	200	375	225	375	275
114k	225	~~75~~	275	100	325	125	375	150	375	175	375	225	375	275
126k	250	~~75~~	300	100	375	125	375	150	375	175	375	225	375	275
138k	275	~~75~~	325	100	375	125	375	150	375	175	375	225	375	250
152k	300	~~75~~	350	100	375	125	375	150	375	175	375	225	375	250

(Design Example) The peak of magnetizing current is obtained as:

$$I_{CM} = \frac{N_P}{N_S} \cdot \frac{V_O + V_F}{(L_P - L_r)M_V} \cdot \frac{1}{4 f_O} = 1.21A$$

Assuming FCB20N60 is used in the primary side, the effective output capacitance is 165 pF. Then, the minimum dead time for the primary side MOSFETs is obtained as:

$$T_{D.PROUT} > \frac{\pi}{2} \cdot \frac{V_{IN}^{\max} \cdot 2C_{OSS}}{I_{CM}} = 170ns$$

To guarantee stable ZVS operation against load variation and stray capacitance, 350 ns dead time is selected for the primary side MOSFETs.
For the secondary side SR, 200 ns dead time is selected.

By choosing C_{DT}=470 pF, RDT is chosen as 43 kΩ.

[STEP-14] SR Drain voltage sensing

The SR conduction times for SR1 and SR2 for each switching cycle are measured using a single pin (SR1DS pin). The SR1DS voltage and its delayed signal, resulting from a 100 ns RC time constant, are compared as shown in Figure 30. When the SR is conducting, the SR1DS voltage is clamped to either ground or the high voltage rail (2 times the output voltage) as illustrated in Figure 31. Whereas, SR1DS voltage changes fast when there is a switching transition. When both of the SR MOSFETs are turned off, the SR1DS voltage oscillates. When the SR1DS voltage changes faster than 0.25 V / 100 ns on the rising edge and 0.2 V / 100 ns on the falling edge the switching transition of the SR conduction state is detected. Based on the detected switching transition, FAN7688 predicts the SR current zero crossing instant for the next switching cycle. The 100 ns detection delay caused by the RC time constant is compensated in the internal timing detection circuit for a correct gate drive for SR.

Figure 31 and Figure 32 show the typical waveforms of SR1DS pin voltage together with other key waveforms. Since the voltage rating of SR1DS pin is 4 V, the voltage divider should be properly designed such that no over-voltage is applied to this pin as:

$$R_{DS2} > (\frac{2V_O}{4} - 1) \cdot R_{DS1} \quad (44)$$

Additional bypass capacitor (C_{DS}) can be connected to SR1DS pin to improve noise immunity. However, the equivalent time constant generated from the bypass capacitor and voltage divider resistors should be smaller than the internal RC time constant (100 ns) of the detection circuit for proper SR current zero crossing detection.

$$C_{DS} < \frac{100ns}{(R_{DS1} // R_{DS2})} \quad (45)$$

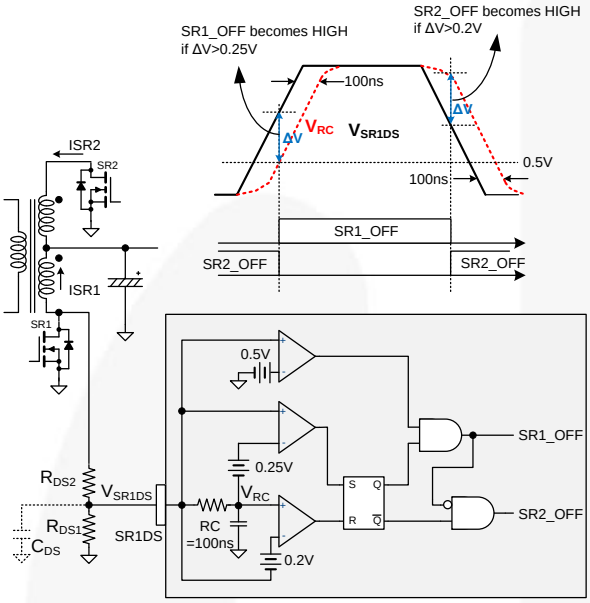


Figure 30. SR Conduction Detection with Single Pin (SR1DS Pin)

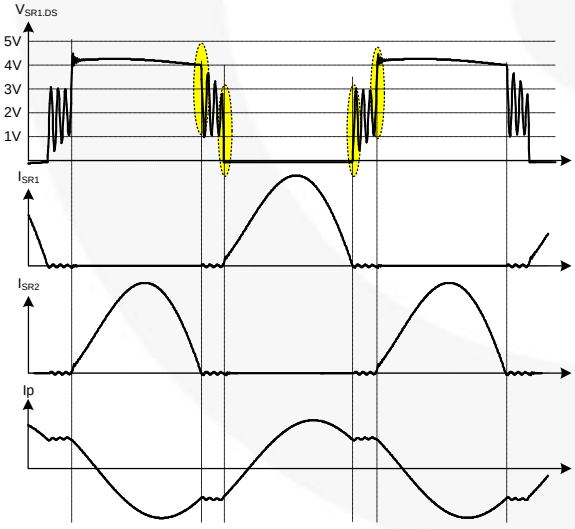


Figure 31. SR Conduction Detection Waveform at below Resonance Operation

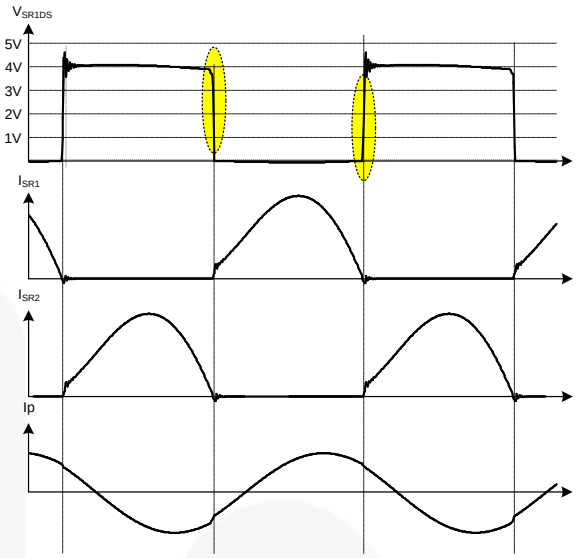


Figure 32. SR Conduction Detection Waveform at above Resonance Operation

(Design Example) By choosing 2.7 kΩ for R_{DS1}, the minimum R_{DS2} is obtained as:

$$R_{DS2} > (\frac{2V_O}{4} - 1) \cdot R_{DS1} = 14.2k\Omega$$

After selecting R_{DS2}=15 kΩ, the maximum filter capacitance on C_{DS} is obtained as:

$$C_{DS} < \frac{100ns}{(R_{DS1} // R_{DS2})} = 44pF$$

Thus, 33 pF is selected for C_{DS}.

Design Summary

Figure 33 shows the final schematic of the design example. ETD44 is used for the transformer and the resonant inductor is implemented using the leakage inductance.

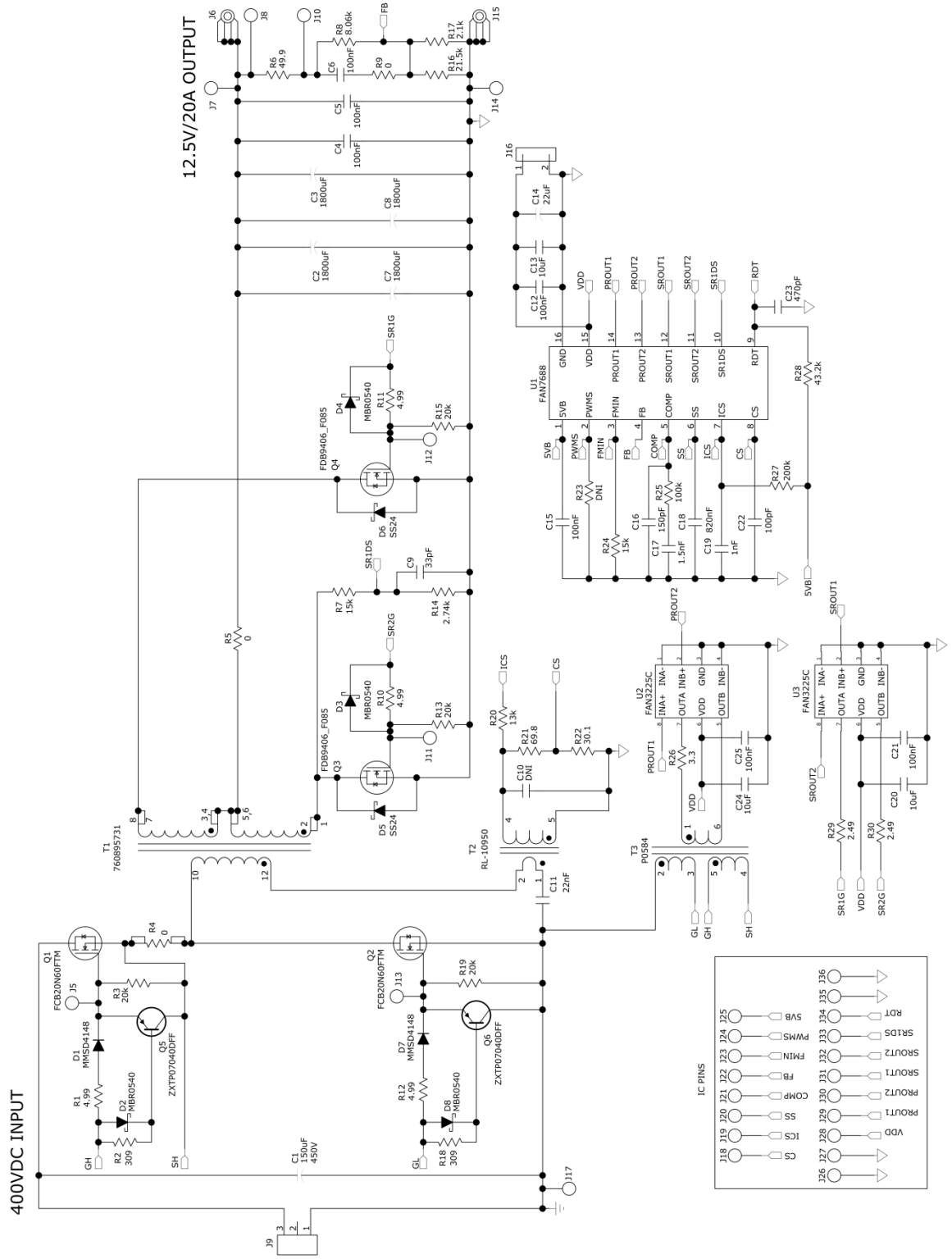


Figure 33. Final Schematic of Half-Bridge LLC Resonant Converter using FAN7688

760895731 from Wurth Elektronik (www.we-online.com) is a LLC transformer orderable from Digikey. A split bobbin is used to incorporate the resonant inductance (leakage inductance) and magnetizing inductance into a single magnetic component.

- Core: ETD44 (A_e=172 mm^2)
- Bobbin: 16 Pin TH
- Magnetizing Inductance : 475 µH, ±10%
- Leakage Inductance: 100 µH, ±10%

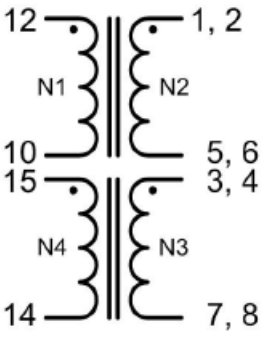


Figure 34. LLC Power Transformer (T1) in the Evaluation Board

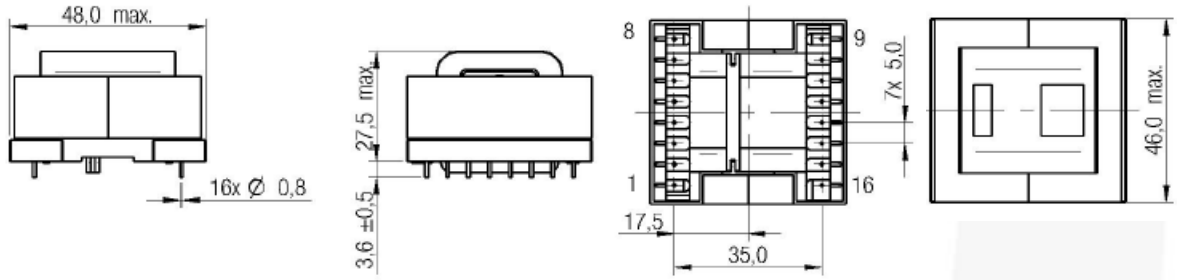


Figure 35. Wurth 760895731 Mechanical Drawing (dimensions in mm)

Table 3. Wurth 760895731 Transformer Electrical Specifications

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	475	µH	±10%
Turns ratio		n	35 : 2 : 2 : 3		±3%
Saturation current	$\|\Delta L/L\| < 20\%$	I_{sat}	5.0	A	typ.
DC Resistance 1	@ 20°C	R_{DC1}	128	mΩ	max.
DC Resistance 2	@ 20°C	R_{DC2}	4.0	mΩ	max.
DC Resistance 3	@ 20°C	R_{DC3}	4.0	mΩ	max.
DC Resistance 4	@ 20°C	R_{DC4}	192	mΩ	max.
Leakage inductance	100 kHz/ 100 mV	L_S	100	µH	±10%
Insulation test voltage	W1,4 => W2,3	U_T	4000	V (AC)	

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