LINEAR TECHNOLOGY

DESIGN NOTES

Sampling of Signals for Digital Filtering and Gated Measurements – Design Note 2

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Introduction

For many signal processing applications a sample and hold function is required in a data acquisition system. It is often critical for the processing system to know the exact value of an analog input at an exact time. In DSP applications such as digital filters, the usable bandwidth of the system is limited by the Nyquist frequency and the sample and hold bandwidth need only be, and is often intentionally limited to, one half the sampling rate. However, another area of application requires infrequently capturing instantaneous values of relatively fast signals, sometimes referred to as gated measurements. In the extreme case of pulse height measurements, only one sample point is required. Here, the sample and hold bandwidth should be as high as possible even though the sampling rate is very low.

The LTC®1090 excels in both environments. This note shows how the LTC1090 sample and hold can be synchronized to an external event and gives two simple applications: an 8-channel data acquisition system with digital filtering, and the gated measurement of a 1MHz sine wave.

The LTC1090 Sample and Hold

The LTC1090 provides a sample and hold which is fast, accurate and can be synchronized to an external event. Although the sampling rate is limited by the A/D conversion and data transfer rate to about 30kHz, the signal bandwidth of the sample and hold exceeds 1MHz. The acquisition time is less than 1µs to 0.1% (1LSB). Accuracy is so good, in fact, that it is possible to include all the sample and hold's error contributions (offset, gain, hold step, droop rate, etc.) into the converter specification and still maintain overall system accuracy of ±0.05% (±0.5LSB) over temperature.

Sampling occurs on the failing edge of the last data transfer clock pulse as described in the LTC1090 data sheet. Figure 1 shows a typical application which includes circuitry to synchronize sampling to an external sample clock, f_S.

8-Channel Data Acquisition System with Digital Filter

The circuit of Figure 1 contains an LTC1090 providing multiplexing, sample and hold, A/D conversion and data transfer to the microcontroller (MCU). An MC68HC05C4 is used as the controller (much higher filter performance may be achieved with a dedicated DSP processor). The MCU communicates with the LTC1090 over the serial peripheral interface (SPI), performs the digital filtering algorithm and provides the filtered data on its output port. The DAC provides reconstruction of the filtered waveform for viewing on an oscilloscope or spectrum analyzer. The 74C74 and 74C00 synchronize the sampling of the LTC1090 to the externally applied sample clock, f_S.

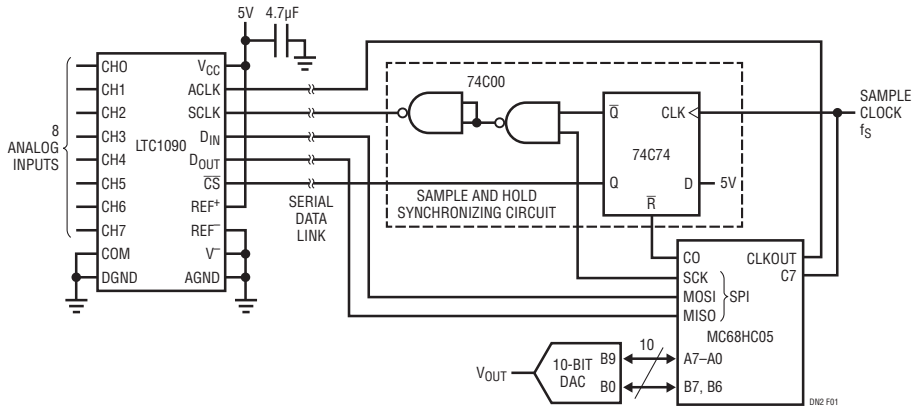

Figure 1. 8-Channel Data Acquisition System Showing Sample and Hold Synchronizing Circuitry

In Figure 1, the MCU initiates a two-byte serial data exchange with the LTC1090. This configures the LTC1090 for the next conversion, simultaneously reads back the previous conversion result and resets the 74C74. The LTC1090 will sample the analog input when the last shift clock (SCLK) pulse fails, so the MCU must end the data transfer by leaving the SCLK in a high state. This inhibits sampling of the selected analog input. When the sample clock, f_S, rises, it clocks the 74C74 which raises the $\overline{CS}$ and drops the SCLK. This failing SCLK causes the sample to be taken and starts the conversion. After the MCU senses the rising sample clock, it waits for the conversion to be completed (44 ACLK cycles) and then initiates another data exchange, preparing the LTC1090 for the next sample. This cycle repeats.

4th Order Elliptic Filter

Using the circuit of Figure 1, a 4th order elliptic digital filter was implemented. 10-bit input and output data words and 14-bit coefficients were used with the same coefficients being used for each channel. A direct form II IIR filter was implemented according the following equations:

$$D(n)=[7203 \bullet D(n-1) - 19209 \bullet D(n-2) + 6324 \bullet D(n-3) - 4383 \bullet D(n-4)] \bullet 2^{-14} + X(n)$$

$$Y(n)=[3069 \bullet D(n) + 5505 \bullet D(n-1) + 7824 \bullet D(n-2) + 5504 \bullet D(n-3) + 3066 \bullet D(n-4)] \bullet 2^{-14}$$

where: X(n) = filter input value
Y (n) = filter output value
D(n) = delay node value

The filter frequency response is shown in Figure 2. The cutoff frequency is 175Hz, one fourth the sample frequency of 700Hz. The cutoff frequency of the filter can be tuned by varying the frequency of the sample clock.

Because of 68HC05 speed and instruction set limitations, sample rate is limited by the MCU's ability to perform the DSP algorithm. Maximum sample rate was determined to be 700Hz for a single channel filter and 90Hz for eight channels. Using a high performance DSP would allow sample rates approaching the limit of 30kHz for one channel and 3.7kHz for all eight set by the LTC1090. Hopefully, this simple example will encourage the reader to pursue higher order, higher performance applications.

If large amplitude, unwanted AC signals are present on the inputs, a linear filter such as the LTC1062 can be used to remove them and prevent reduction in the dynamic range of the system.

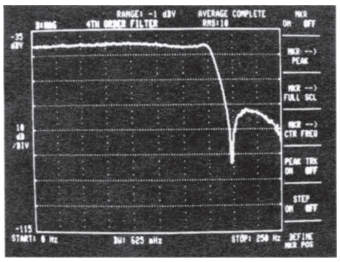

Figure 2. Spectrum of 4th Order Elliptic Digital Filter Used in the Data Acquisition System, f_C = 175Hz

Gated Measurements of Fast Signals

As an example of gated measurements, the circuit of Figure 1 was used with no filtering to repetitively sample a $5V_{P-P}$ 1MHz sine wave. The waveform was sampled at 15kHz (approximately one sample every 67 cycles of the 1MHz waveform). A 20ns pulse, triggered off the sample clock, was applied to the z-axis input of a storage scope to illuminate one dot on the CRT per sample. Samples were allowed to accumulate on the storage scope as shown in Figure 3. The upper waveform is the sampled input to the LTC1090 and the lower waveform is the sampled output of the DAC. (Remember that the waveforms are not real time: one dot was illuminated only every 67 cycles of the 1MHz sine wave.) With this technique, the signal bandwidth of the LTC1090 sample and hold was determined to be 2MHz.

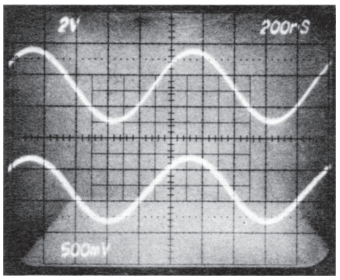

Figure 3. Input and Output Sample Points of a 1MHz Sine Wave Accumulated on a Storage Scope

Using the LTC1090 sample and hold, high speed circuits such as a 1MHz bandwidth AC to DC converter are possible. Because the acquisition time is less than 1µs, it is also possible to make a gated measurement of the height of a pulse as narrow as 1µs to 0.1% accuracy.

Data Sheet Download

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