Single-Output High-Side N-Channel Power MOSFET Gate Driver Application and Circuit of the TPD7104AF Reference Guide
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1. Overview

Mechanical relays have traditionally been used as switches to open and close a path between a power supply (e.g., Battery) and a load. However, because mechanical contacts have limited life wearing out with on/off cycles, semiconductor-based solid-state relays are coming into widespread use for applications requiring long-term reliability. Increasing of complex system requirement, solid-state relays must have more capability, especially a load switch with low-on-resistance discrete N-channel power MOSFETs can be used to create a high-current solid-state relay while reducing its power loss and heat generation.

The TPD7104AF is a single-output N-channel power MOSFET gate driver with a charge pump for high-side switch applications and it can realize a high current load switch with external discrete N-channel MOSFETs. The TPD7104AF also has a comparator for Load Short-circuit (Overcurrent) Detection and a Power Supply Reverse Connection Protection circuit in order to protect and ensure safe operation of high-current applications that have unexpected such kind of accidents.

This reference guide focuses on the operations and applications of load short-circuit detection and Power Supply Reverse Connection Protection available with the TPD7104AF that are crucial for the safe function of systems with high-current load switches.

For details of other features and functions of the TPD7104AF, see its datasheet.

To download the datasheet for the TPD7104AF → Click Here

1.1. Target applications

- Solid-state relays
- Battery management systems (BMS)

Circuit example

* Toshiba offers a portfolio of MOSFETs suitable for these applications.

For details of MOSFETs → Click Here
2. Load Short-circuit (Overcurrent) Detection circuit

2.1. Circuit example

Figure 2.1.1 shows an example of a circuit for Load Short-circuit (Overcurrent) Detection. In this circuit, two MOSFETs are connected in series and the TPD7104AF that drives MOSFET1 is used for Load Short-circuit (Overcurrent) Detection.

Figure 2.1.1 Example of a Load Short-circuit (Overcurrent) Detection circuit and the TPD7104AF internal block diagram

When a load current increases, the TPD7104AF detects a Load Short-circuit (Overcurrent) condition since the IS pin voltage ($V_{IS}$) reaches the threshold voltage ($V_{det}$). At this time, the TPD7104AF acts:

- Disables the OUT output to shut down the load current.
- Turn the DIAG output High to indicate a load short-circuit condition.

The threshold voltage ($V_{det}$) for overcurrent detection is programmable via the $R_{ISref}$ pin. When the $R_{ISref}$ pin is left open, $V_{det}$ is equal to the default $V_{ISOC}$ value (1.02V typical). To set $V_{det}$ to a voltage lower than the default, connect a resistor ($R_{IS}$) between the $R_{ISref}$ and GND pins. In this case, $V_{det}$ is equal to the voltage ($V_{RISref}$) derived from $R_{IS}$ and the internal constant-current source ($I_{ISREF}=38 \mu A$ typical) associated with the $R_{ISref}$ pin. However, $V_{det}$ becomes equal to $V_{ISOC}$ when $V_{RISref}$ exceeds $V_{ISOC}$.
Figure 2.1.2 shows the relationship between $R_{IS}$ and $V_{det}$.

How to set $V_{det}$ with $R_{IS}$:

1. When the $R_{IS\text{ref}}$ pin is open:
   
   $V_{det} = V_{ISOC}$ (1.02V typical)

2. When a resistor ($R_{IS}$) is connected to the $R_{IS\text{ref}}$ pin and $V_{RIS\text{ref}} \leq V_{ISOC}$:
   
   $V_{det} = V_{RIS\text{ref}} = I_{IS\text{REF}} \times R_{IS} = 38\mu A$ (typical) $\times R_{IS}$

3. When a resistor ($R_{IS}$) is connected to the $R_{IS\text{ref}}$ pin and $V_{RIS\text{ref}} > V_{ISOC}$:
   
   $V_{det} = V_{ISOC}$ (1.02V typical)

![Figure 2.1.2 Relationship between $R_{IS}$ and $V_{det}$](image-url)
2.2. Timing chart

Figure 2.2.1 shows a timing chart for Load Short-circuit (Overcurrent) Detection.

![Timing Chart](image)

**Figure 2.2.1 Load Short-circuit (Overcurrent) Detection timing**

Note: Upon detection of a load short-circuit (overcurrent) condition, the output shuts down and remains latched to protect (turn off) the driven power MOSFET. At this time, the diagnostic output, DIAG, is driven High. Setting $V_{IN}$ to a Low level de-latches the output.
3. Power Supply Reverse Connection Protection circuit

3.1. Circuit example

Figure 3.1.1 shows an example of a circuit for Power Supply Reverse Connection Protection. In this circuit, two MOSFETs are connected in series and the TPD7104AF that drives MOSFET2 is used for Power Supply Reverse Connection Protection. Power Supply Reverse Connection Protection is enabled when the SUB pin is left open. Even if a power supply is connected in the reverse direction, MOSFET2 does not turn on because the TPD7104AF does not have power supply and no internal current flow so total system is protected from critical damage. It should be noted, however, that devices closer to the power supply (V_IN) than MOSFET2 (e.g., the Current Sense block in Figure 3.1.1) are not protected so some separate protection circuits are necessary if a system design has any current paths from ground to the power supply.

![Diagram of Power Supply Reverse Connection Protection circuit](image-url)

Figure 3.1.1 Example of a Power Supply Reverse Connection Protection circuit and the TPD7104AF internal block diagram
4. Application circuit example and bill of materials

4.1. Application circuit example

Figure 4.1.1 shows an example of an application circuit for a solid-state relay using two TKR74F04PB N-channel power MOSFET and two TPD7104AF. The use of the low-on-resistance TKR74F04PB (with a $V_{DS}$ of 40V and a maximum $R_{DS(ON)}$ of 0.74mΩ) makes it possible to flow a current up to 40A. Two TPD7104AF, IC1 and IC2, drive separate MOSFETs. IC1 provides Load Short-circuit (Overcurrent) Detection whereas IC2 provides Power Supply Reverse Connection Protection.

![Application circuit example for the TPD7104AF](image)

Figure 4.1.1 Application circuit example for the TPD7104AF
### 4.2. Bill of materials

Table 4.2.1 shows the bill of materials for the application circuit.

<table>
<thead>
<tr>
<th>No.</th>
<th>Ref.</th>
<th>Qty</th>
<th>Value</th>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Description</th>
<th>Packaging</th>
<th>Typical Dimensions mm (inches)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IC1, IC2</td>
<td>2</td>
<td>—</td>
<td>TPD7104AF</td>
<td>TOSHIBA</td>
<td>MOSFET gate driver</td>
<td>PS8</td>
<td>2.9 x 2.8</td>
</tr>
<tr>
<td>2</td>
<td>IC3</td>
<td>1</td>
<td>—</td>
<td>LTC6101BCS5</td>
<td>Analog Devices</td>
<td>Current sense amplifier</td>
<td>TSOT-23</td>
<td>2.9 x 2.8</td>
</tr>
<tr>
<td>3</td>
<td>Q1, Q2</td>
<td>2</td>
<td>—</td>
<td>TKR74F04PB</td>
<td>TOSHIBA</td>
<td>Power MOSFET</td>
<td>TO220-SM(W)</td>
<td>10 x 13</td>
</tr>
<tr>
<td>4</td>
<td>D1, D2, D3, D4</td>
<td>4</td>
<td>—</td>
<td>CRZ16</td>
<td>TOSHIBA</td>
<td>Zener diode</td>
<td>S-FLAT</td>
<td>3.5 x 1.6</td>
</tr>
<tr>
<td>5</td>
<td>D5</td>
<td>1</td>
<td>—</td>
<td>CMG07</td>
<td>TOSHIBA</td>
<td>Diode</td>
<td>M-FLAT</td>
<td>4.7 x 2.4</td>
</tr>
<tr>
<td>6</td>
<td>D6, D7</td>
<td>2</td>
<td>—</td>
<td>CMZ27</td>
<td>TOSHIBA</td>
<td>Zener diode</td>
<td>M-FLAT</td>
<td>4.7 x 2.4</td>
</tr>
<tr>
<td>7</td>
<td>D8, D9, D10</td>
<td>3</td>
<td>—</td>
<td>1SS352</td>
<td>TOSHIBA</td>
<td>Diode</td>
<td>USC</td>
<td>2.5 x 1.25</td>
</tr>
<tr>
<td>8</td>
<td>R1</td>
<td>1</td>
<td>0.5MΩ</td>
<td>PSJ2NTEBL500F/BVS-M-R0005-1.0</td>
<td>KOA Isabellenhutte</td>
<td>10W, ±1% 9W, ±1%</td>
<td></td>
<td>10 x 5.2</td>
</tr>
<tr>
<td>9</td>
<td>R2</td>
<td>1</td>
<td>300Ω</td>
<td></td>
<td></td>
<td>63mW, ±1%</td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>10</td>
<td>R3, R5</td>
<td>2</td>
<td>100kΩ</td>
<td></td>
<td></td>
<td>63mW, ±5%</td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>11</td>
<td>R4</td>
<td>1</td>
<td>10kΩ</td>
<td></td>
<td></td>
<td>63mW, ±1%</td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>12</td>
<td>R6, R7, R8, R9</td>
<td>4</td>
<td>10kΩ</td>
<td></td>
<td></td>
<td>63mW, ±5%</td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>13</td>
<td>R10, R11</td>
<td>2</td>
<td>20kΩ</td>
<td></td>
<td></td>
<td>63mW, ±5%</td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>14</td>
<td>R12</td>
<td>1</td>
<td>1kΩ</td>
<td></td>
<td></td>
<td>63mW, ±5%</td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>15</td>
<td>C1, C2, C3</td>
<td>3</td>
<td>1μF</td>
<td></td>
<td>Ceramic, 25V, ±10%</td>
<td></td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
</tr>
<tr>
<td>16</td>
<td>C4, C5</td>
<td>2</td>
<td>10nF</td>
<td>Ceramic, 50V, ±10%</td>
<td></td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>C6</td>
<td>1</td>
<td>100nF</td>
<td>Ceramic, 50V, ±5%</td>
<td></td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>C7</td>
<td>1</td>
<td>15pF</td>
<td>Ceramic, 50V, ±5%</td>
<td></td>
<td></td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
</tr>
</tbody>
</table>
5. Guidelines for application circuit design

This section provides design guidelines for Load Short-circuit (Overcurrent) Detection and Power Supply Reverse Connection Protection using the 40-A solid-state relay shown in Figure 4.1.1.

5.1. Designing Load Short-circuit (Overcurrent) Detection circuit

In Figure 4.1.1, IC1 (TPD7104AF IPD driver) and IC3 (LTC6101BCS5 current-sense amplifier) provide overcurrent detection. The load current \( I_{det} \) is calculated as follow:

\[
I_{det} = V_{det} \times \frac{R_2}{R_1 \times R_4} \quad (1)
\]

Whereas:
- \( I_{det}(A) \) : Load Current
- \( R_1(\Omega) \) : Current Sense Resistor
- \( R_2(\Omega) \) : Current Sense Amplifier Input Resistor
- \( R_4(\Omega) \) : Current Sense Amplifier Output Resistor

The values of \( V_{det}, R_2, R_1, \) and \( R_4 \) can be determined as follows.

1. Determine the maximum system load current: \( I_{max} \)
   The maximum current to be supplied to a system from its specification. For example, the solid-state relay shown in Figure 4.1.1 is designed to switch 40A, the \( I_{max} \) is 40A.

2. Determine the value of the \( R_1 \)
   To reduce power consumption, select a small-value resistor for \( R_1 \), considering the performance of the current-sense amplifier. For example, if the power system design requires 1W loss, \( R_1 \) should be less than 0.625mΩ so it should be 0.5mΩ in the case. The voltage between the terminals of \( R_1 \) is 20mV at \( I_{max} \). To ensure current-sensing accuracy, this voltage must be sufficiently lower than the input offset voltage of the current-sense amplifier. The temperature drift of the current-sense amplifier should also be considered as necessary. The LTC6101BCS5 has ±0.81mV input offset voltage and ±3μV/°C temperature drift. If the LTC6101BCS5 is exposed to a temperature change of 100°C during operation, then the LTC6101BCS5 has 1.11mV total offset voltage, which translates to a current-sensing error of 2.22A.

3. Determine the value of \( R_2 \) and \( R_4 \)
   A Load Short-circuit (Overcurrent) condition must not be detected at \( I_{max} \) or lower. Therefore, the gain of the current-sense amplifier must satisfy the following equation:

\[
\text{Gain} < \frac{V_{det(min)}}{I_{max} \times R_1} \quad (2)
\]

\[
\text{Gain} = \frac{R_4}{R_2} \quad (3)
\]
Since $V_{\text{det}}(\text{min}) = (V_{\text{ISOC}}(\text{min})) = 0.8V$, the gain must be less than 40 per (2). Taking variations in parts characteristics into consideration, it should be used $300\Omega \pm 1%$ resistor as R2 and $10k\Omega \pm 1%$ resistor as R4 to generate a gain of 33 per (3) in the case.

4. Confirm variations
Using the above parameters to calculate $I_{\text{det}}$ variations in order to ensure that the selected parts meet the design requirements.

Imax must be greater than $I_{\text{det}}(\text{min})$. Per (1) and each values, $I_{\text{det}}(\text{min})$ is:

$$I_{\text{det}}(\text{min}) = 0.80 \times 300 \times 0.99 / (0.5m \times 1.01 \times 10k \times 1.01) - 2.22$$
$$= 44.4A$$

Therefore, $I_{\text{det}}(\text{min})$ has around 10% margin against $I_{\text{max}} (=40A)$. $I_{\text{det}}(\text{min})$ is acceptable even when slight TCR variations of resistors are taken into account.

The maximum ratings of the parts must not be exceeded at $I_{\text{det}}(\text{max})$. Per (1) and each values, $I_{\text{det}}(\text{max})$ is:

$$I_{\text{det}}(\text{max}) = 1.2 \times 300 \times 1.01 / (0.5m \times 0.99 \times 10k \times 0.99) + 2.22$$
$$= 76.4A$$

At this time, the current-sense resistor (R1) has a power loss of 2.9W. Therefore, R1 has enough margin relative to its rated power of 5W (at a pin temperature of 100°C).

Calculate $I_{\text{det}}(\text{typical})$, Per (1) and each values, $I_{\text{det}}(\text{typical})$ is:

$$I_{\text{det}}(\text{typical}) = 1.02 \times 300 / (10k \times 0.5m)$$
$$= 61.2A$$

5.2. Designing Power Supply Reverse Connection Protection circuit

In Figure 4.1.1, IC2 (TPD7104AF) provides Power Supply Reverse Connection Protection. Its Power Supply Reverse Connection Protection function is enabled when the SUB pin is left open. For more detail, see 3.1 description.
6. Simulation

6.1. Function of Load Short-circuit (Overcurrent) Detection

This section shows the simulation result of the Load Short-circuit (Overcurrent) Detection function available with the TPD7104AF. Figure 6.1.1 shows the circuit simulated using OrCAD. It is similar to the circuit of Figure 4.1.1, but uses the ideal op amp available with OrCAD for current sensing. The circuit shown in Figure 6.1.1 is available for download at RD016-SPICE-02.

We performed a simulation as follows:

- **Conditions**
  - VIN: 12V
  - VCC5: 5V
  - IN1, IN2: 0V
  - Load switch (U14): Off (The load current, Iout, is off.)

- **Procedure**
  - Simulation starts (at \( t = 0 \)).
  - At \( t = 0.5 \)ms, IN1 is set to the High level. (Q1 turns on.)
  - At \( t = 0.6 \)ms, IN2 is set to the High level. (Q2 turns on.)
  - At \( t = 2 \)ms, the load switch (U14) is turned on. (The short-circuit current turns on.)

![Simulation Circuit for Load Short-circuit (Overcurrent) Detection](image-url)
Figure 6.1.2 shows the simulation results. When the load switch turns on, a short-circuit current flows. Upon detection of an overcurrent, the TPD7104AF:

- Turns off Q1 to cut off the load current;
- Drives the DIAG1 signal High to indicate an overcurrent condition.
Figure 6.1.2 Simulation result for Load Short-circuit (Overcurrent) Detection

1. IN1 and IN2 goes High.

2. The control signals of IC1 and IC2 goes High.

2. Q1 and Q2 turn on.

3. The 12V output turns on.

4. The load switch turns on. As a result, the load current increases (to roughly 62 A).

5. As the load current increases, the IS pin voltage increases.

6. The IS voltage reaches the threshold (1.02V). As a result, a load short-circuit condition is detected.

7. The control signal of IC1 goes Low.

7. Q1 turns off.

8. The 12V output turns off.

8. The load switch turns off.

7. The DIAG1 signal is driven High.

2. The DIAG1 and DIAG2 signals are driven Low.
6.2. Function of Power Supply Reverse Connection Protection

This section shows the simulation result of Power Supply Reverse Connection Protection function with the TPD7104AF. Figure 6.2.1 shows the circuit simulated using OrCAD.

In case a power supply is connected to VIN in the reverse direction, IC2 and Q2 provide Power Supply Reverse Connection Protection. The circuit shown in Figure 6.2.1 is available for download at RD016-SPICE-02.

- Conditions
  - VIN: -12V (reverse direction)
  - VCC5, IN1, IN2: 0V
  - The SUS pin is left open to enable Power Supply Reverse Connection Protection.

- Procedure
  - Simulation is started, with Power Supply Reverse Connection Protection enabled.

Figure 6.2.1 Simulation Circuit for Power Supply Reverse Connection Protection

Figure 6.2.2 shows the simulation results. VIN-GND is in reverse polarity (= -12V). Since Power Supply Reverse Connection Protection is enabled, no load current flows for a period of 5ms after the simulation starts.
Figure 6.2.2 Simulation result for Power Supply Reverse Connection Protection

1. Vout is 0V.

1. To simulate a reverse supply connection, -12V is applied to VIN.

1. No load current flows.
7. Product overview
7.1. TPD7104AF
7.1.1. Overview
The TPD7104AF is a single-output N-channel power MOSFET gate driver for high-side switch applications. With a charge pump circuit, the TPD7104AF simplifies a load switch design for high-current applications.

- Integrated a charge pump circuit
- Provides Load Short-circuit (Overcurrent) Detection and Power Supply Reverse Connection Protection
- Small package (PS-8)

7.1.2. External view and pin assignment

![Pin Assignment (top view)](image)

Figure 7.1.2.1 External view and pin assignment
7.1.3. Internal block diagram

![Internal block diagram of TPD7104AF]

7.1.4. Pin description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Power supply pin.</td>
</tr>
<tr>
<td>2</td>
<td>IS</td>
<td>Detection pin for short circuit. If short circuit detection is not used, IS pin connect to GND.</td>
</tr>
<tr>
<td>3</td>
<td>OUT</td>
<td>Output pin for an external MOSFET drive. State is off if detect short circuit.</td>
</tr>
<tr>
<td>4</td>
<td>SUB</td>
<td>Please use open if use protection for reverse connection of power supply. If protection for reverse connection of power supply is not used, SUB pin connect to GND.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>6</td>
<td>IN</td>
<td>Input pin. IN has a pull-down resistor.</td>
</tr>
<tr>
<td>7</td>
<td>DIAG</td>
<td>Diagnosis detection pin. It is open drain composition. Output is inverted if detect short circuit.</td>
</tr>
<tr>
<td>8</td>
<td>R1Sref</td>
<td>Adjust pin for sense level for short circuit detection. If R1Sref is not used, R1Sref pin is open.</td>
</tr>
</tbody>
</table>
7.2. TKR74F04PB

7.2.1. Overview

The TKR74F04PB is Toshiba’s low-on-resistance, high-current MOSFET fabricated using the latest low-voltage U-MOSIX-H process.

- Low drain-source on-resistance: $R_{DS(ON)} = 0.6 \text{m} \Omega$ typical ($@V_{GS}=10 \text{V}$)
- Maximum drain current: $I_D = 250 \text{A (DC)}$
- Maximum drain-source voltage: $V_{DSS} = 40 \text{V}$

7.2.2. External view and pin assignment

![External View and Pin Assignment Diagram]

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