DK8_HC11
USER MANUAL

DK68HC11-52J-110/220 Development Board

CONTENTS

■ (Please see next page)

Thank you for purchasing the ST Development Board, the most complete kit of it's type on the market today.

Concept

The ST Development Board provides the following capabilities;

- Demonstrate design concepts early, optimizing "time to market"
- Jump start user application with proven framework (hardware and software)
- Substitute for user target design until target prototypes are available
- Specific PSD evaluation or migration from one family to another
- Evaluate compiler vendors

These features combine with the following to provide faster "time to market" for user applications.

- Embedded monitor
- Bundled compiler from major vendor, limited version
- Windows serial command interface for code download
- Flash reprogrammability via JTAG (PSD813F family only).
  Requires FLASHLink (included).

The Development board is offered in the following configurations.

- **Development Kit, DK68HC11-52J-xx0**. This includes the Development Board described below as well as FLASHlink and PSDsoft. The xx denotes 120 VAC(11) or 220VAC(22).

- **Development Board, DVB68HC11-xx0.** This includes the mother board only described within this manual, UART cable, Power supply, The xx denotes 120 VAC(11) or 220VAC(22). Requires daughter board, PSDsoft, and programmer).

- **Daughter Board, WS6200.** This includes the daughter board only for PSD8xxF.

Overview

Each ST Development Kit consists of the following:

- Mother board (EVM_xxx)
- Daughter board (EVD_xxx)
- Uart cable(straight through DB9M to DB9F)
- Class 2 transformer (120vac)
- Software:
  Two executable programs(F1_ee.obj and demo1.obj)
  Windows download software, PSDload (for PSD813F only)
  PSDSoft (development tool)
- Compiler package

The major components are described in the sections below.

Mother board/daughter board

The Development Board is physically packaged in a mother/daughter board arrangement. The mother board is specific to the microcontroller. The daughter board is specific to the PSD. The intent of the packaging scheme is that any daughter board can be interchanged with any mother board. This packaging philosophy allows migration in either the microcontroller and/or the PSD areas.

Core executable software programs

Several programs are bundled with the development board and are described below. The C level source code is included with the board as well as all functions and components (such as flash and EEPROM routines) allowing easy incorporation into user applications.

- F1_ee
  This is a hardware test of the assembly. Each test is annunciated with the display, and a final results code is displayed at the end of the test. See Appendix D and source code for details. The C level source code for this is on the CD under "Coded Examples".
- Demo1
  This code displays a message and exercises the PSD logic microcells.

The functionality of these programs is consistent across all Development Boards even though their specific implementation within any board may vary.

PSDload

This win95/NT compatible application for the PC allows the microcontroller executable software to be downloaded via the UART channel. The download destination can be either in flash (all PSD813 devices) or EEPROM (for PSD813F1 only) but not the PLD.

New executable code can be downloaded to the Development board two different ways; via the UART or via JTAG. The UART avenue (9 pin DSUB on the mother board) allows only data and executable code to be downloaded to the flash and/or EEPROM on the PSD over the PC serial link. The JTAG programming avenue (2x7 connector on daughter board) allows the PLD within the PSD to be downloaded in addition to the contents of flash and/or EEPROM. JTAG download requires the FLASHlink cable and a PC parallel port connection.

Compiler and Debugger

ST has partnered with a different compiler vendor for each microcontroller. These vendors supply a demo version of their products, tailored to the ST Development Board environment. Together, this constitutes a complete development system including code development as well as evaluation of ST's PSD components.

The compiler package is comprised of the following:

Compiler
Assembler
Linker
Debugger (via uart)

See specific compiler documentation for details.

The list of present partners:

8031 family

Keil Software
16990 Dallas Parkway, Suite 120
Dallas, TX 75248
1-800-348-8051
www.keil.com

HC11 family

COSMIC Software Inc.
400 West Cummings Park STE 6000
Woburn, MA 01801-6512
1-781-932-2556
www.cosmic-software.com

Detailed Descriptions

Mother board

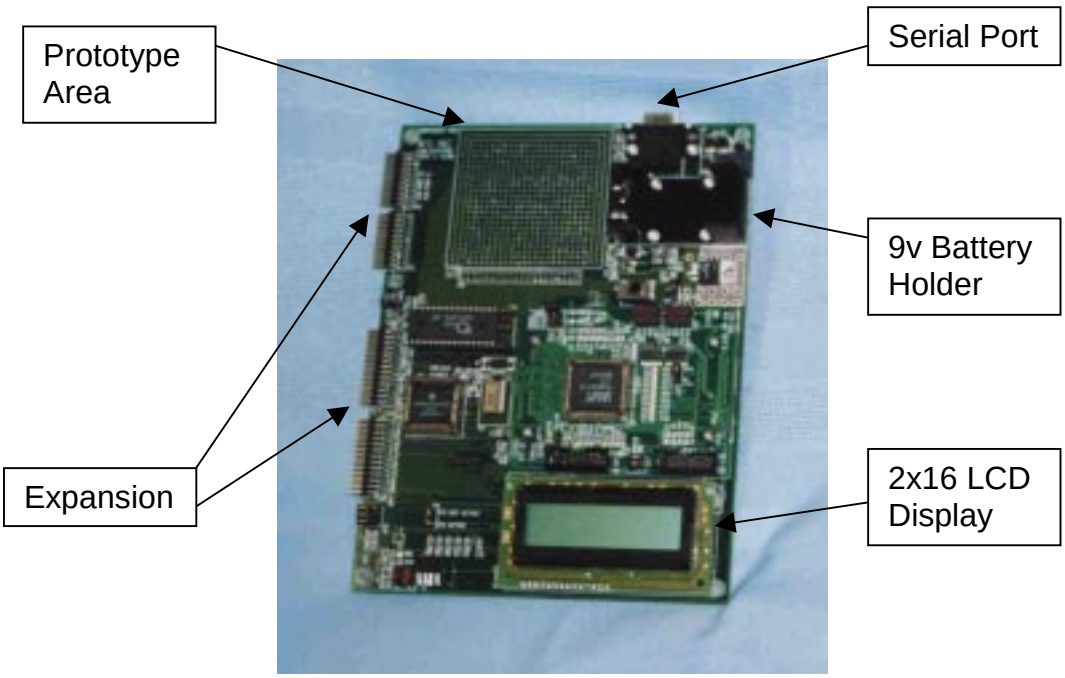


Figure 1 Development Board

Above is depicted the functional mother and daughter board assembly. An assembly drawing appears in Appendix A which highlights the location of the major components.

Please refer to appendix A for the following descriptions:

Prototype area

Each mother board contains a prototyping area (2.4" x 2.5") with plated thru holes on 0.1 inch centers. The prototyping area is bounded by Vcc and ground on three sides and with general signals (address/data bus and control signals) on the fourth side.

Expansion

In cases where the above prototype area is inadequate, provision has been made for off board expansion via right angle 0.025 square posts. Four connectors have been provided with the critical signals routed to the first two. This allows another circuit card to be attached to the Development Board.

Display

A two line by 16 character LCD display is included on the Development Board.

Power Supply description and options

Several sources of power can be used with the development board.

1. 9v battery holder is included on the mother board for portable applications.
2. A standard 120vac class 2 transformer is provided. T
   The equivalent 240vac transfomer is Digikey DPD090050E-P-5.
3. External supply

The external supply capability is included for two reasons;

a. demonstration of the JTAG chaining capability with multiple PSD's
b. provide headroom for user expansion.

The battery and transformer can be connected simultaneously due to the diode isolation included on the board. In this case, the higher of the two voltages will power the board and reverse bias the diode in series with the other source.

In the case of an external supply, such as used for JTAG chaining, operational power for the regulated 5v is supplied with a single board via the JTAG cable itself and then propagated to downstream devices.

Regulated power is supplied via a 0.5 amp TO-220 regulator. While heat sinking has been provided via copper on the board itself, clearance has been left on the mother board for a conventional heatsink. Typical thermal rise with one development board results in less than 2°C on this regulator showing the guardband associated with the implementation.

Jumper Functions (see appendix A)

The following list details the controllable functions of the assembly.

The specific position to control each function is shown on the board legend screen and in Appendix A as well as the locations of each jumper assembly.

Mother board (EVM, see Appendix A)

JP1	CSI active/ not active
JP4	Power supply (internal/external)

Daughter Board(EVD, see Appendix A)

JP1	Current measuring
JP2	JTAG /no JTAG (clock connection)
JP3	chain/no chain (JTAG Programming)

Reset

A manual reset button is provided to pulse the microcontroller reset line via a supervisory chip. This button is in parallel with the JTAG RST line so that the same function can occur either locally or remotely via the FLASHlink.

UART

A standard 8 bit asynchronous channel is provided.

Daughter board

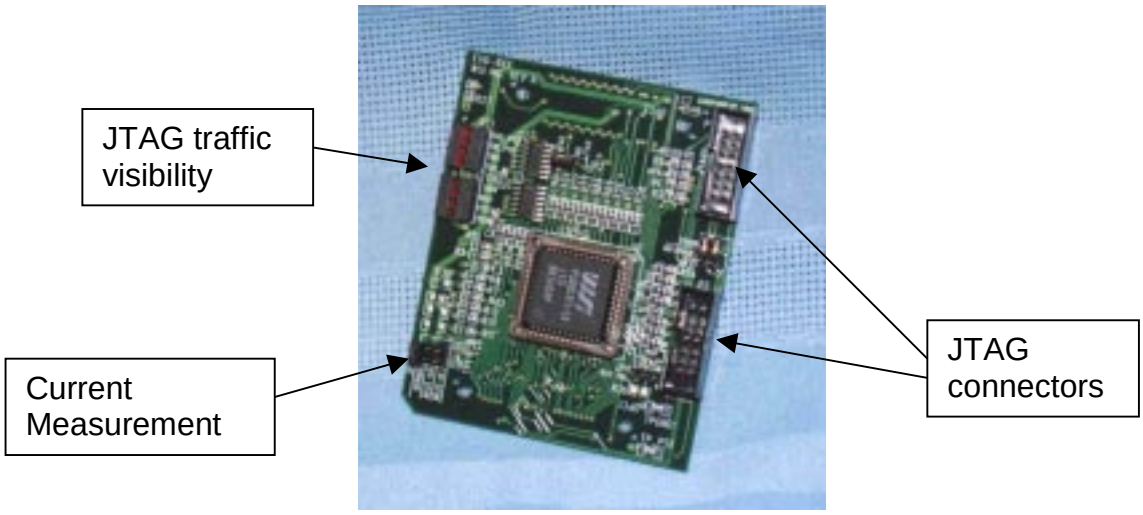


Figure 2 Daughter Board

A detailed drawing of this assembly is shown in the Appendix A (in final configuration).

Current Measuring Capability

JP1 provides the ability to measure PSD current consumption by placing a resistor in series with the PSD. The current consumption may be calculated by measuring the resistive voltage drop across this resistor. Lines for the measurement are routed from the daughter board (JP1, daughter board) through the OPC connector to the mother board near the prototype area for convenience. One method to exploit this alternative could be to add an a/d converter and processing circuitry to implement analog functions. An a/d converter is not included in the development package.

Three jumper positions are provided as listed below;

a. Normal. PSD supply is connected to Vcc power plane directly.
b. Measure ma. This position places a 10 ohm resistor in series with the PSD.
c. Measure ua. This position places a 1000 ohm resistor in series with the PSD. It is intended to allow the measurement of alternate power modes within the PSD.

Note: Based on the product term usage and subsequent current consumption on your design, the values may need to be modified such that the voltage drop remains within the PSD Vcc specification for proper operation.

JTAG

The PSD813F JTAG interface provides the capability of programming all memory within the PSD (PLD, configuration, flash and boot areas). This interface can also be used to program a completely blank component as JTAG enabled is the default PSD state. The vehicle for this programming is the IEEE 1149.1 JTAG standard. See Application Note 54 (AN054) for further description on our CD or website at www.st.com/psm.

The JTAG traffic can be observed during download via board mounted LEDs.

ST provides a FLASHlink cable to facilitate this JTAG programming operation. The FLASHlink cable connects the PC parallel port to the JTAG connector (JTAGIN or JTAG1) and is driven by PSDsoft(PSD development tool).

The required jumper settings on the daughter board are listed in the following table.

Jumper settings	
	set to
JP2	JTAG
JP3	no chain

Table 1 Jumper settings JTAG (for single device)

JTAG Chaining

Using the JTAG interface, multiple devices can be interconnected such that programming can occur on all devices. This interconnection is termed “chaining” and is discussed further in the Application Note 54 (AN054). During this operation, data is clocked serially into each device in the chain. Appendix C of this document shows a schematic of the data propagation path for chaining several PSDs using Development Board hardware.

With boards configured in chaining mode, only one board needs to be powered by a battery of transformer. All other boards derive power from this single source since the Vcc on all boards are tied together through the interconnecting JTAG cable. The downstream boards should move JP4 on the mother board to the external position so that the downstream regulators are not involved.

Jumper settings	
	set to
JP2	JTAG
JP3	chain

Table 2 Jumper settings JTAG (for multiple device)

Software Functional Description (F1_ee.obj)

This software is primarily intended to test the Development Board hardware. However, as a consequence of this validation, many of the unique features of the PSD are also demonstrated. Thus, it serves both purposes conveniently. The software is included for these reasons and to provide examples of possible design solutions.

Following is a list of the tests that are performed. Further descriptive information is included following the list. Additionally, the C level source code is provided on CD as further reference.

Software operational sequence for F1_ee.obj

- LCD test
- Announce execution source (from fixed source)
- LED test, Mother board
- LED test, Daughter board (PSD Port C)
- Page Register test
- PSD SRAM test (0x55, 0xAA, 0xFF, 0x00)
- External SRAM test (0x55, 0xAA, 0xFF, 0x00, walking pattern)
- Code copy tests
- EEPROM to FLASH
- EEPROM to SRAM
- UART test
- Display results code (see Appendix D)

Code Copy Tests

These operations are a prelude to memory swapping operations that are described later.

The functional boot code is copied from its original location in EEPROM into FLASH and external SRAM. Subsequent resets of the Development Board result in the execution of the code at these alternate locations based on the position of the dip switches.

To ensure the execution occurs from the desired location, a message is displayed at power up. The executing code knows to display the message from a fixed location without knowledge of what the specific message is. For example, upon initial boot from EEPROM, the message says "Execution Source, EEPROM". In this case, the message is hard coded into the EEPROM.

When the code is copied to the alternate location in FLASH (for example), the message in the destination memory fixed location is also updated to show the new execution source. When boot occurs from this new source, the copied message is displayed saying "Execution Source, FLASH" Similar operation occurs for external SRAM execution.

UART Test

At the time of this writing the final UART software is not complete. This simple hardware test was implemented to show functionality.

Send a "0" from terminal, Development Board responds with "1"

Baud rate is fixed at 19.2 Kbaud and 8N1.

Memory swapping tutorial (F1_ee.obj)

The code copy test is one method to demonstrate the memory swapping capabilities of the PSD. An alternative memory swapping demonstration could be to download a second executable into the desired location using the UART or JTAG(FLASHlink). This program demo1.obj is supplied for this purpose.

A consolidated graphical depiction of the memory map during these operations is shown in Appendix E for F1_ee.obj and duplicated below for convenience

The base memory map for F1_ee.obj and demo1.obj is shown below. The boot code is located in the EEPROM (ees0,ees1). The EEPROM is located in high memory in order to encompass the interrupt and reset vectors.

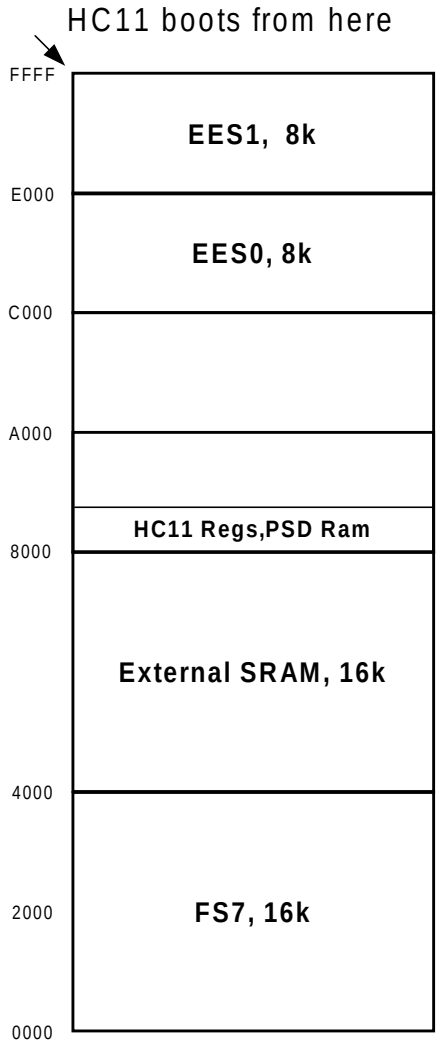


Figure 3 Memory map for F1_ee.obj

At initial boot from a newly programmed PSD, the external SRAM and FLASH areas are blank as shown in Figure 4 on the left (unshaded areas). After the F1_ee.obj code runs the first time, both external SRAM and FLASH have been populated with a copy of the boot code(using the EEPROM as a source). The copy is identical to the code in EEPROM except that the message area has been updated to reflect the destination of the copy operation as shown in Figure 4 below on the left.

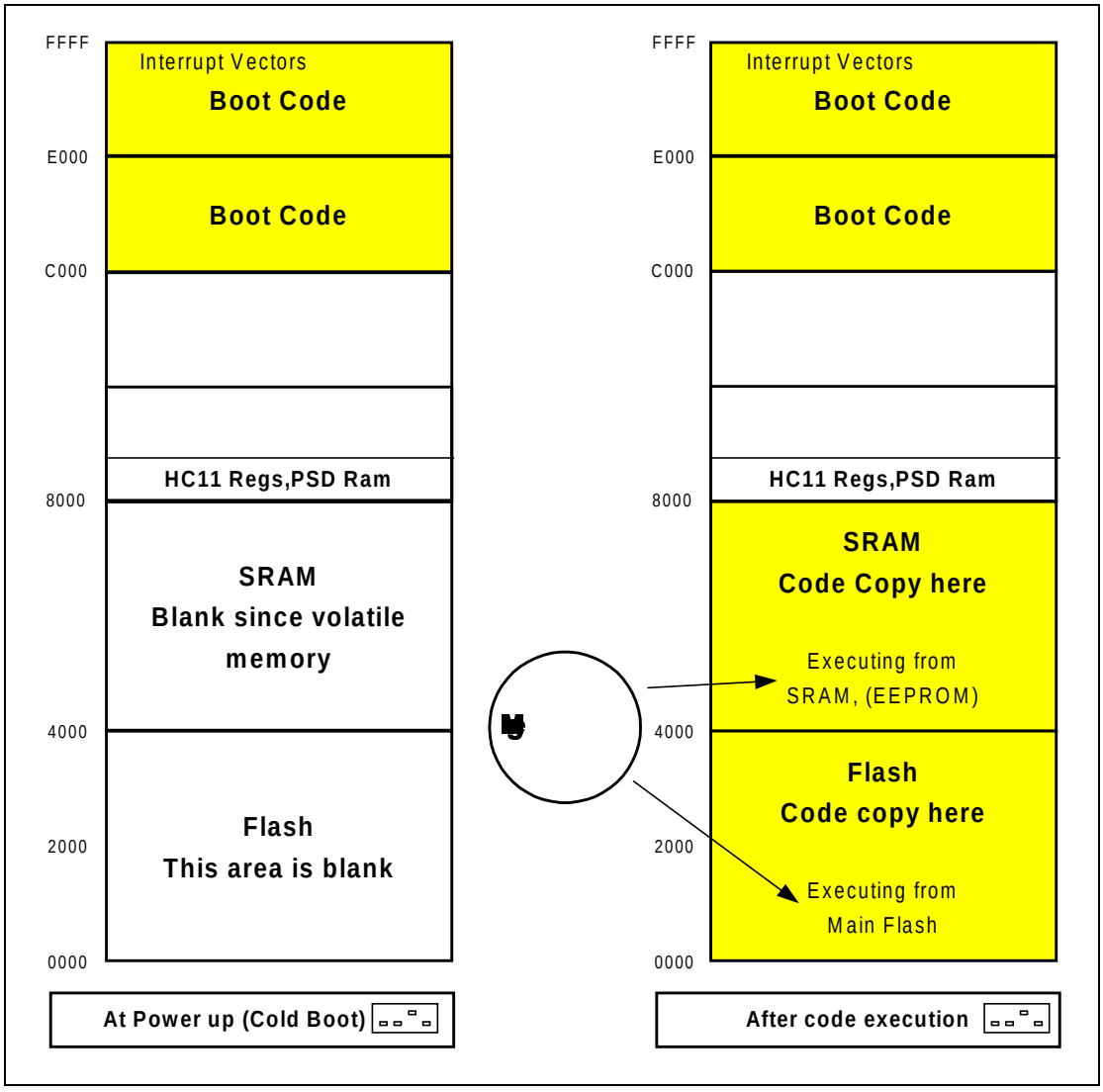


Figure 4 Memory map before and after execution

In this case, execution is set to occur from EEPROM as noted in the above figure by the dip switch graphic . The two left switches denote that the execution occurs from the EEPROM (es0 and es1, down = 0). This boot action occurs due to the PLD equations listed below and the fact that the PAGE register is 0 at power up. These equations are from the PSD *.abl file.

```
ees1 = ((address >= ^hE000) & (address <= ^hFFFF) & (page == X) &  es0 &  es1 );
ees0 = ((address >= ^hC000) & (address <= ^hDFFF) & (page == X) &  es0 &  es1 );
```

Now, lets execute from FLASH. Change the dip switch to  in order to execute from FLASH. Push the reset button and be quick to observe the execution source message. Now we're executing from FLASH. The memory map is shown on the left in the following Figure 5.

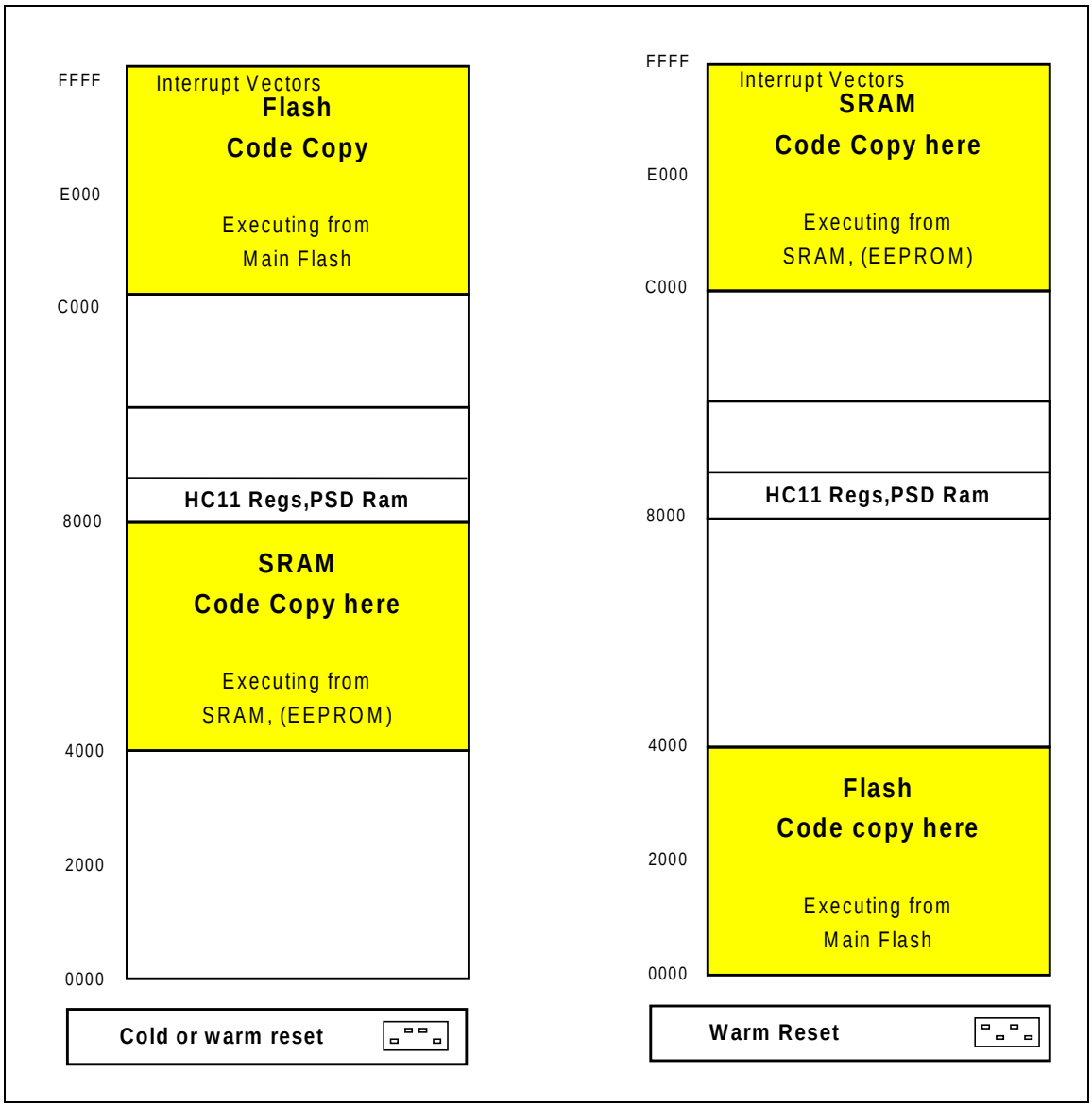


Figure 5 Memory Swapping using F1_ee.obj

Again this occurs due to the PLD equation listed below for the FLASH segment (FS7).

```
fs7 = ((address >= ^hC000) & (address <= ^hFFFF) & (page == X) & es0 &  es1  )
      # ((address >= ^h0000) & (address <= ^h3FFF) & (page == X)  );
```

Note that normally FS7 resides from 0x0 to 0x3FFF (Figure 4) until we change the dip switch. At reboot, the dip switch is read and written into the PAGE register. If the positions are es0=1 and es1=0, FS7 now appears from 0xC000 to 0xFFFF and the MCU never knows the difference

Similar operation occurs with the dip switch in the SRAM position  . Again, it's due to the PLD equation for the external SRAM noted below.

```
cs_ram_ =  ((address >= ^hC000) & (address <= ^hFFFF) & (page == X) &  es0 & es1 )
           # ((address >= ^h4000) & (address <= ^h7FFF) & (page == X) );
```

Give this one a try and observe the message

What really happens

At power up, the PAGE register is 0 due to PSD initialization. This means that execution always starts out in the EEPROM (es0 = es1 = 0) regardless of the source selection on the dip switch.

After a few initialization issues are handled by the first few EEPROM instructions, the dip switches are read and, after some shifting, written into the PAGE register. The location must coincide with the position of es0 and es1 as defined in the f1_ee.abl file used by PSDsoft. Once these locations are written, the very next instruction fetch occurs from the new location.

References

IEEE Std 1149.1-1990 IEEE Test Access Port and Boundary Scan Architecture
PSDSoft User Manual
Flashlink User Manual

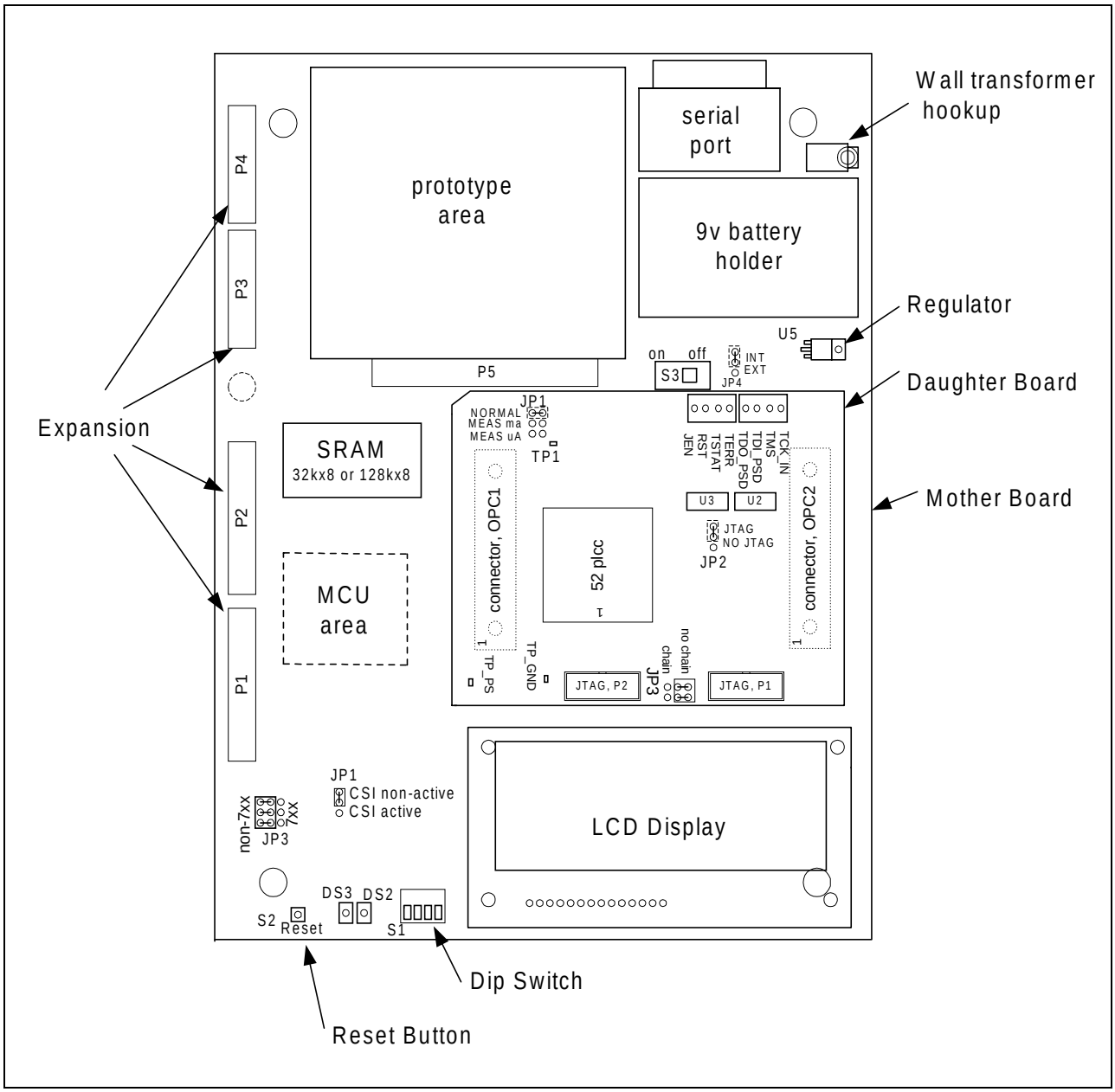
Application notes

AN054 JTAG Information
AN055 GPLD Primer
AN057 Design Tutorial for PSD813F/8031

APPENDIX

Appendix A

Assembly drawing



Appendix B

Parts lists

EVD-8XX			Daughter Board	5/26/98 tmw	rev J
REF.	**QTY**	**GENERIC**			
DES.	**PER**	**P/N**	**DESCRIPTION**	**VENDOR**	**P/N**
	1	pcbevd0001	pc board, EVD_8xx		
	1	soc101-0052	plcc socket, 52 pin for u1	robinson nugent	plcce-052-s1-tt
u1	1	upsd0001	psd		
sc1-4	4	scr256-0375	2-56 screws, 0.375" long phillips head (daughter bd to opc)	RB &W Bosco	
lw1-4	4	lw256-0001	2-56 split lock washer for above screws		
u2,u3	2	ugen0001	led drivers	motorola	74vhc14d (soic)
ds1,ds2	2	led101-0002	led bank (4) with integral resistors	dialight	555-5003
jp2, jp4	2	con225-1003	3 position header	samtec	tsw-103-23-L-s-LL
j1,j2, j4	3	con225-1002	jumper	samtec	snt-100-bk-g
jp1, jp3	2	con225-2003	2x3 025sq post header	samtec	tsw-103-23-L-D-LL
j3	1	con225-2002	2x2 jumper	samtec	mnt-102-bk-g
tp_ps,tp_gnd,tp1	3	tp101-0001	test points	koa	rcw
p1,p2	2	con104-2007	jtag connectors	samtec	tst-107-01-L-D-LL
c1	1	cap1206-1004	cap, 1uf cer, 1206	AVX	1206zc105mat2a
c2,c6, c7, c8, c9	5	cap0603-1003	0.1 cap, smt, cer	panasonic	ecu-e1c103kbq
c3-5	3	cap0603-1002	0.01 cap, smt, cer	panasonic	ecu-e1c102kbq
r1-r5	8	res0805-1002	resistor, smt, 10k, 1/8 watt, 0805	samsung	rm10f1002ct
r6-33	29	res0805-1003	resistor, smt, 100k, 1%, 0805	samsung	rm10f1003ct
r34	1	res0805-1009	resistor, smt, 10	dale	crcw-1205100F
r35	1	res0805-1001	resistor, smt, 1.0 k	dale	tnpw-0805102F
cab1	1		idc cable	samtec	HCSD-07-D-12.00-01-N-G

			Mother Board	5/26/98 tmw	rev I
EVM-HC11					
	QTY	**GENERIC**			
ref des, hc11	**PER**	**P/N**	**DESCRIPTION**	**VENDOR**	**PART NUMBER**
	1	pcbevm0001	pc board, mother		
opc1, opc2	2	con101-2025	connectors	samtec	opc-125-G-D-N-A
f1,f2, f3, f4	4	fas256-0001	broaching fasteners(for opc, 2-56)	pem	kf2-256-et
f5	1	fas440-0001	broaching fasteners(for u5 regulator, 4-40)	pem	kf2-440-et
	1	scr440-0375	screws for u5 (440 x 0.375 with phillips head)		
p1, p2	2	con125-2013	13x2 pin, rt angle 0.025 sq post connector	samtec	tsw-113-08-L-D-LA
p3,p4	2	con125-2010	10x2 pin, rt angle 0.025 sq post connector	samtec	tsw-110-08-L-D-LA
con1	1	con102-0001	9v battery holder	keystone	1294-ND
	6	riv101-0281	rivet	rivet king	c-1 (std tubular rivet)
ds1	1	dis101-0001	display	hantronix	hdm16216h-b
	2	std101-0250	standoffs for display, 0.250	richco	dlcbsat-4-01
	2	std101-0125	standoffs for daughter board	richco	srs4-2-01
	1	con225-1014	14 pin single in line connector/spacer (display)	samtec	dw-14-17-T-S-250-LL
	6	std102-0250	standoffs for board	richco	SRS4-5-01
	6		screws for above standoffs	RB &W Bosco	#4-40, 0.25", pan head
tp_ps,tp_gnd,tp_lir	3	tp101-0001	test points	koa	rcw
	1	soc101-0044	plcc socket, 44 pin	robinson nugent	plcce-044-s1-tt
j3	1	con232-0001	rt angle rs232 connector(female, 9 pin)	amp	745988-4
s1	1	swdip0004	4 position dip switch,side actuated	cts	195-4mst
ds2,3	2	led101-0001	led with integral resistors	dialight	555-3003
y1	1	y101-0001	crystal, 9.8304MHZ	valpey-fisher	vfsmc-316pf9.804
u1	1	umcu0001	MCU	motorola	68hc11ed0cfn3
u2	1	usup0001	max6315, supervisory	maxim, 5v	max6315us44d2-t
u3	1	uram0001	sram, 32kx8, DIP		
			32KX8, 0.6 in PDIP, 5V	mosel	v62c518256L-70P
			32KX8, 0.6 in PDIP, 3V	mosel	v62c318256L-70P

			32kx8, 0.6 in plastic DIP	hitachi	hm62256BLP-7
			32kx8, 0.3 in plastic DIP	hitachi	hm62256BLSP-7
			32KX8, 0.6 in PDIP, 5V	toshiba	tc55257DPL-70L
			32kx8, 0.3 in plastic DIP, 5v	cypress	cy7c199-35PC
			32KX8, 0.6 in PDIP, 5V	issi	is62256-70w
			32KX8, 0.3 in PDIP, 3V	issi	is62LV256-70n
			128KX8, 0.6 in PDIP, 5V	mosel	v62c5181024L-70P
			128KX8, 0.6 in PDIP, 5V	hitachi	hm628128BLP-7
			128KX8, 0.6 in PDIP, 5V	issi	is62c1024L-70W
	3	rec101-1016	single row socket for sram	samtec	SL-116-T-30
u5	1	ureg-0001	regulator	micrel	mic5237-5.0bt
u4	1	u232-0001	232 driver	analog devices	adm202jrn
s2	1	sw102-0001	reset switch, momentary	bourns	7914g
d1-4, d7	5	cr101-0001	diode		s1ab
d5	1	vr101-0001	zener diode, 15v	motorola	mmsz5254bt1
d6	1	cr101-0002	signal diode	national	fdLL4148
t1	1	tr101-0001	class 2 transformer, 500ma,female	cui stack	dpd090050-p-5
con2	1	con103-0001	connector for ps, male	digikey	pj-202a
c8,c9	2	cap0603-2209	22 pf caps, cer	murata	grm39c0g22050ad
c15	1	cap1206-1004	cap, 1uf tant	murata	grm42-6y5v105z016ad
c1,c11,c13,c17	4	cap1206-1004	cap, 1uf cer, 1206	AVX	1206zc105mat2a
c2-7,c12,c14,c16,c18,c19	11	cap0603-1003	0.1 cap, smt, cer	murata	grm39z5u104z016ad
c20-22	3	cap0603-1002	0.01 cap, smt, cer	murata	grm39z5u103z016ad
c10	1	cap0603-1000	cap, 100pf,smt	murata	grm39cog101j050al
r1,r2,r10,r11,r17	5	res0805-4701	resistor, smt, 4.7k, 1/8 watt, 0805	samsung	rm10j472ct
r3,r5-r9,r12,r18	8	res0805-1002	resistor, smt, 10k, 1/8 watt, 0805	samsung	rm10f1002ct
r4	1	res0805-5600	resistor, smt, 560, 1/8 watt, 0805	samsung	
r19, r21,r22	3	res0805-1003	resistor, smt, 100k, 1%, 0805	samsung	rm10f1003ct
r13-15, r23	4	res0805-1000	resistor, smt, 100, 1/8 watt	samsung	rm12j101ct

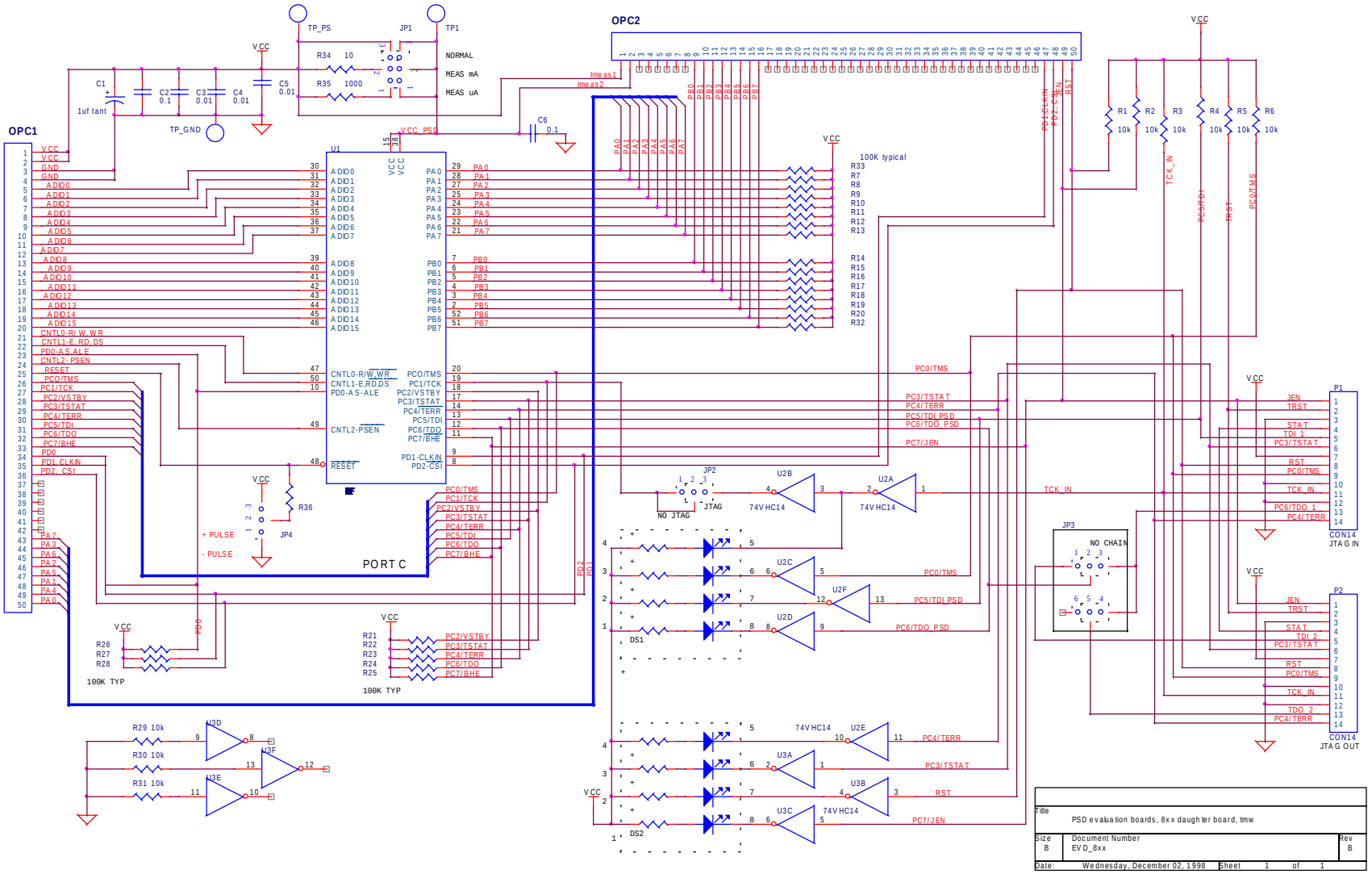
r16	1	res0805-1005	resistor, smt, 10M, 1/8 watt, 0805	samsung	rm10j106ct
jp1,jp2,jp4, jp5	4	con225-1003	3 position header	samtec	tsw-103-23-L-s-LL
j1,j2,j4,j5	4	rec225-1002	shunt (use with jpx above)	samtec	snt-100-bk-g
s3	1	sw101-0002	on-off switch	c&k	1101-m2-s3-v3-B
jp3	1	con225-3003	post 3x3	samtec	tsw-103-23-L-T-LL
j3	1	rec225-3002	triple shunt (use with jp3)	samtec	mnt-103-bk-g

Appendix C

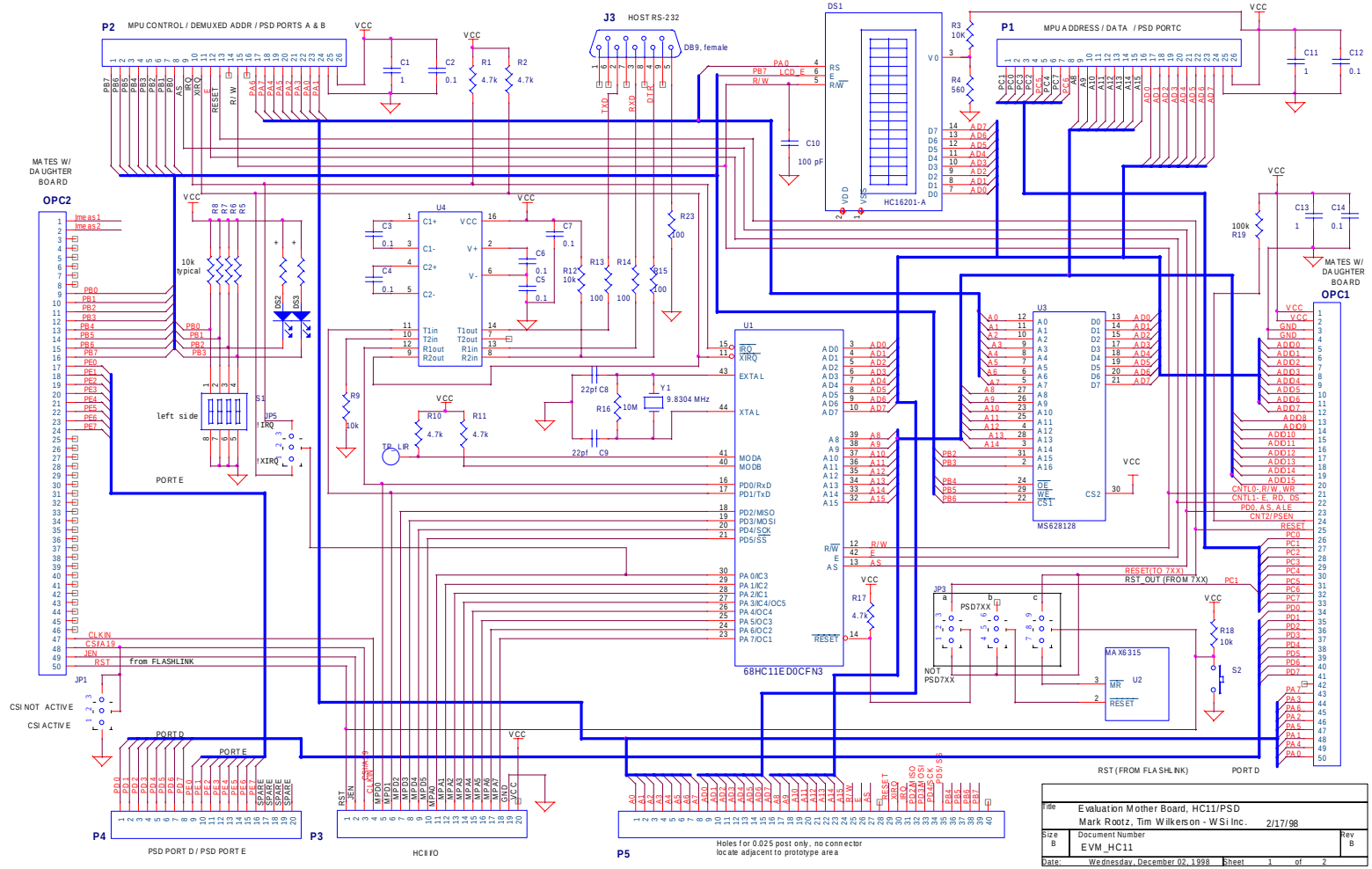
Schematics

Following are the schematics of the mother and daughter boards.

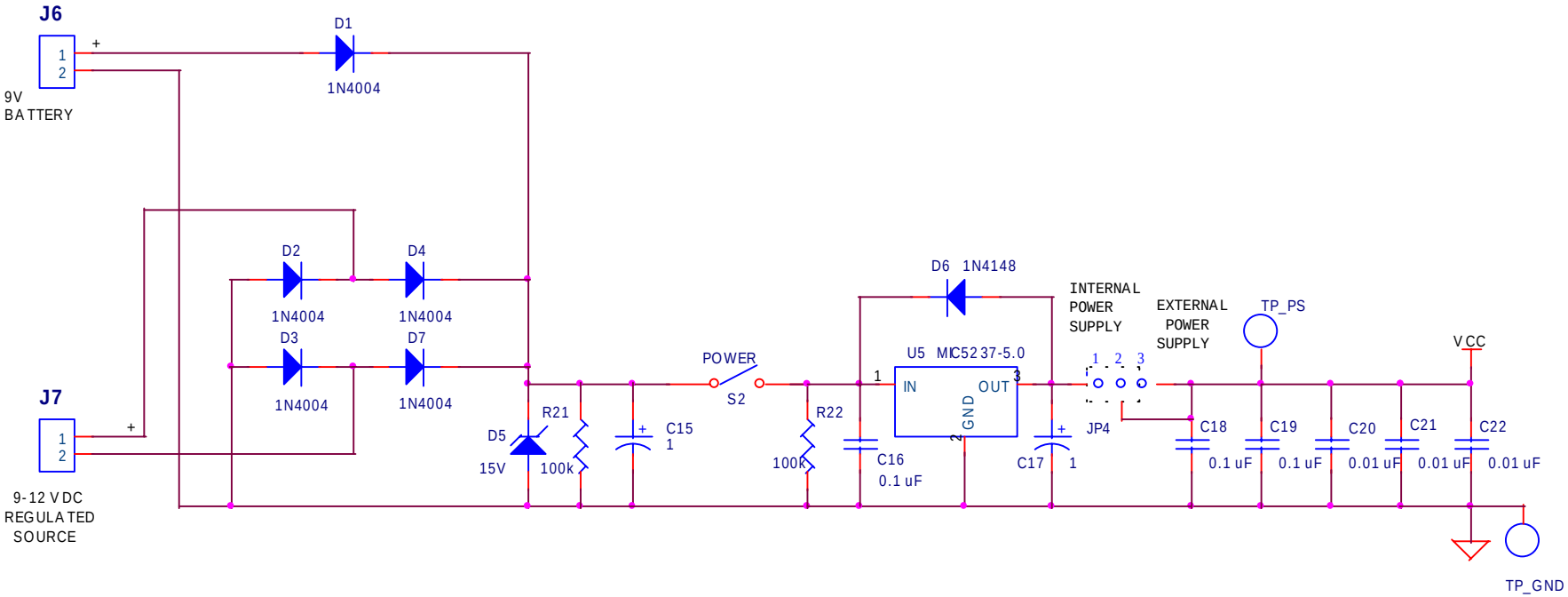
Daughter Board, EVD_8xx
Mother Board, EVM_HC11, part a
Mother Board, EVM_HC11, part b
JTAG chaining using Development Board hardware


OPC1
OPC2
U1
TP_PS
TP1
JP1
NORMAL
MEAS mA
MEAS uA
TP_GND
VCC_PSD
C1
1uf tant
C2 0.1
C3 0.01
C4 0.01
C5 0.01
C6 0.1
R34 10
R35 1000
PORT C
+ PULSE
- PULSE
JP4
R36
JP2
JTAG
NO JTAG
74V HC14
U2A
U2B
U2C
U2D
U2E
U2F
U3A
U3B
U3C
U3D
U3E
U3F
DS1
DS2
JP3
NO CHAIN
P1
P2
CON14
JTAG IN
JTAG OUT
100K typical
100K TYP
TCK_IN
Title
PSD evaluation boards, 8xx daughter board, tmw
Size B
Document Number EVD_8xx
Rev B
Date: Wednesday, December 02, 1998
Sheet 1 of 1

EVD_8xx

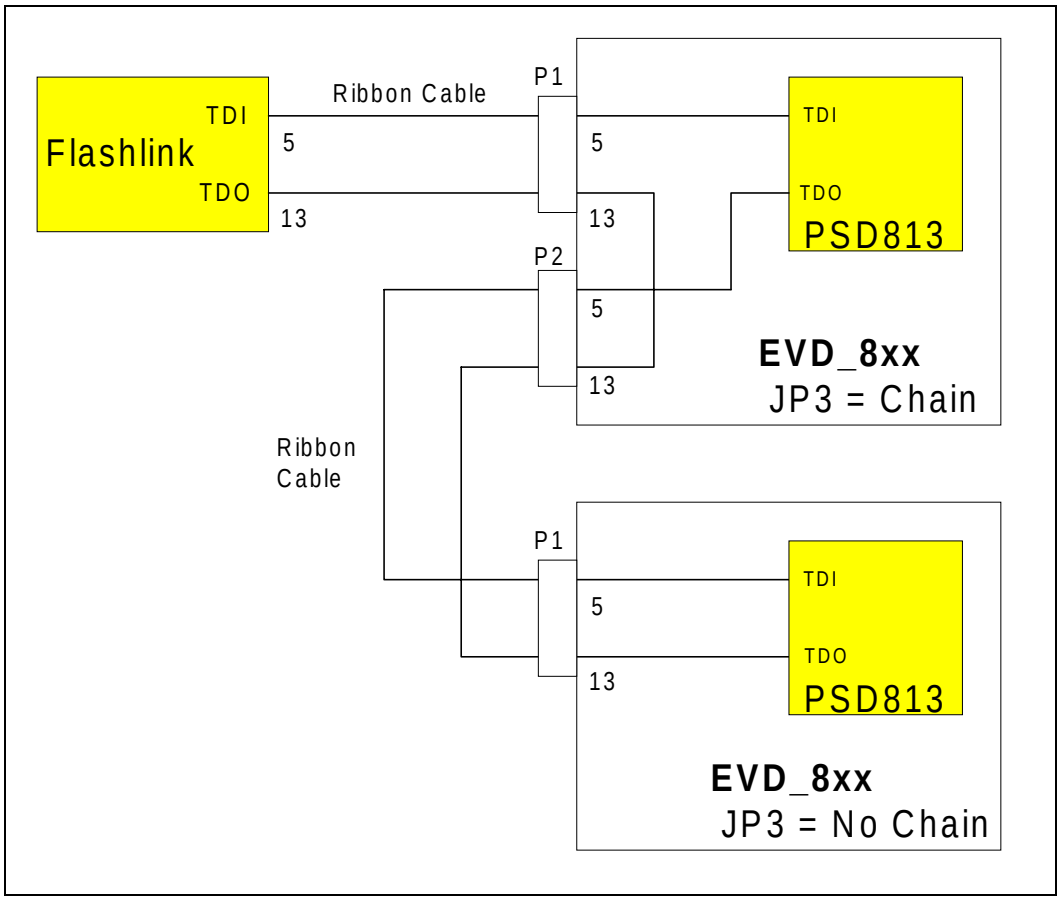

P2 MPU CONTROL / DEMUXED ADDR / PSD PORTS A & B
P1 MPU ADDRESS / DATA / PSD PORTC
J3 HOST RS-232
DB9, female
DS1
HC16201-A
MATES W/ DAUGHTER BOARD
OPC2
OPC1
10k typical
left side
PORT E
PORT D
JP1
JP5
JP3
S1
S2
U1
68HC11ED0CFN3
U2
MAX6315
U3
MS628128
PSD7XX
NOT PSD7XX
CSI NOT ACTIVE
CSI ACTIVE
from FLASHLINK
RST (FROM FLASHLINK)
RESET(TO 7XX)
RST_OUT (FROM 7XX)
P4
PSD PORT D / PSD PORT E
P3
HC11 I/O
P5
Holes for 0.025 post only, no connector locate adjacent to prototype area
Evaluation Mother Board, HC11/PSD
Mark Rootz, Tim Wilkerson - WSI Inc.
2/17/98
Document Number
EVM_HC11
Size B
Rev B
Wednesday, December 02, 1998
Sheet 1 of 2

EVM_HC11_a


J6
1
2
9V
BATTERY
D1
1N4004
D2
1N4004
D4
1N4004
D3
1N4004
D7
1N4004
J7
1
2
9-12 VDC
REGULATED
SOURCE
D5
15V
R21
100k
C15
1
POWER
S2
R22
100k
C16
0.1 uF
D6 1N4148
U5 MIC5237-5.0
IN
OUT
GND
INTERNAL
POWER
SUPPLY
EXTERNAL
POWER
SUPPLY
JP4
C17
1
TP_PS
VCC
C18
0.1 uF
C19
0.1 uF
C20
0.01 uF
C21
0.01 uF
C22
0.01 uF
TP_GND

EVM_HC11_b

Development board chaining



Chaining using Development Board Hardware

Appendix D

Results codes and debug tree for f1_ee.obj

Results codes

	binary	
Results =	abcd	
0	0000	Success Code
1	0001	
2	0010	
3	0011	
4	0100	
5	0101	
6	0110	
7	0111	
8	1000	
9	1001	
A	1010	
B	1011	
C	1100	
D	1101	
E	1110	
F	1111	

Table 3 Hex to Binary Conversion

Debug tree

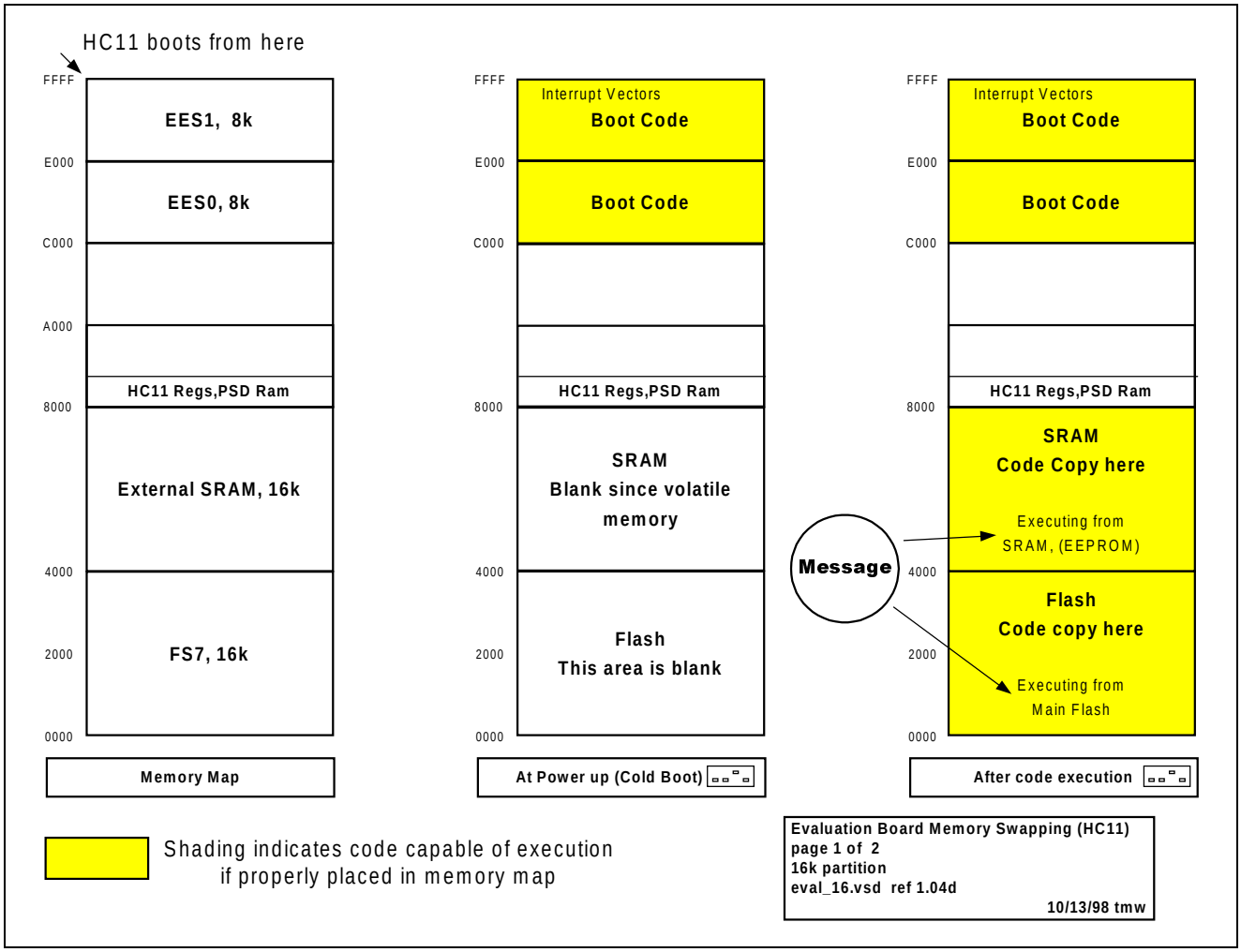
X = don't care

a	**b**	**c**	**d**		**action**
x	x	x	1	Page register test	Replace PSD (u1 on EVD) and retest
x	x	1	x	PSD ram error	Replace PSD (u1 on EVD) and retest
x	1	x	x	External Ram error	Replace sram (u3 EVM) and retest
1	x	x	x	Uart error	Repair u4 or surrounding circuitry, EVM (this is under the EVD board)

Table 4 Debug Tree

Appendix E

Maps for Memory Swapping



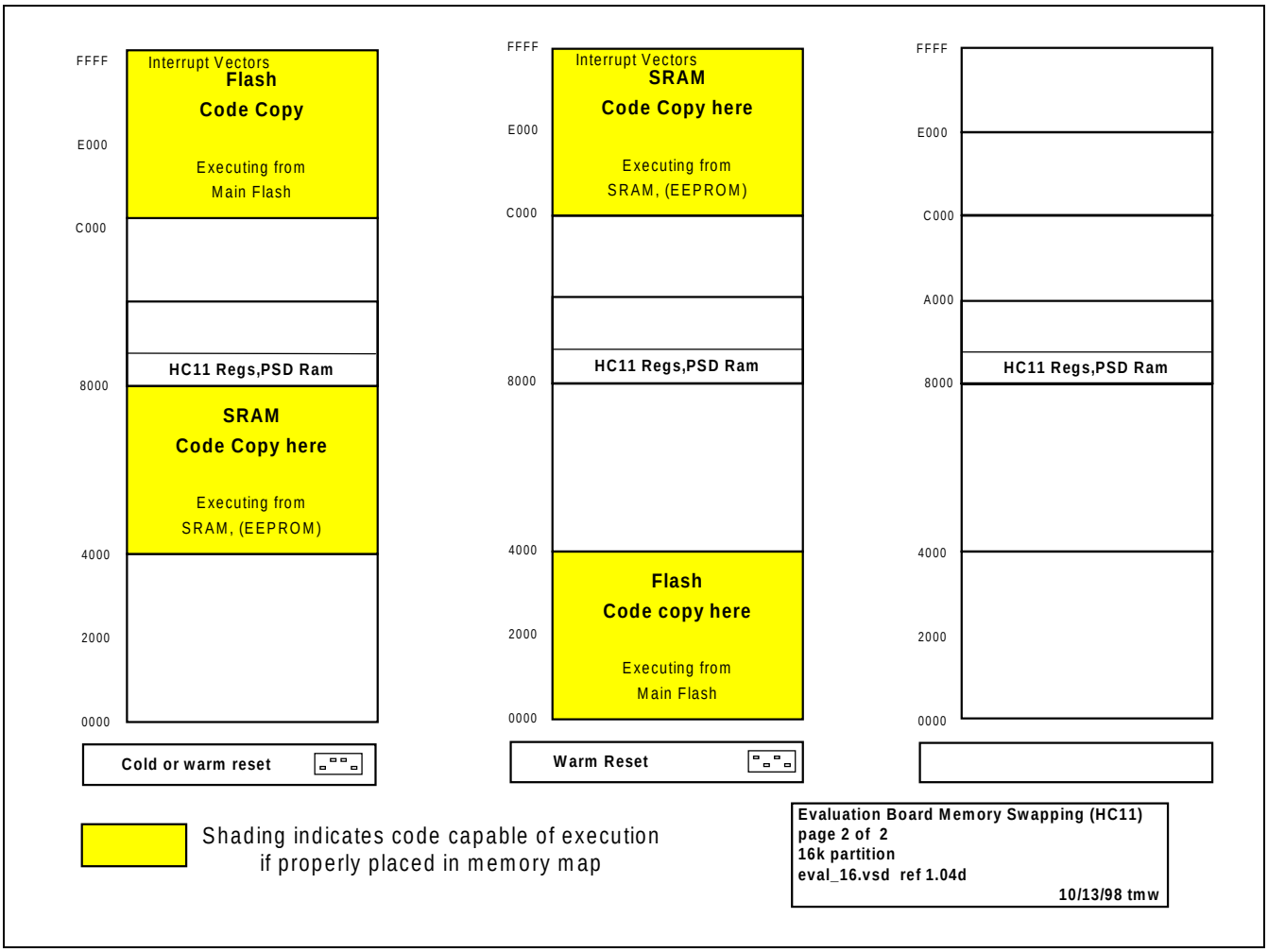

FFFF
Interrupt Vectors
Flash
Code Copy
Executing from
Main Flash
E000
C000
8000
HC11 Regs,PSD Ram
SRAM
Code Copy here
Executing from
SRAM, (EEPROM)
4000
2000
0000
Cold or warm reset
FFFF
Interrupt Vectors
SRAM
Code Copy here
Executing from
SRAM, (EEPROM)
E000
C000
8000
HC11 Regs,PSD Ram
4000
Flash
Code copy here
Executing from
Main Flash
2000
0000
Warm Reset
FFFF
E000
C000
A000
8000
HC11 Regs,PSD Ram
4000
2000
0000
Shading indicates code capable of execution
if properly placed in memory map
Evaluation Board Memory Swapping (HC11)
page 2 of 2
16k partition
eval_16.vsd ref 1.04d
10/13/98 tmw

Table 1. Document Revision History

Date	Rev.	Description of Revision
	1.0	Document written in the WSI format
31-Jan-2002	1.1	DK8_HC11: DK68HC11-52J-110/220 Development Board Front page, and back two pages, in ST format, added to the PDF file Any references to Waferscale, WSI, EasyFLASH and PSDsoft 2000 updated to ST, ST, Flash+PSD and PSDsoft Express

For current information on PSD products, please consult our pages on the world wide web:
www.st.com/psm

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.psd@st.com (for application support)
ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.