AD8307 Evaluation Board

EVAL-AD8307EB

BOARD DESCRIPTION

The AD8307 evaluation board has been carefully laid out and tested to demonstrate the specified high speed performance of the device. Figure 1 shows the schematic of the evaluation board. For ordering information, please refer to the Ordering Guide.

Figures 2 and 4 show the component-side and solder-side silkscreens of the evaluation board. The component-side and solder-side layouts are shown in Figures 3 and 5 respectively.

For connection to external instruments, side-launched SMA type connectors are provided. Space is also provided on the board for the installation of SMB or SMC type connectors. When using the top-mount SMA connector, it is recommended that the stripline on the outside 1/8" of the board edge be removed (i.e., scraped using a blade) as this unused stripline acts as an open stub that could degrade the overall performance of the evaluation board/device combination at high frequencies.

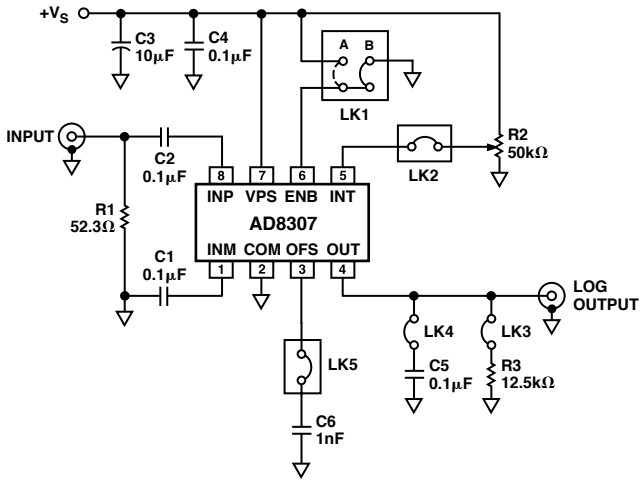

Figure 1. Evaluation Board Schematic

ORDERING GUIDE

Model	Package Description
AD8307-EB	Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the EVAL-AD8307EB features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

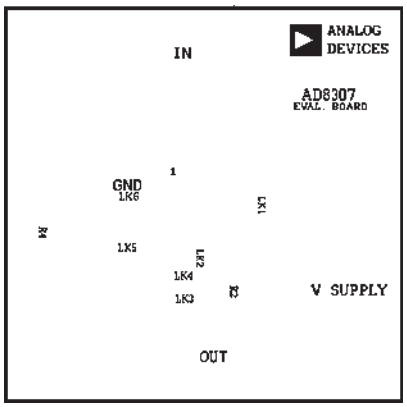

Figure 2. Component Side Silkscreen

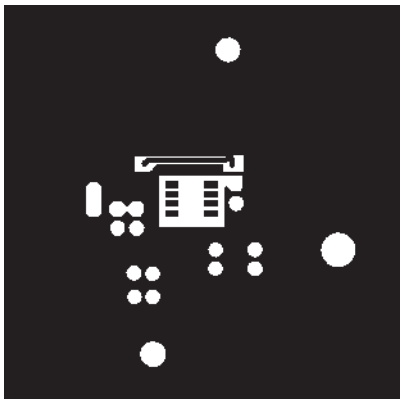

Figure 3. Board Layout (Component Side)

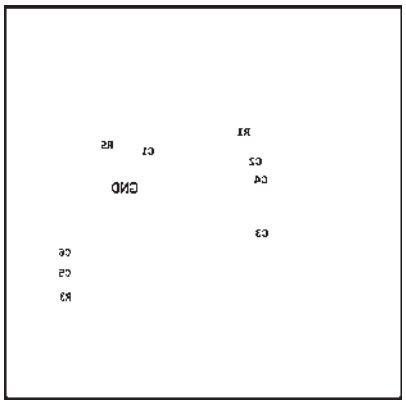

Figure 4. Solder Side Silkscreen

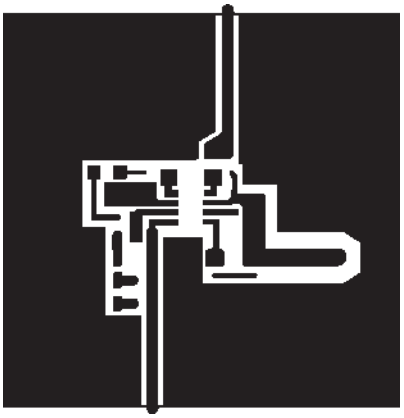

Figure 5. Board Layout (Solder Side)

Link and Trim Options

There are a number of link options and trim potentiometers on the evaluation board that should be set for the required operating setup before using the board. The functions of these link options and trim potentiometers are described in detail in Table I.

Table I. Evaluation Board Link Options

Link No.	Default Position	Function
LK1	A	Power Up/Power Down. When this link is in position B, the ENB pin is connected to ground, putting the AD8307 in power-down mode. Placing this link in position A connects the ENB pin to the positive supply, thereby putting the AD8307 in normal operating mode.
LK2	Open	Intercept Adjust. When Pin LK2 is left open, the AD8307 has a nominal logarithmic intercept of –84 dBm. Putting LK2 in place connects the wiper of potentiometer R2 to Pin 5 (INT). By varying the voltage on INT, the position of the intercept can be adjusted. The intercept varies by about 8 dB/V.
LK3	Open	Slope Adjust. When this link is open, the nominal slope of the output is 25 mV/dB. Putting this link in place connects a ground referenced 12.5 kΩ load resistor (R3) to the logarithmic output. The parallel combination of this resistor and an internal 12.5 kΩ resistor reduces the logarithmic slope to 12.5 mV/dB. R3 may be adjusted for other scaling factors.
LK4	Open	Corner Frequency of Low-Pass Demodulating Filter. When this link is open, the corner frequency of the low-pass post demodulation filter has a nominal value of 4 MHz. This is set by an on-chip load impedance of 12.5 kΩ and an on-chip load capacitance of 3.5 pF. The load capacitance (e.g., of an oscilloscope probe) must be added to this capacitance, and will lower the internal video bandwidth to a nominal 1 MHz for a total of 13.5 pF. Putting LK4 in place connects an external load capacitance (C5) of 0.1 μF to the output, reducing the corner frequency of the low-pass filter to about 125 Hz. For large values of C5, the corner frequency can be calculated using the equation, $f \approx 12.7\ Hz/C5\ (\mu F)$.
LK5	Open	Offset Control Loop. When this link is open, the internal offset control loop gives the circuit an overall high-pass corner frequency of about 1 MHz. With LK5 link in place, a 1 nF capacitor (C6) is connected to the OFS pin, reducing the high-pass corner frequency to allow accurate operation down to 10 kHz. To reduce the minimum operational frequency even further, a larger capacitor can replace C6 (e.g., a 1 μF capacitor allows operation down to 10 Hz). Note that external capacitor C6 has no effect on the minimum signal frequency for input levels that exceed the offset voltage (typically 400 μV). The range for such signals extends down to dc (for signals applied directly to the input pins).

C03290–0–12/02(0)

PRINTED IN U.S.A.