SigmaDSP™ Evaluation Board

EVAL-AD1953EB

OVERVIEW

The AD1953 evaluation board (EVAL-AD1953EB) permits testing and demonstration of the AD1953 3-channel, 24-bit SigmaDSP audio processor. An input signal is required in either optical or coaxial S/PDIF format, or directly via one of three 10-pin headers in I^2S, left-justified, right-justified, or DSP modes. The internal signal processing program and parameters of the AD1953 can be controlled by a 25-lead SPI interface to a computer's parallel port.

Power requirements are a ±9 V to +12 V dc source for both the analog and digital sections. On-board regulators drive separate "clean" 5 V dc supplies for the digital and analog sections. Three analog RCA phone jacks provide analog audio output. Digital output comes from optical and RCA jacks in S/PDIF format.

AD1953 OVERVIEW

The AD1953 is a complete 26-bit, single-chip, 3-channel digital audio playback system with built-in DSP functionality for speaker equalization, dual-band dynamics processing (compressor/expander/limiter/noise gate), delay compensation, and spatial enhancement. These algorithms can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of perceived audio quality.

The signal processing used in the AD1953 is comparable to that found in high end studio equipment. Most of the processing is done in full 48-bit double-precision mode, resulting in very good low level signal performance and the absence of limit cycles or idle tones. The compressor/limiter uses a sophisticated two-band algorithm often found in high end broadcast compressors.

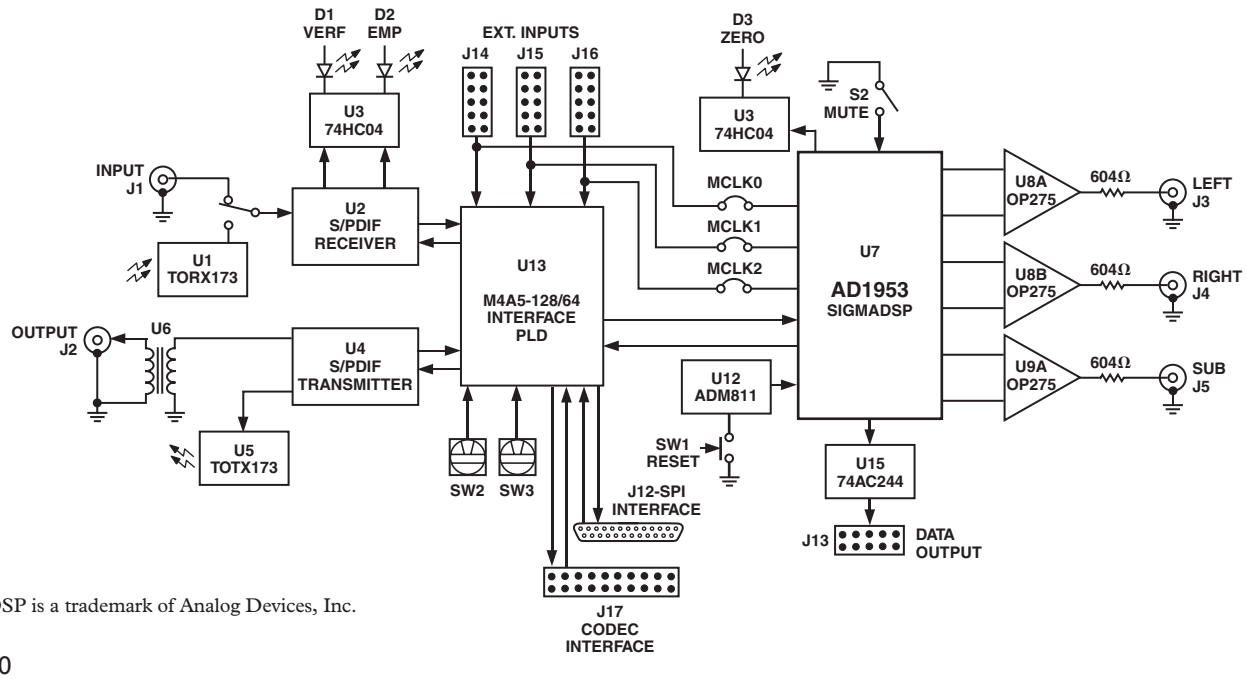
An extensive SPI port allows click-free parameter updates, along with readback capability from any point in the algorithm flow.

The AD1953 also includes ADI's patented multibit sigma-delta DAC architecture that provides 112 dB SNR and dynamic range and THD+N of –100 dB. These specifications allow the AD1953 to be used in applications ranging from low end boom boxes to high end professional mixing/editing systems.

The AD1953 also has a digital output that allows it to be used purely as a DSP. This digital output can be used to drive an external DAC to extend the number of channels beyond the three that are provided on the chip.

The AD1953 operates from a single 5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 48-lead LQFP package for operation over the temperature range –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM



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PERFORMANCE SPECIFICATIONS

The typical evaluation board performance is tabulated below.

1. SNR 112 dB ± 1 dB
2. DR, A-Weighted 112 dB ± 1 dB
3. THD + N –100 dB ± 2 dB
4. Frequency Response ±0.2 dB, 20 Hz to 20 kHz (0 dBFS)
5. Noise Floor –145 dB
6. Full-Scale Audio Output 2.0 V_{rms}

FUNCTIONAL DESCRIPTION

The AD1953 evaluation board presents a reference design that can be used as a suggested layout and circuit implementation that will deliver optimal performance from the SigmaDSP audio processor. As far as is possible, current assembly methods and components are used on the evaluation board. Most components are surface-mount devices, although there is a version of the evaluation board that uses through-hole components in the output filters, and a four-layer printed circuit board is used with full internal power and ground planes for superior noise performance. A schematic, bill of materials, and PCB plots are included for guidance.

POWER SUPPLIES

The board is divided into analog and digital sections, with common power supplies.

The power supply is input via binding posts J8, J9, and J10. The recommended supply settings are +12 V dc with a maximum current of +350 mA and –12 V dc with a maximum current of –50 mA. An on-board, low noise voltage regulator (U11) provides 5 V dc, ±5% to the evaluation board circuit.

DIGITAL SIGNAL INPUTS AND OUTPUTS

RCA phone jack J1 and optical TOSLINK input U1 may be used for standard consumer mode S/PDIF input signals. J1 is terminated with a 75 Ω resistor. Switch S1 selects between J1 and U1 inputs and feeds the selected signal to the digital interface receiver (U2).

The EXT DATA INTF 1/2/3 (J14, J15, and J16) inputs permit access, buffered via U13, to the BCLK, LRCLK, SDATA, and MCLK inputs of the AD1953. This permits testing with left-justified, I^2S, or right-justified serial input modes. Note that switch SW3 must be set to correspond to the input data format. When using the direct input header, it is necessary to provide all four signals: MCLK, BCLK, LRCLK, and SDATA. A termination network consisting of a series-connected 100 Ω resistor and a 47 pF capacitor is shunted across each signal line to reduce line reflections.

Digital audio signals are output through the RCA phone jack J2 or TOSLINK output U5. Both output jacks are always "on," so no switch is needed to select between the two. The transformer (U6) on the output buffers the external connection from the rest of the evaluation board to prevent a ground loop.

Header J13 is for the serial data output from the input MUX and the data capture serial output. Either of these two signals, coupled with the left/right clock and bit clock signals, form a valid 3-wire output. This header can be used to connect an external DAC to the AD1953 evaluation board.

Twenty-lead header J17 is for interfacing to an Analog Devices codec evaluation board. This connection can be used to supply two serial data lines from external ADCs and all of the necessary clocks to the AD1953 evaluation board, as well as to send the serial data to the external DACs.

Headers J6 and J7 are for future expansion and functionality of the evaluation board.

EXTERNAL SPI CONTROL PORT

The AD1953 evaluation board includes a 25-lead header that interfaces the chip's SPI input with a computer's parallel port. This port is capable of full read/write operation for all of the memories (program and parameter) and some of the SPI registers. Most signal processing parameters are controlled by writing new values to the parameter RAM using the SPI port. Other functions, such as volume and de-emphasis filtering, are programmed by writing to SPI control registers. Details of signal format and timing can be found in the AD1953 data sheet.

AUDIO SIGNAL OUTPUTS

RCA jacks J3, J4, and J5 provide left, right, and sub outputs, respectively. The output is low-pass filtered with an anti-image filter and converted from a differential voltage output to single-ended voltage by op amps U8 and U9. The left and right channel filters' –3 dB cutoff frequency is 100 kHz and has an approximate third order Bessel (linear phase) response. The subwoofer channel uses the same filter but with a –3 dB cutoff at 10 kHz. The output impedance is approximately 600 Ω. The full-scale output signal is 2.0 V_{rms} for all channels.

SWITCH AND JUMPER FUNCTIONS

A quick reference for the default switch and jumper positions is shown in Table I. These settings should be used for a first-time use of the evaluation board. All directional references assume that the board is facing with the digital connections on the left and the analog connections on the right. A more detailed description of each switch and jumper follows.

Table I. Default Switch/Jumper Positions

Jumper/Switch	Position	Setting
S1	Down	RCA Input
S2	Right	Mute Off
S4	Don't Care	For Future Functionality
S5	Don't Care	For Future Functionality
SW2	0	See Tables II and III
SW3	0	See Table IV
LK2	B (Right)	5 V
LK5	On (Down)	AVDD Reference
LK6	Off (Up)	XREF Off
LK9	C (Bottom)	DIR_MCLK
LK10	B (Right)	MCLK1_INTF
LK11	B (Right)	MCLK2_INTF

Slide switch S1 selects between the RCA S/PDIF input and the TOSLINK input.

Push-button switch SW1 provides a RESET function via reset generator U12 (ADM811) and a "clean" 240 ms delay after release. U12 also provides a 240 ms reset pulse at power-up.

A 16-position rotary switch (SW2) controls the signal routing on the evaluation board. The source of the SDATA, BCLK, and LRCLK signals for each of the three MUXes is indicated in Table II. Table III shows the source of signals driving the CS8404A (U4, S/PDIF digital output transmitter). In each of these two tables,

the column entries are the signal sources and the headings are the signal destinations for a given switch position.

Note: Switch position F is not used.

Table II. SW2 Settings—Signal Sources

SW2 Pos.	MUX 0	MUX 1	MUX 2	AUXDATA
0	8414	Ext. port 1	Ext. port 2	Ext. port 0
1	Ext. port 0	8414	Ext. port 2	Ext. port 1
2	Ext. port 0	Ext. port 1	8414	Ext. port 2
3	Ext. port 0	Ext. port 1	Ext. port 2	8414
4	8414	Ext. port 1	Ext. port 2	Ext. port 0
5	Ext. port 0	8414	Ext. port 2	Ext. port 1
6	Ext. port 0	Ext. port 1	8414	Ext. port 2
7	Ext. port 0	Ext. port 1	Ext. port 2	8414
8	8414	Ext. port 1	Ext. port 2	Ext. port 0
9	Ext. port 0	8414	Ext. port 2	Ext. port 1
A	Ext. port 0	Ext. port 1	8414	Ext. port 2
B	ASDATA1	ASDATA1	ASDATA1	ASDATA2
C	ASDATA2	ASDATA2	ASDATA2	ASDATA1
D	ASDATA1	ASDATA1	ASDATA1	ASDATA2
E	ASDATA2	ASDATA2	ASDATA2	ASDATA1

Table III. SW2 Settings—CS8404A Signal Sources

SW2 Pos.	8404 SDI	8404 LRCLK/BCLK	8404 MCLK (128 f_S)*
0	DCSOUT	8414	8414 (* 1/2)
1	DCSOUT	8414	8414 (* 1/2)
2	DCSOUT	8414	8414 (* 1/2)
3	DCSOUT	MUX OUT	MCLKOUT (* 1/2)
4	SDATAOUT	MUX OUT	8414 (* 1/2)
5	SDATAOUT	MUX OUT	8414 (* 1/2)
6	SDATAOUT	MUX OUT	8414 (* 1/2)
7	SDATAOUT	MUX OUT	8414 (* 1/2)
8	DCSOUT	MUX OUT	MCLKOUT (* 1/2)
9	DCSOUT	MUX OUT	MCLKOUT (* 1/2)
A	DCSOUT	MUX OUT	MCLKOUT (* 1/2)
B	DCSOUT	MUX OUT	Ext. CODEC (* 1/2)
C	DCSOUT	MUX OUT	Ext. CODEC (* 1/2)
D	SDATAOUT	MUX OUT	Ext. CODEC (* 1/2)
E	SDATAOUT	MUX OUT	Ext. CODEC (* 1/2)

*MCLK input signals to the CS8404 are divided by two in the PLD because this part runs on 128 f_S, while the rest of the board runs on a 256 f_S MCLK.

Rotary switch SW3 determines which serial interface format is selected. Table IV shows the different modes.

Note: Switch positions 6–F are not used.

Table IV. SW3 Settings

SW3 Position	Serial Data Format
0	I^2S
1	Right Justified — 24-bit
2	DSP
3	Left Justified
4	Right Justified — 20-bit
5	Right Justified — 16-bit

Switch S2 enables the AD1953 mute function.

Push-button switch SW4 and switches S4 and S5 are not currently functional but will be used in future evaluation board revisions.

Jumper LK2 selects between an external supply (Position A) or a 5 V input (Position B) to the AD1953's ODVDD pin. ODVDD is the supply for the digital output pins. Using an external supply at 3 V allows the outputs to be 3.3 V compatible. The switch should be left in the 5 V position if no external power supply is connected to the EXT side of the jumper.

Jumper LK9, LK10, and LK11 select between internal and external MCLK inputs to the MCLK MUX for MCLK0, MCLK1, and MCLK2, respectively. For LK9, Position A selects the MCLK0_INTF from External Data Interface 0 (J14), Position B selects the MCLK from the codec interface header (J17), and Position C selects the recovered DIR_MCLK from the S/PDIF receiver (U2). For LK10 and LK11, in the left Position (A), the DIR_MCLK signal from U2 is selected. Position B selects the MCLKx_INTF signal from external data header J15 and J16.

Jumpers LK5 and LK6 connect the reference voltage to the VREF_IN pin. If LK5 is on, then the voltage will come from AVDD. With LK6 on, the reference voltage will be taken from the external reference Test Point 1 (TP1).

INDICATOR DISPLAY LEDS

Five LED indicators are provided for status indication.

- Display LED D1, VERF, indicates that the S/PDIF digital interface receiver has detected an error condition in the received signal. When not illuminated, this LED is a good indicator that there is a signal present on the S/PDIF input.
- Display LED D2, EMP, indicates that the incoming signal has had pre-emphasis added.
- Display LED D3, ZERO, is provided to show that the AD1953 is detecting a zero input in one of the two input channels.
- Display LEDs D6 and D11, DVDD and AVDD, show the presence of 5 V dc on the digital and analog 5 V power supplies, respectively.

INTEGRATED CIRCUIT FUNCTIONS

There are 16 active devices on the AD1953 evaluation board. Following is a brief description of the function of each part.

- U1 (TORX173) is the Toshiba digital audio optical receiver. It accepts the visible red S/PDIF modulated signal and converts it to a standard TTL digital signal suitable for input to the digital audio receiver (U2).
- U2 (CS8414-CS) receives the serial S/PDIF digital audio encoded signal and decodes the audio information. The CS8414 decodes four digital signals from the serial input stream: the serial data SDATA, the master clock MCLK, the left/right frame clock LRCLK, and the serial bit clock BCLK at 64 Fs. The output interface mode of U2 must be compatible with the input to the AD1953 (U7). This mode is selected at the same time for both U2 and U7 via switch SW3.
- U3 (74HC04) is a quad input logic inverter that provides miscellaneous buffering and interface functions.
- U4 (CS8404A-CS) is the S/PDIF transmitter that takes in the serial data SDATA, master clock MCLK, the left/right

frame clock LRCLK, and the serial bit clock BCLK, and outputs the S/PDIF signal to the TOSLINK transmitter and the RCA output jack.

- U5 (TOTX173) is the Toshiba digital audio optical transmitter. It creates a visible red S/PDIF modulated signal from the standard TTL digital signal output of the digital audio transmitter (U4).
- U6 (SC937-02) is a digital audio transformer with low jitter and high CMRR that provides buffering between the evaluation board and the external circuit, preventing ground loops.
- U7 (AD1953) is the SigmaDSP digital audio processor and converter.
- U8 and U9 (OP275) are low noise and distortion audio op amps. U8 provides differential-to-single-ended conversion for the left and right channel outputs, while U9 does the same for the sub channel. A third order low-pass Bessel filter response is implemented with a –3 dB corner frequency of 100 kHz on the left and right channels, 10 kHz on the subchannel, and a 60 dB/decade (18 dB/octave) roll-off. This type of filter is characterized by a linear phase response and fast transient response without overshoot.
- U10 (LM317) provides 5 V dc low voltage regulation for the digital section of the evaluation board.
- U11 (ADP3303-5) is a low noise 5 V dc regulator for the analog section of the AD1953.
- U12 (ADM811) is a RESET generator that provides a debounced reset signal from the push-button (SW1) or a 240 ms reset pulse on power-up.
- U13 (M4A5-128/64) provides decoding, buffering, and selection functions between the different modes of operation.
- U14 (74HC243) is a quad three-state noninverting buffer.
- U15 (74AC244) is an octal noninverting buffer/line driver with three-state outputs.
- U16 (NC7S14) is a high performance inverter with Schmitt trigger input.

SOFTWARE

The AD1953 evaluation board comes with software that can be used to control all of the part's functions. The evaluation board interfaces with this software via the 25-lead header (J12), which connects to a computer's parallel port.

Custom programming tools are available for the AD1953. A Graphical Compiler, in conjunction with OrCAD, can be used to design custom signal processing algorithms using any of the AD1953's processing blocks. All settings can be programmed with this Graphical Compiler, which writes to the program and parameter RAMs through the SPI port of the AD1953.

More in-depth documentation is available for all software.

FURTHER INFORMATION

Ordering information: order number is EVAL-AD1953EB.

For application questions, please contact our Central Applications Department at 1-781-937-1428.

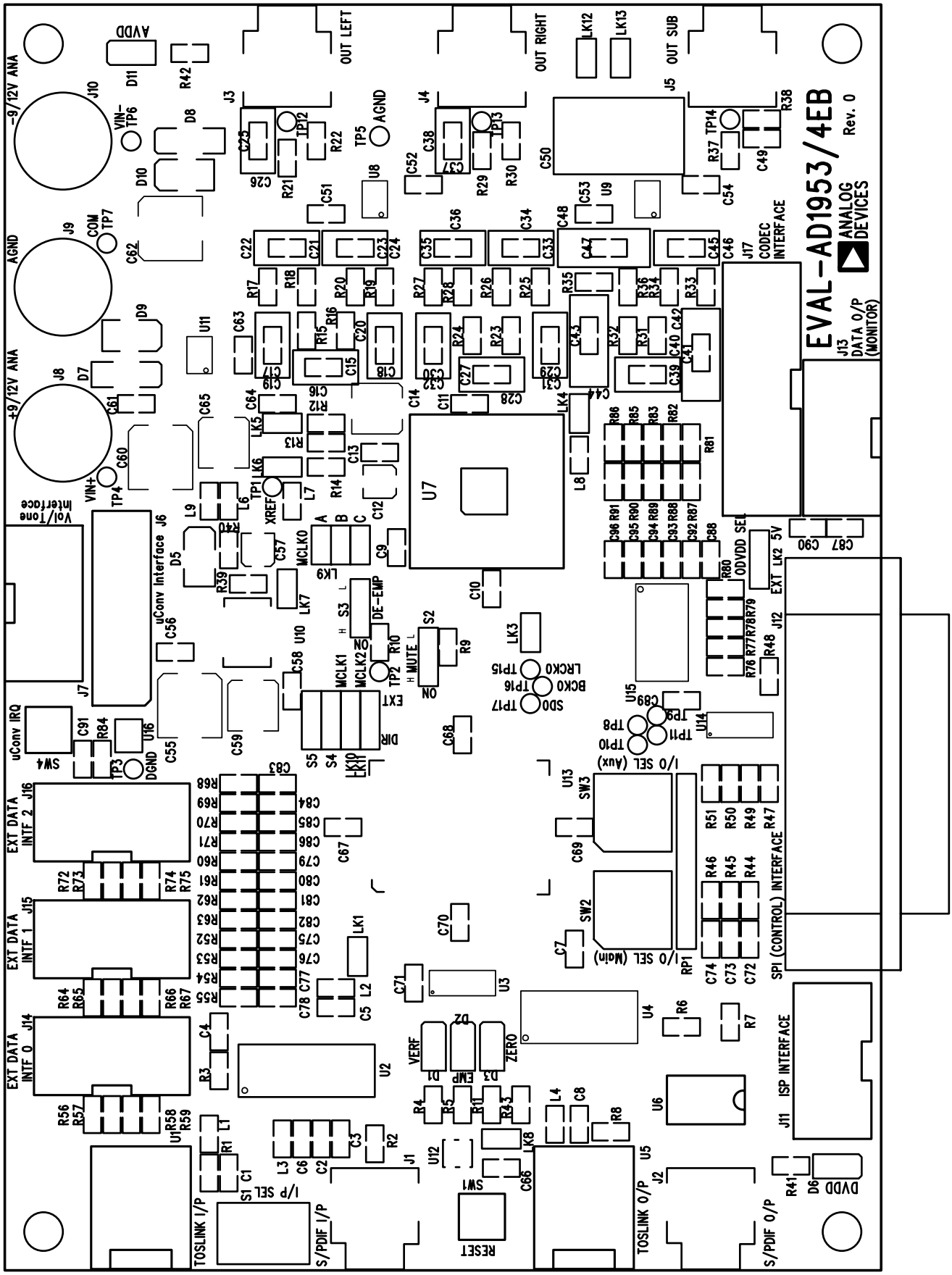

Figure 1. Silkscreen – Top Overlay

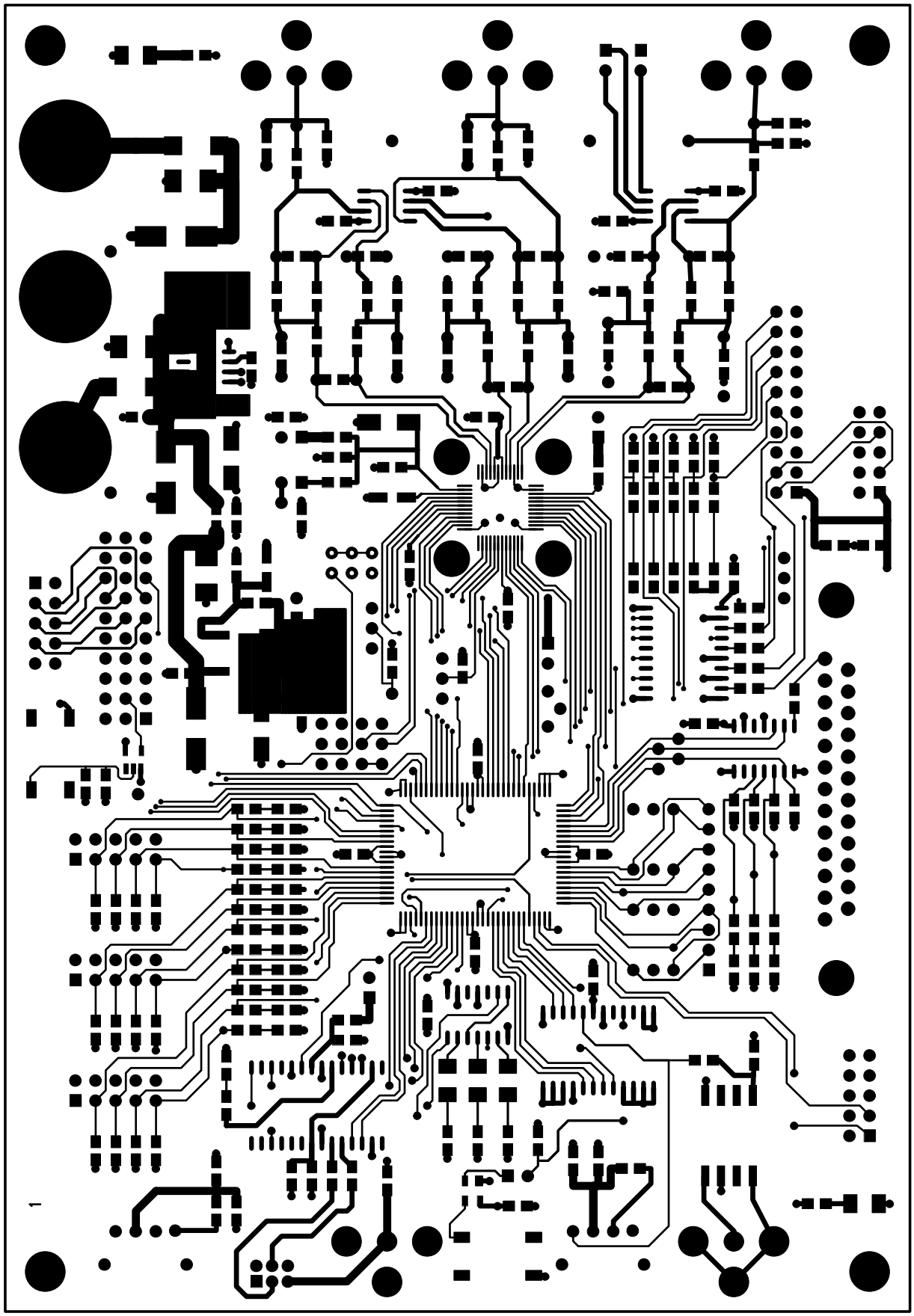

Figure 2. Component – Top Layer

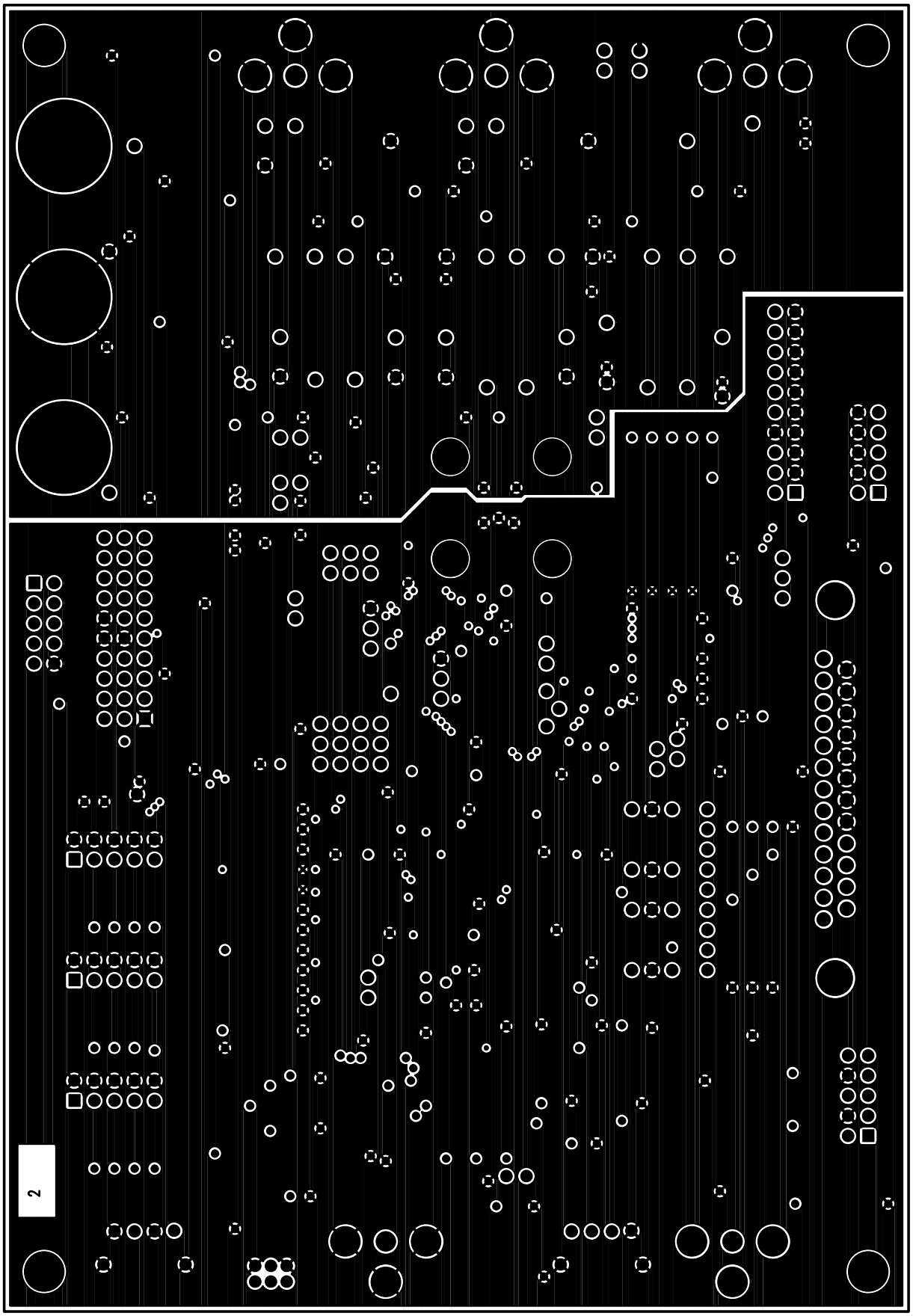

Figure 3. Internal Plane 2 – Ground Planes

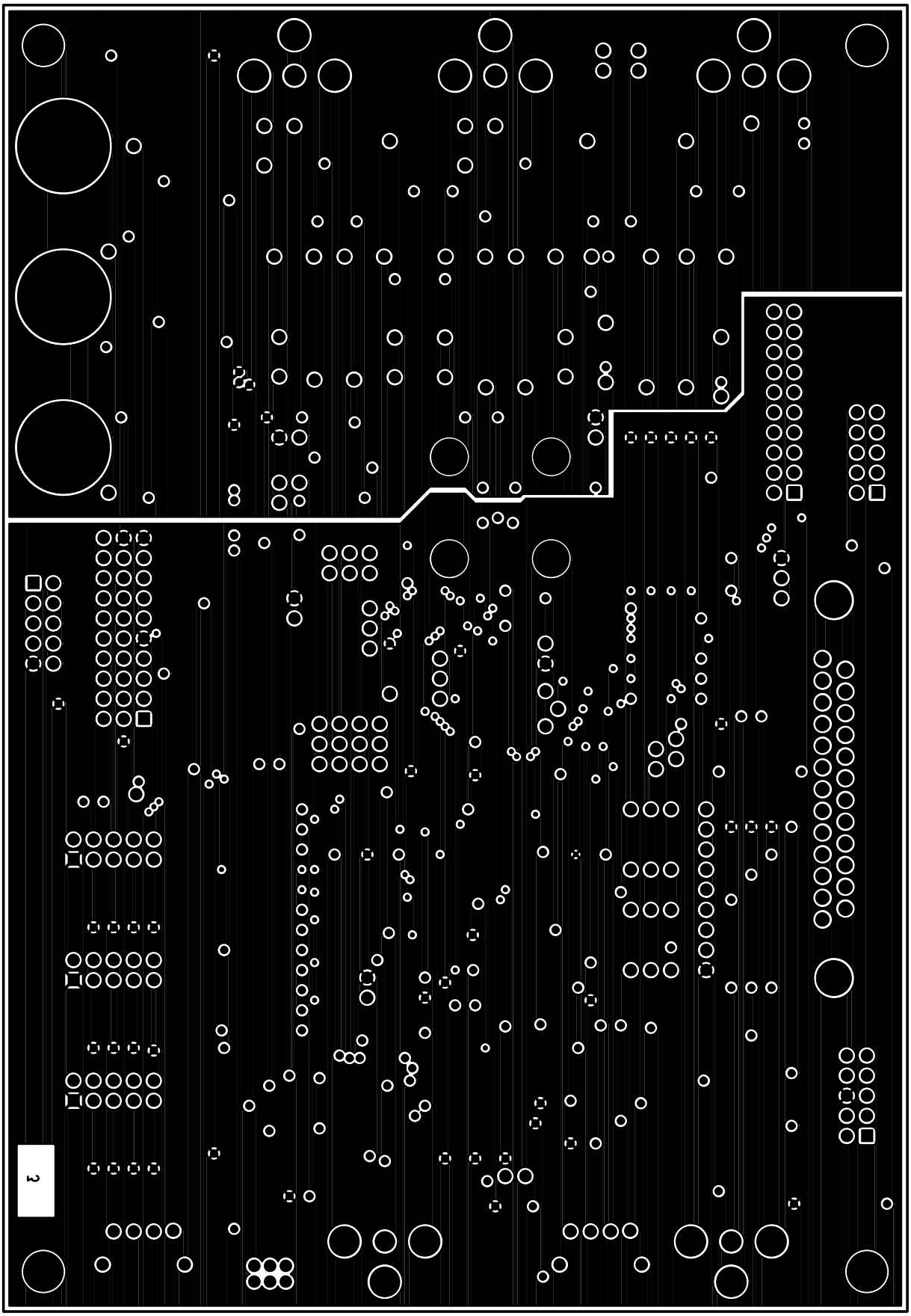

Figure 4. Internal Plane 3 – Power Planes

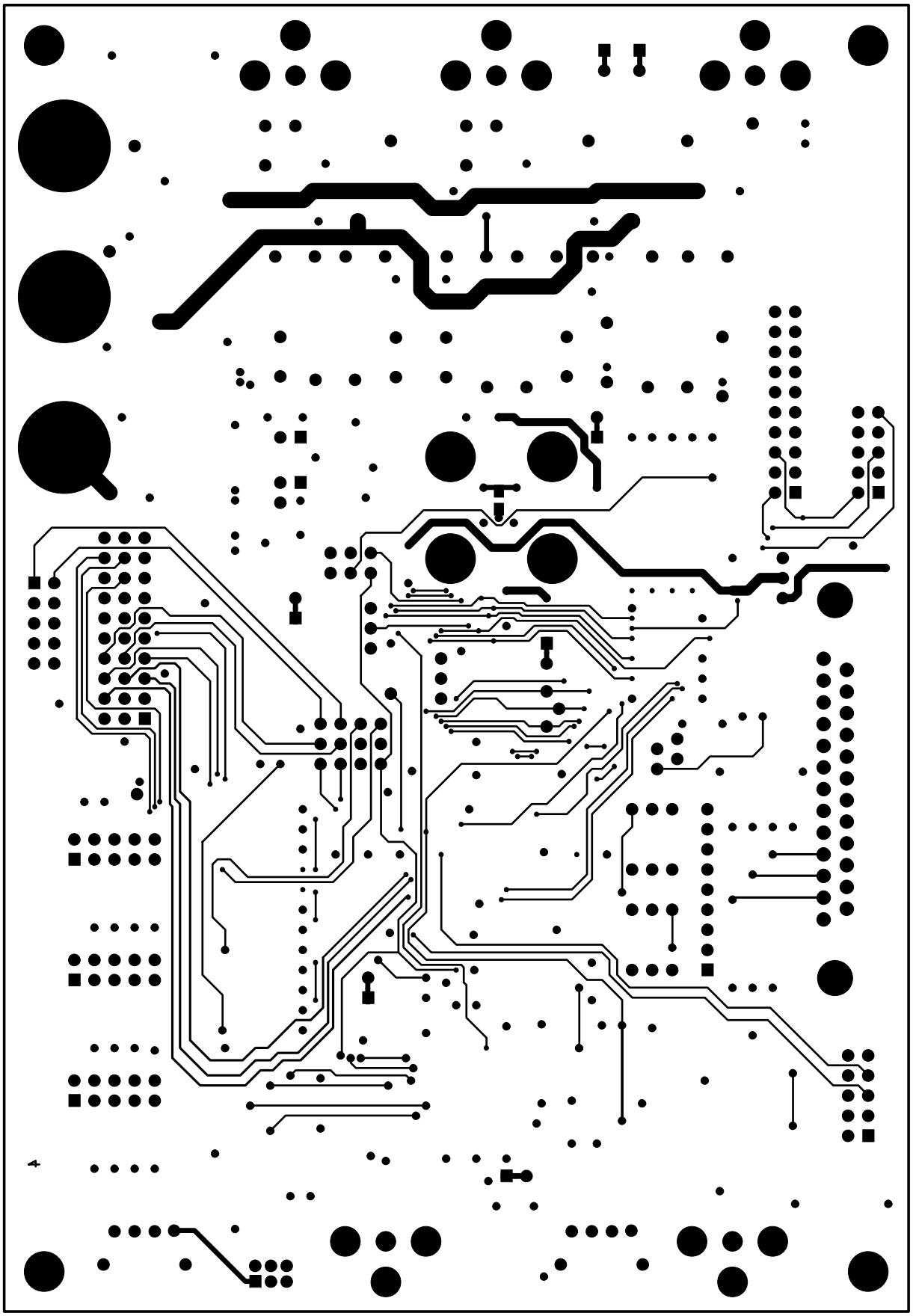

Figure 5. Bottom Layer – Solder Side

Bill of Materials

Qty. Used	Designator	Description	Part Decal	Value
27	C1, C5–C11, C13, C51–C54, C56, C58, C61, C64, C66–C71, C87–C90	Multilayer Ceramic 50 V X7R	SMD 0805 Case	0.1 µF
4	C2, C3, C63, C91	Multilayer Ceramic 50 V X7R	SMD 0805 Case	10 nF
1	C4	Multilayer Ceramic 50 V X7R	SMD 0805 Case	68 nF
2	C12, C57	SMD Aluminum Electrolytic Capacitor (Case B) 16 V	CAP\ELEK_SMD_B	10 µF
3	C14, C59, C65	SMD Aluminum Electrolytic Capacitor (Case D) 16 V	CAP\ELEK_SMD_D	47 µF
3	C15, C27, C39	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	100 pF
3	C16, C28, C40	P-Series Polypropylene Capacitor	CAP-5 mm	100 pF
2	C17, C29	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	1 nF
2	C18, C30	Film Chip Capacitor, 5%, 50 V, PPS	SMD 0805 Case	2 n7F
2	C19, C31	P-Series Polypropylene Capacitor	CAP-5 mm	1 nF
2	C20, C32	P-Series Polypropylene Capacitor	CAP-5 mm	2 n7F
2	C21, C33	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	270 pF
2	C22, C34	P-Series Polypropylene Capacitor	CAP-5 mm	270 pF
2	C23, C35	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	820 pF
2	C24, C36	P-Series Polypropylene Capacitor	CAP-5 mm	820 pF
2	C25, C37	Film Chip Capacitor, 5%, 50 V, PPS	SMD 0805 Case	2n2F
2	C26, C38	P-Series Polypropylene Capacitor	CAP-5 mm	2n2F
1	C41	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	270 pF
1	C42	Panasonic PPS (ECHS) Series Capacitor	CAP-5 mm	27 nF
1	C43	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	560 pF
1	C44	Panasonic PPS (ECHS) Series Capacitor	CAP-5 mm	56 nF
1	C45	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	68 pF
1	C46	Panasonic PPS (ECHS) Series Capacitor	CAP-5 mm	6n8F
1	C47	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	150 pF
1	C48	Panasonic PPS (ECHS) Series Capacitor	CAP-5 mm	15 nF
1	C49	Film Chip Capacitor, 5%, 50 V, PPS	SMD 0805 Case	2n2F
1	C50	Panasonic PPS (ECHS) Series Capacitor	CAP-5 mm	220 nF
3	C55, C60, C62	SMD Electrolytic Capacitor (Case D) 25 V	CAP\ELEK_SMD_E	47 µF
20	C72–C86, C92–C96	Ceramic Chip Capacitor, 5%, 50 V, NPO	SMD 0805 Case	47 pF
2	D1, D6	Red Light Emitting Diode	LED_SMT	Red
2	D2, D3	Yellow Light Emitting Diode	LED_SMT	Yellow
1	D11	Green Light Emitting Diode	LED_SMT	Green
2	D7–D8	SMD Aluminum Rectifier Diode, 50 V, 1 A, SOD-87	MELF1	
3	D5, D9–D10	15 V Zener Diode	DIODE-SMB	15 V
5	J1–J5	Audio Connector—RCA Female Right Angle	PHONO	
1	J8	Connector, Binding Post (Uninsulated Base)	BINDING-POST	Yellow
1	J9	Connector, Binding Post (Uninsulated Base)	BINDING-POST	Green
1	J10	Connector, Binding Post (Uninsulated Base)	BINDING-POST	Blue
6	J7, J11, J13–J16	10-Way (5 × 2) IDC Header—Shrouded	HEADER10-POL	
1	J12	CON\DB25HM	DB25-HM	
	J17	20-Way (10 × 2) IDC Header—Shrouded		
6	L1–L4, L8–L9	Chip Ferrite Bead 600 Ω @ 100 MHz	SMD 0805 Case	
1	L5	Chip Ferrite Bead 600 Ω @ 100 MHz	SMD 0805 Case	
2	L6, L7	Do Not Insert	SMD 0805 Case	
2	LK5–LK6	Jumper Block, 2 PINS 0.1" SPACING	SIP-2P	
7	LK1, LK3–LK4, LK7–LK8, LK12–LK13	Do Not Insert	SIP-2P	
6	LK2, LK10–LK11, S2, S4, S5	Jumper Changeover × 1	LINK-3P	
1	LK9	6-Pin Square Pin Header (3 × 2) 0.1" Pitch		

Bill of Materials (continued)

Qty. Used	Designator	Description	Part Decal	Value
27	R1, R9, R12–R14, R43, R47, R49–R51, R56–R59, R64–R67, R72–R75, R81, R82, R83, R85, R86	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	10.0 kΩ
1	R2	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	75 Ω
1	R3	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	475 Ω
5	R4–R5, R11, R41–R42	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	649 Ω
1	R6	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	374 Ω
1	R7	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	90.9 kΩ
1	R8	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	8.25 kΩ
2	R15, R23	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	2.80 kΩ
2	R16, R24	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	806 Ω
3	R17, R25, R34	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	3.01 kΩ
3	R18, R26, R36	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	1.50 kΩ
2	R19, R27	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	1.00 kΩ
2	R20, R28	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	499 Ω
2	R21, R29	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	549 Ω
3	R22, R30, R38	Resistor	SMD 0805 Case	OPEN
2	R31, R33	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	11.0 kΩ
2	R32, R35	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	5.62 kΩ
1	R37	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	604 Ω
1	R39	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	243 Ω
1	R40	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	715 Ω
20	R44–R46, R52–R55, R60–R63, R68–R71, R87–R91	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	100 Ω
6	R48, R76–80	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	22.1 Ω
1	R84	Chip Resistor 1% 100 mW Thick Film	SMD 0805 Case	100 kΩ
1	RP1	RES-PACK8	SIP-9P	10 kΩ
1	S1	DPDT PCB Switch (Top Actuator)	SW-DPDT-SLIDE	
2	SW1, SW4	SMD Push-Button Switch (Sealed 6 mm × 6 mm)	SW\PB-SMALL	
2	SW2–3	HEX Rotary Switch	SW-ROTARY-HEX	
17	TP1–17	Testpoint	TESTPOINT	
1	U1	Fiber Optic Receiving Module for Digital Audio	TORX173	TORX173
1	U2	96 kHz Digital Audio Receiver	SO28WB	DIR-CS8414-CS
1	U3	HEX INV	SO14NB	74HC04
1	U4	96 kHz Digital Audio Transmitter	SO24WB	CS8404A-CS
1	U5	Fiber Optic Transmitting Module for Digital Audio	TORX173	TOTX173
1	U6	Digital Audio Signal Transformer (AES/EBU)	TRAFFO-SC937-02	TRAFFO-SC937-02
1	U7	AD1953 – SigmaDSP	LQFP48	AD1953YST
2	U8–9	Dual Bipolar/JFET Audio Op Amp	SO8NB	OP275GP
1	U10	Three Terminal Adjustable Regulator	D-PAK	LM317
1	U11	Precision Low Dropout Voltage Regulator	SO8NB	ADP3303AR-5
1	U12	Voltage Monitor	SOT143	ADM811R-ART
1	U13	CPLD	QFP100-3	CPLD-M4A5-128/64-10YC
1	U14	Quad Bus Transciever Three-State Noninverting	SO14NB	74HC243
1	U15	Octal Buffer/Line Driver Three-State Outputs	SO20WB	74AC244
1	U16	NC7S14	SOT23-5	NC7S14
4		PCB Standoffs		

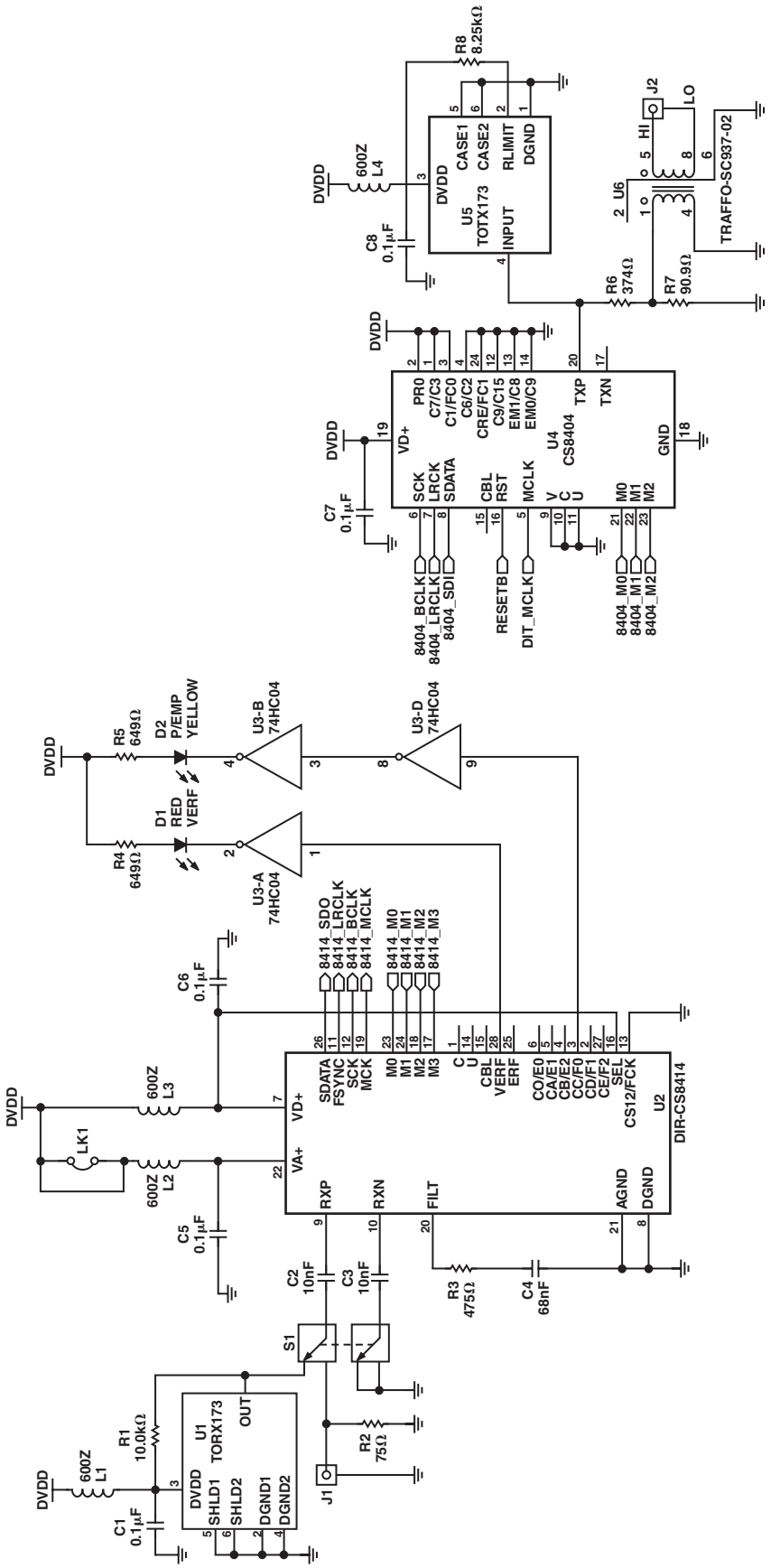

Figure 6. Evaluation Board, S/PDIF Interfaces

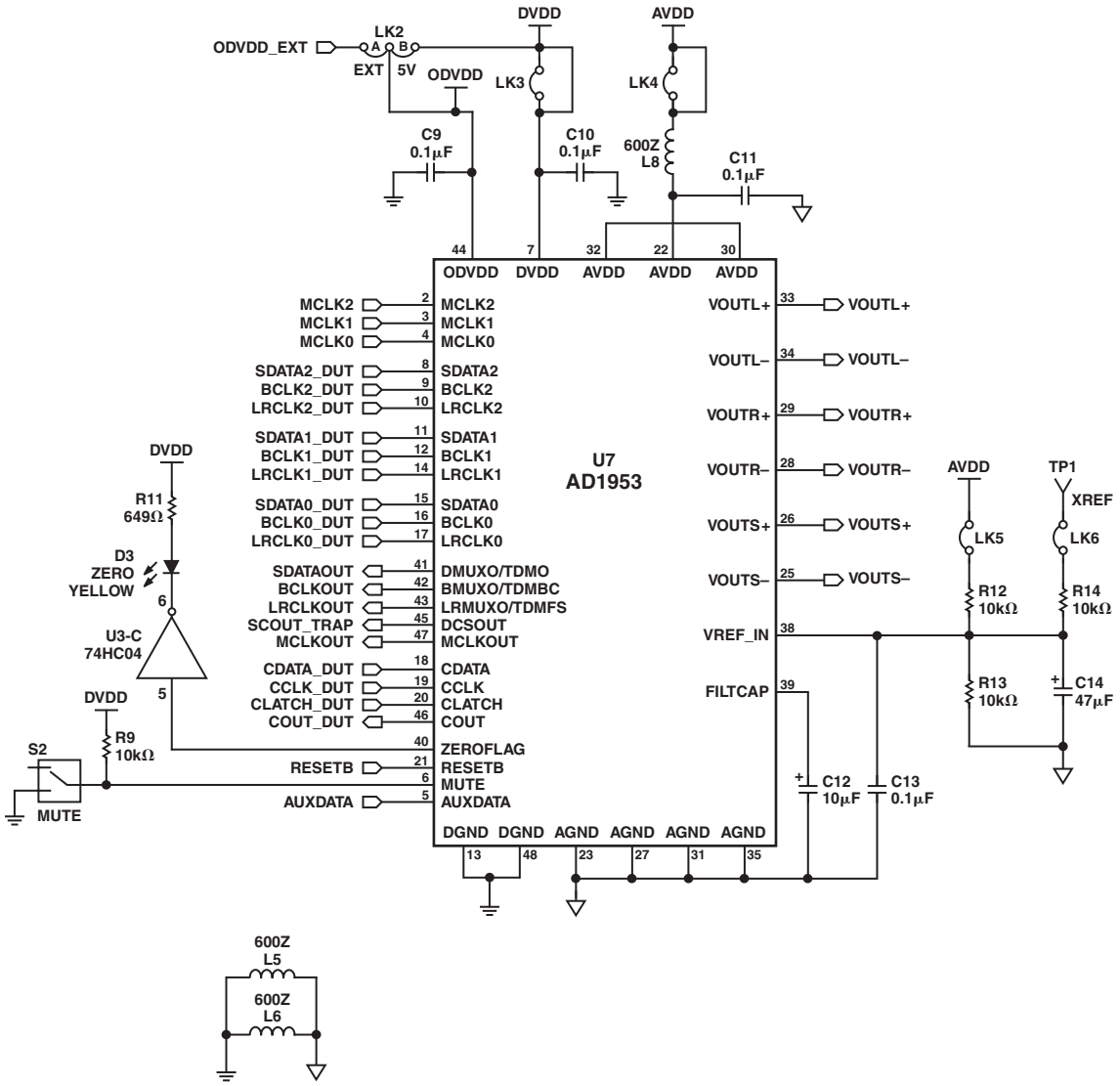

Figure 7. Evaluation Board, DUT

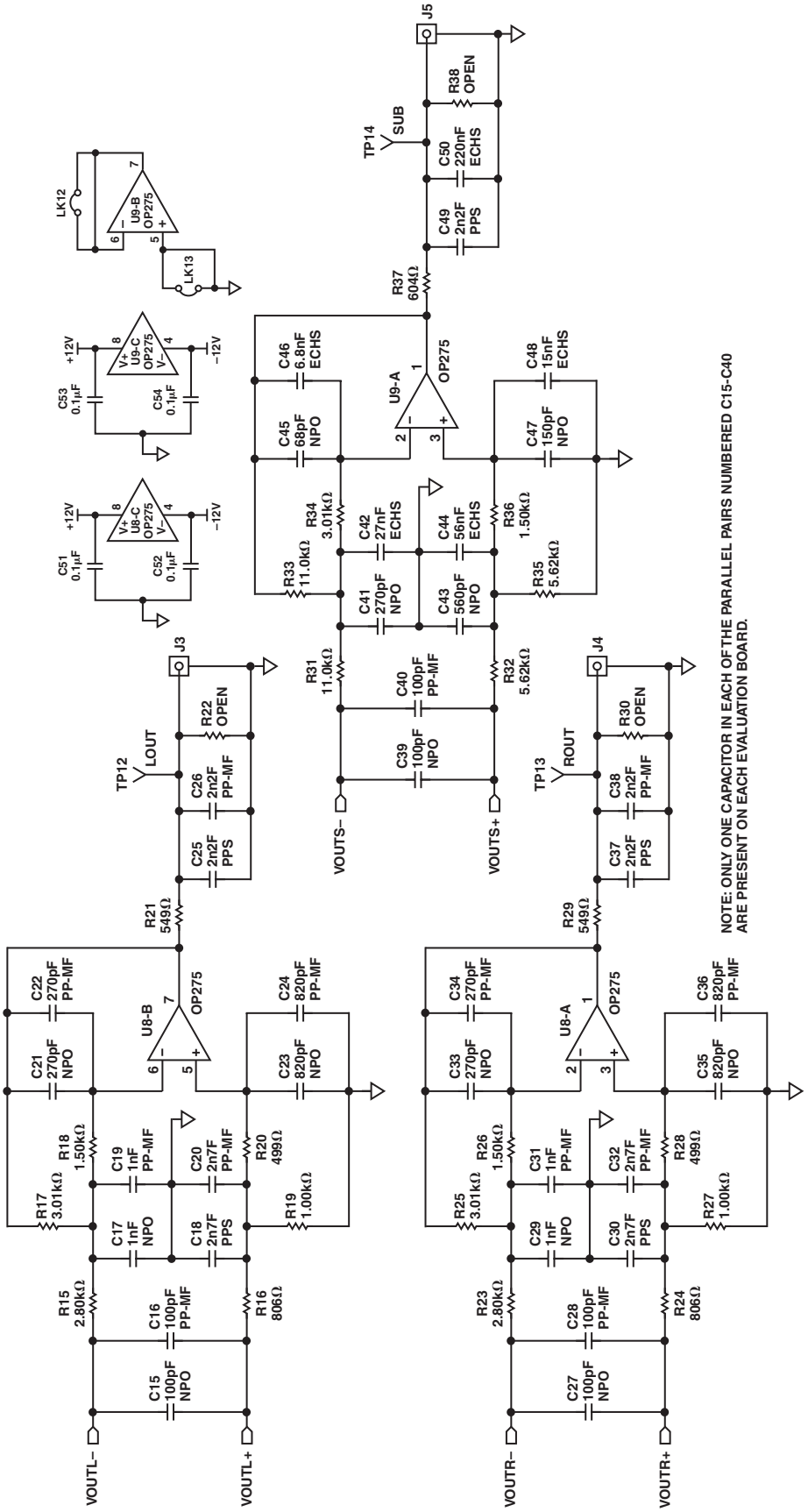

Figure 8. Evaluation Board, Analog Output Section

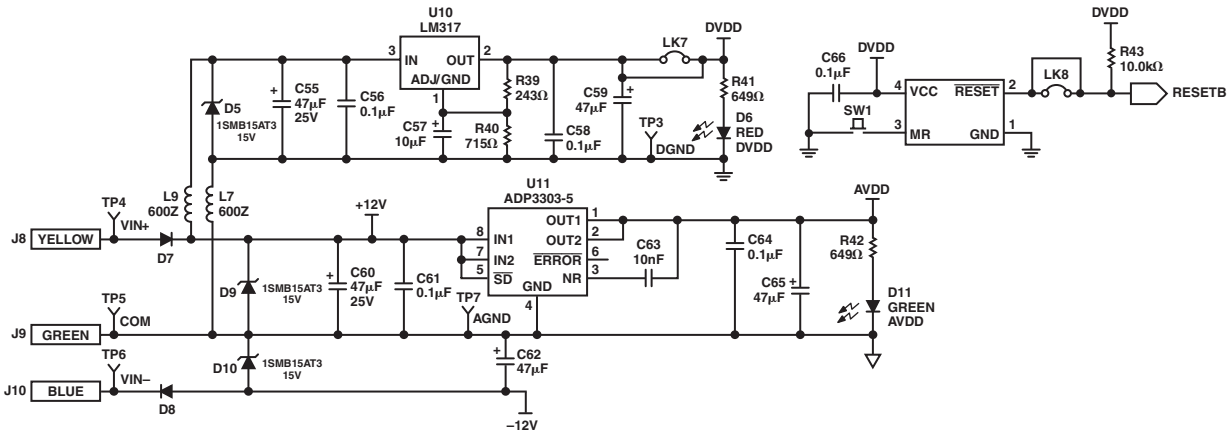

Figure 9. Evaluation Board, Power Supply and Reset Generator Sections

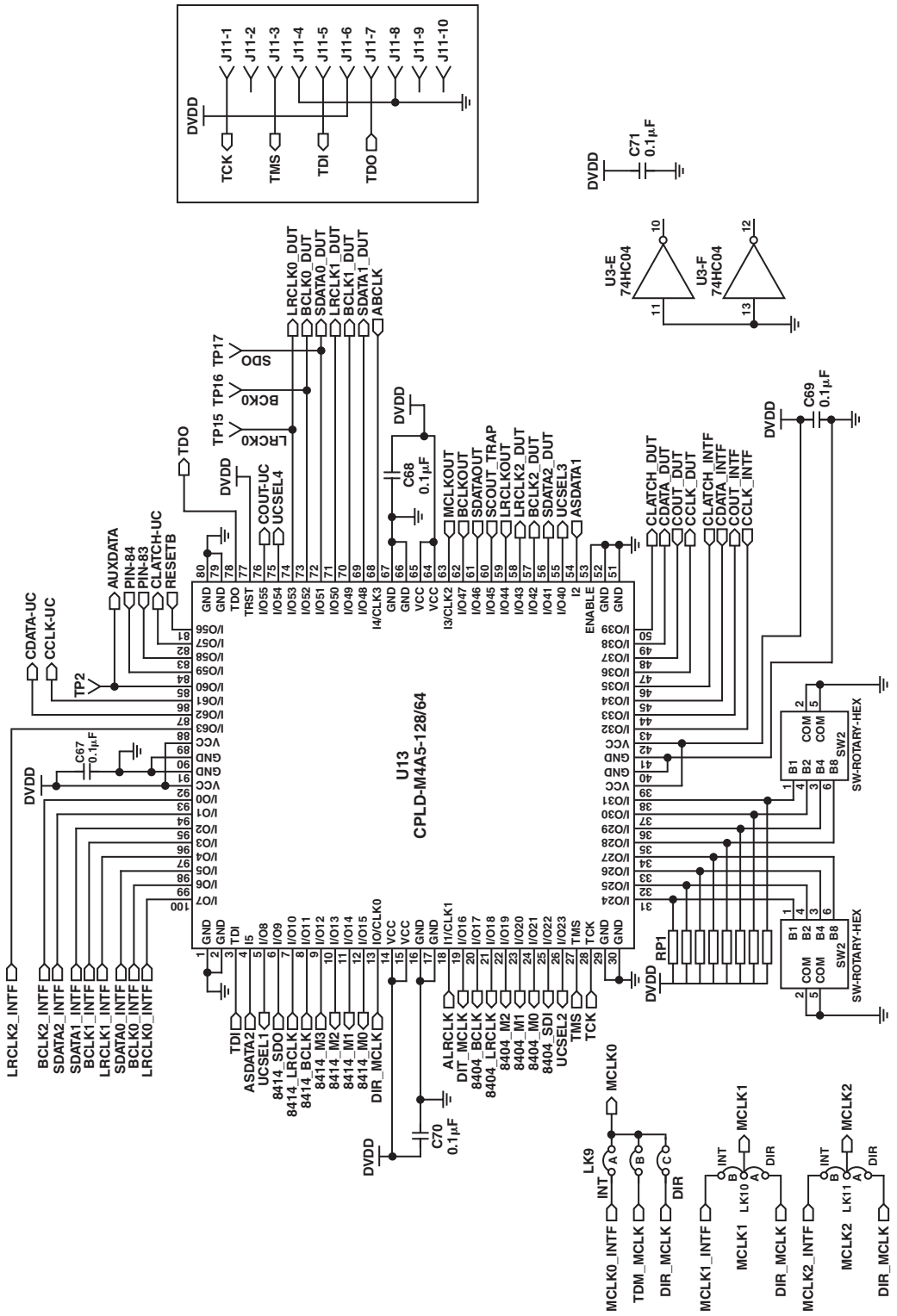

Figure 10. Evaluation Board, CPLD Section

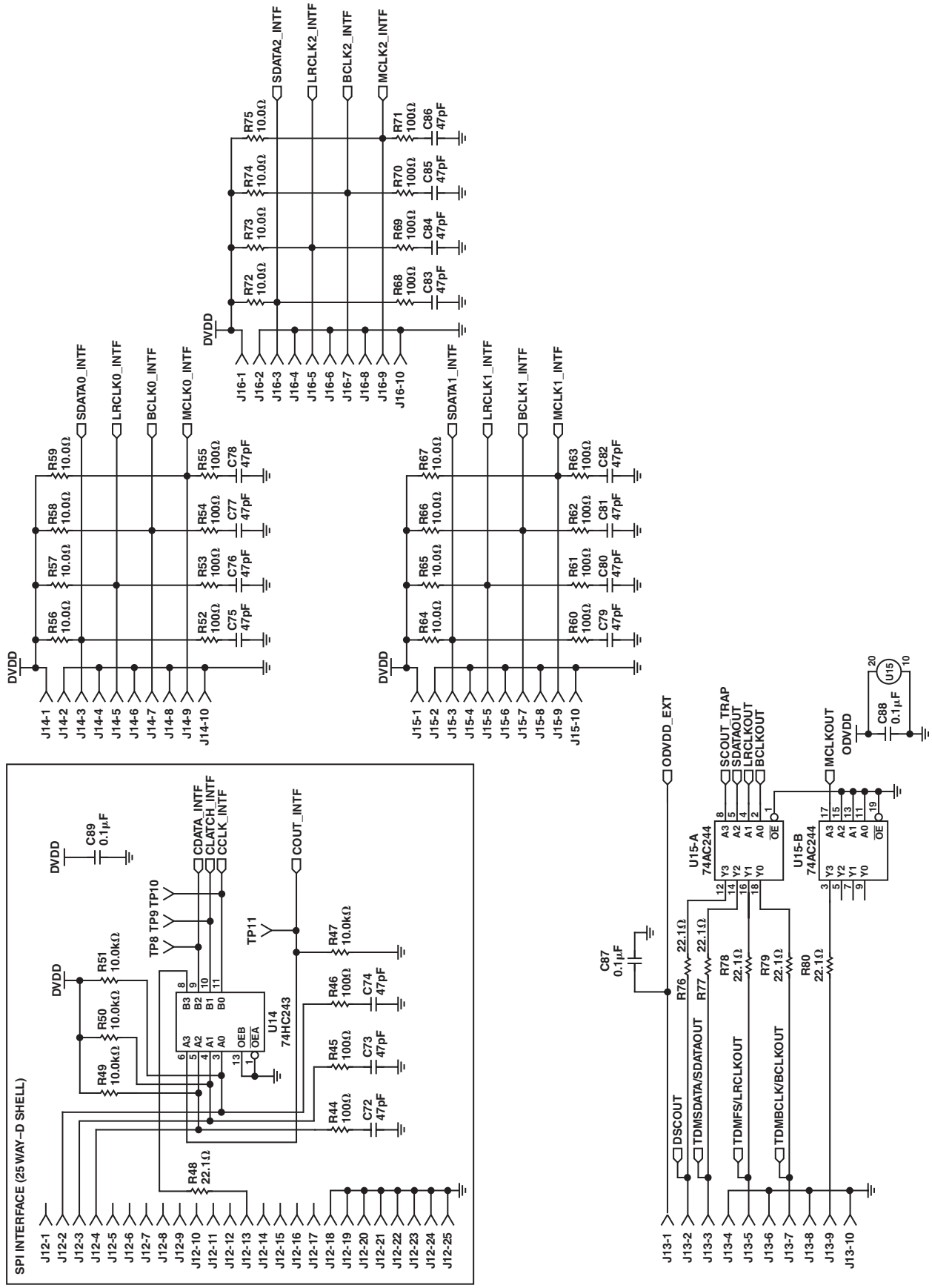

Figure 11. Evaluation Board, External Digital Interface

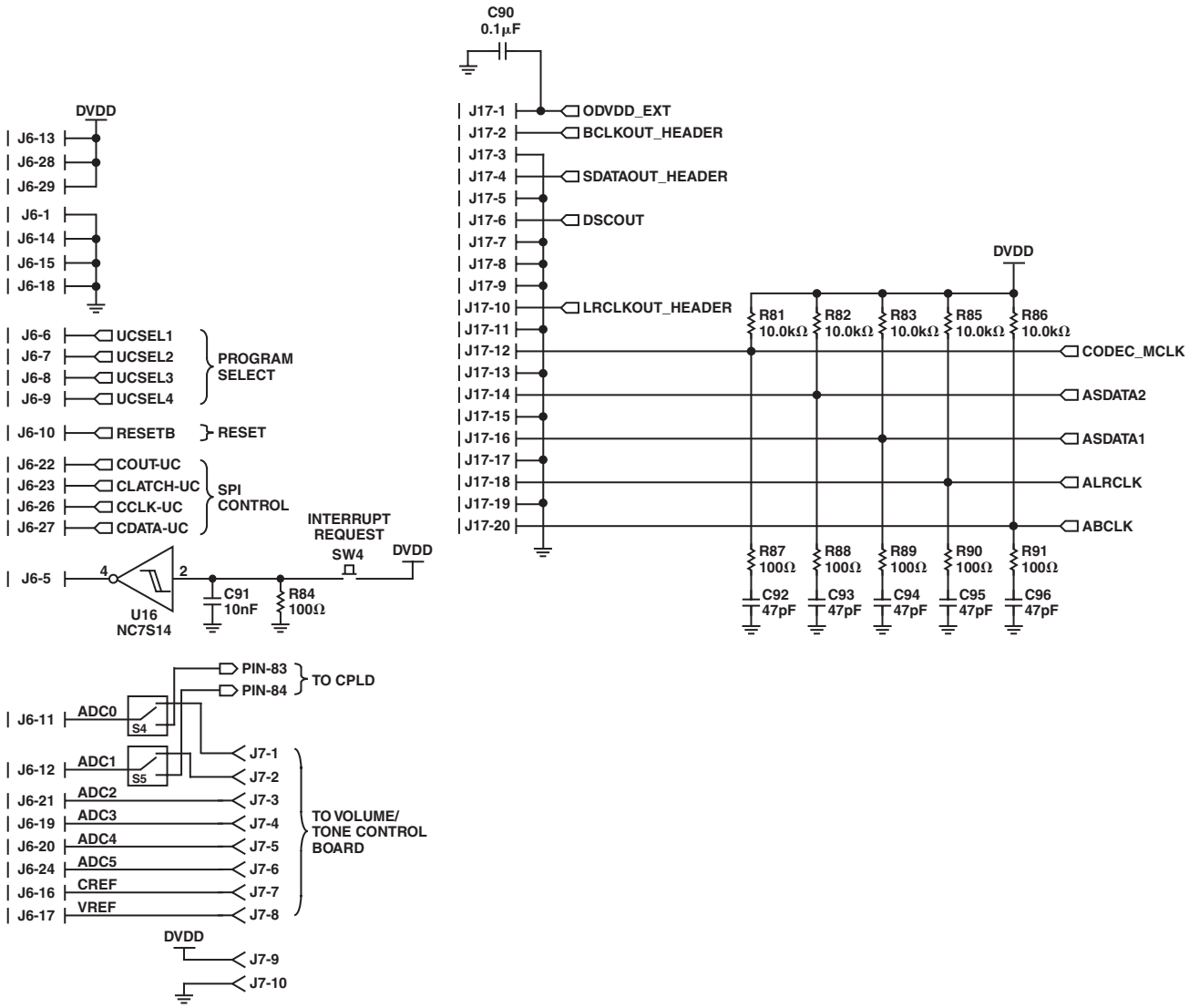

Figure 12. Evaluation Board, ADuC812S Interface

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