Differential Receiver Evaluation Board

EVAL-ADDIFFRX

INTRODUCTION

An Analog Devices differential receiver evaluation board makes it easy for designers to get quick performance results for their particular differential receiver application circuits. The board layout is very flexible, and allows for several feedback configurations, common-mode and differential input terminations, reference voltage application, and other circuit features. Most resistors and capacitors are in 1206 packages.

DEVICES COVERED

The board is used for the AD8129 and AD8130.

POWER SUPPLIES

Power is applied to the board through J1, a Molex 22-11-2032 3-pin header. Pin 1 (square footprint) is for the positive supply, Pin 3 is for the negative supply, and Pin 2 is connected to the board's ground plane. Alternatively, looped test points can be used; Test Point TP6 connects to the positive supply and TP7 connects to the negative supply. TP8, TP9, TP10, and TP11 connect to the ground plane.

The board can accommodate single and dual supplies. For single-supply operation, simply connect the negative supply to the ground plane.

It is very important that the power supply pins of the device under test (DUT) have decoupling circuitry. The board layout facilitates this with footprints for a 1206 ceramic capacitor on each supply. For broadband decoupling, it is recommended that two ceramic capacitors be used—one for lower frequencies and one for higher frequencies. To achieve this, two 1206 ceramic capacitors can be stacked on the same footprint. Bulk decoupling is provided by C1 and C3; 10 μF tantalum capacitors are recommended.

FEEDBACK NETWORKS AND INPUT/OUTPUT TERMINATIONS

R5 and R6 comprise the resistive feedback loop that can be returned to ground through R8 or to the reference voltage circuitry, VR1 and C7. Capacitors C5 and C6 are included across the feedback resistor and gain resistor, respectively, to implement first-order frequency response shaping. C6 introduces a pole into the feedback loop, which must be compensated by C5.

A reference voltage can be injected at Pin 4 of the DUT. Using potentiometer VR1, which spans the power supplies, the designer can adjust the reference voltage over a wide range. C7 provides bypassing on the wiper of VR1. A test point, TP5, is provided for monitoring the reference voltage. When VR1 is used, it is important to ensure that JU3 is shorted.

In order to minimize parasitic summing node capacitance, the ground plane has been voided under and around Pin 5 of the DUT and the copper that connects to it.

Differential termination is provided by R3, and common-mode terminations are provided by R1 and R2. C9 and C10 allow optional input ac coupling, and must be shorted across when not used. JU1 provides the means to directly monitor the differential input by using a suitable high impedance differential probe, or to directly short across the differential inputs for test purposes. Standard Berg type headers can be used in JU1. Alternatively, TP2 and TP3, which accommodate looped-type test points, can be used.

Source termination resistor R7 is included on the output to facilitate driving coaxial cables and test equipment. The output signal can be monitored before the source termination resistor at TP4. Since TP4 is the direct amplifier output, any test equipment connected to TP4 will add to the amplifier's capacitive load, and thus diminish phase margin. Extreme care should be exercised when connecting test equipment to TP4.

INPUT/OUTPUT CONNECTORS

The inputs and outputs have edge-mounted SMA connectors for straightforward connection to coaxial cables. Johnson Components part number 142-0701-801, or equivalent, is recommended. On the inputs, TP13 and TP14 provide the option of using straight or right-angle through-hole SMA connectors. They also accommodate coaxial oscilloscope probe test sockets, such as the Berg Electronics 33JR135-1. TP12 provides the same option on the output.

POWER DOWN

Pull-up resistor R4 and jumper JU2 make it easy for the DUT's power-down feature to be asserted. The recommended value for R4 is 1 kΩ. As with JU1, a Berg-type header can be used for JU2.

OTHER COMPONENTS

There may be application circuits where footprints for desired components are not available on the board. In these cases, the user is encouraged to use his or her ingenuity to find ways to include them.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

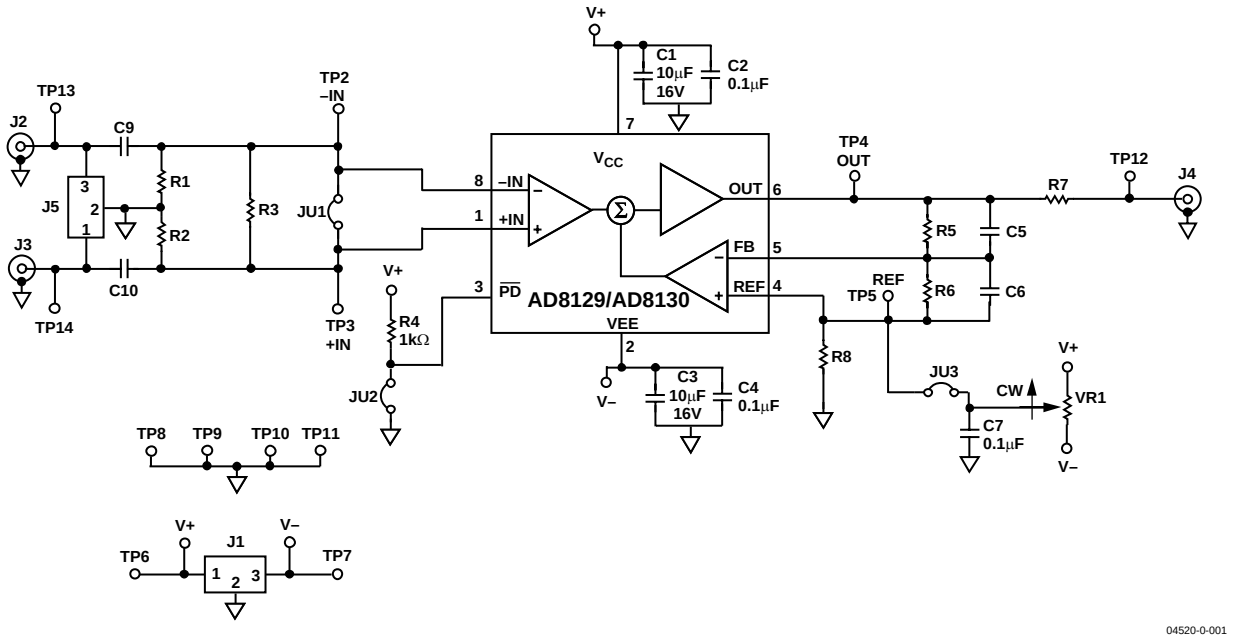

Figure 1. Differential Receiver Evaluation Board Schematic

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Description
EVAL-ADDIFFRX-1R	Differential Driver Evaluation Board (SOIC)
EVAL-ADDIFFRX-1RM	Differential Driver Evaluation Board (MSOP)

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