CS51227DEMO/D

Demonstration Note for CS51227

Enhanced Voltage Mode PWM Controller 5 V to 12 V/1 A Boost Converter

ON Semiconductor®

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DEMONSTRATION NOTE

Description

The CS51227 demo board is configured as a compact 5 V to 12 V/1 A DC–DC converter. The demo board takes advantage of Feed Forward Voltage Mode control, provided by CS51227, to achieve superior line and load regulation. Protection features include pulse–by–pulse current limit and undervoltage lockout (UVLO). The integrated features of the CS51227 allow the designers to use minimum external components for saving cost and board space. The on–board DC and dynamic load facilitates the examination of load regulation and transient response.

Features

- Feed Forward Voltage Mode Control
- Energy Transfer Efficiency Over 85%
- Total of 20 Components and 1.287 × 1.36 inch^2 Board Space
- Pulse–by–Pulse Switch Current Limit and UVLO
- 300 kHz Switching Frequency
- On–Board Load Testing Circuit

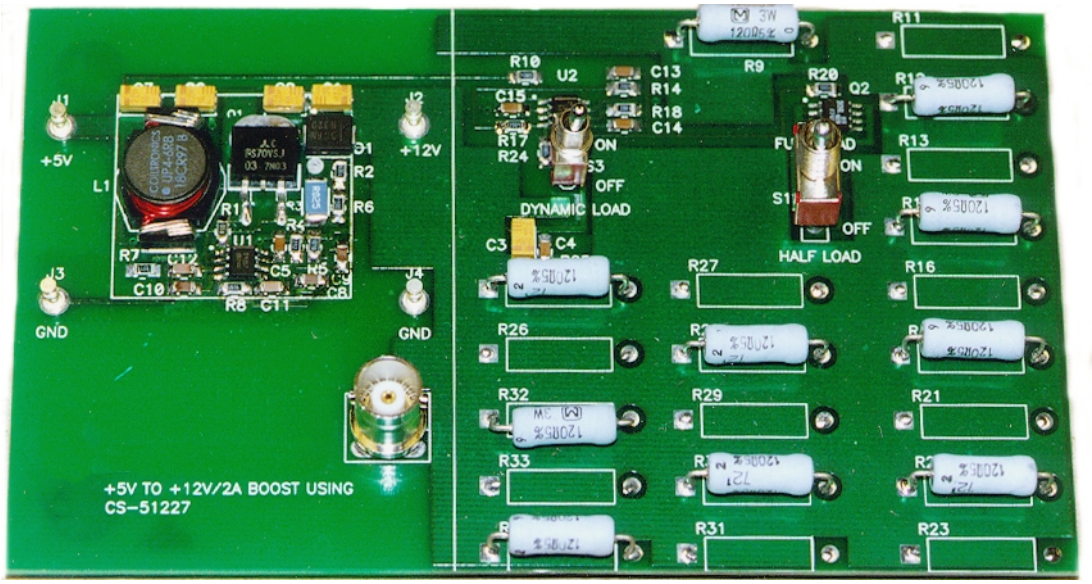


Figure 1. CS51227 Demonstration Board

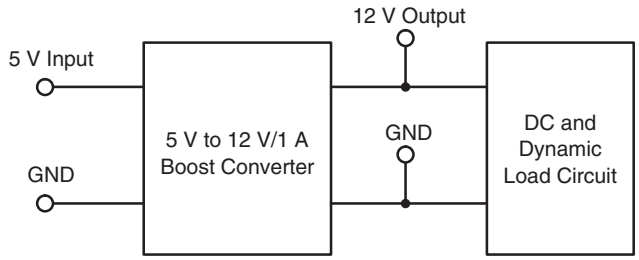


Figure 2. Application Diagram

MAXIMUM RATINGS

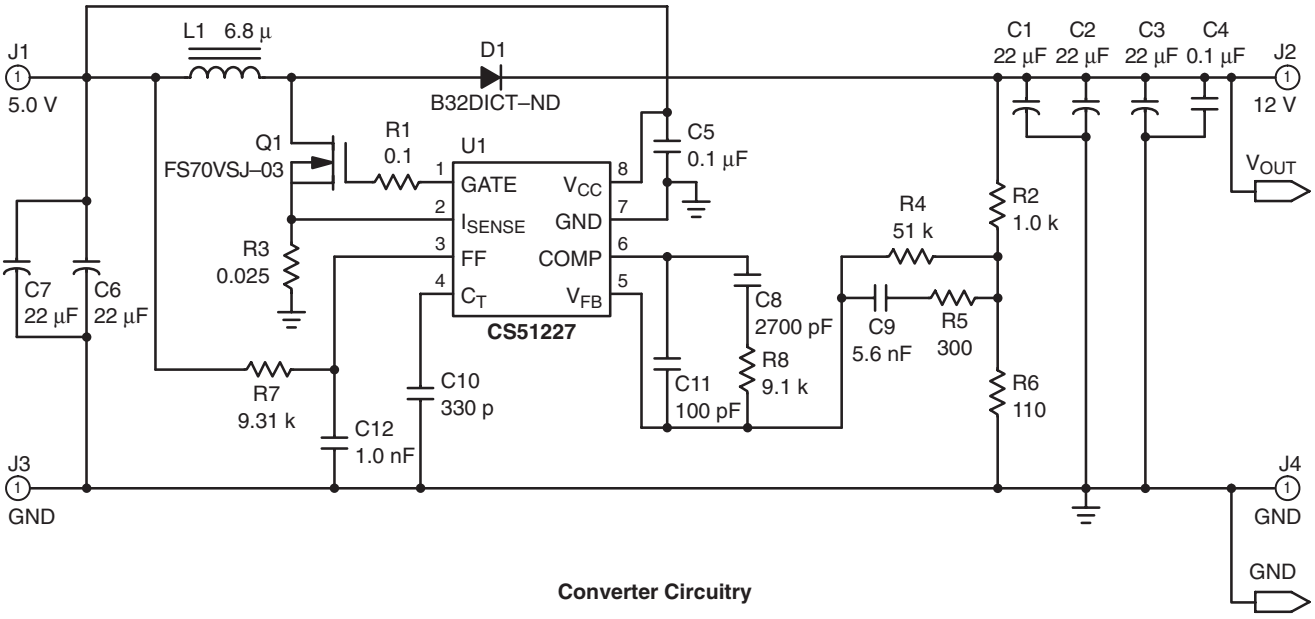
Pin Name	Maximum Voltage	Maximum Current
5 V	+20 V/–0.3 V	4.5 A
GND	NA	4.5 A
12 V	16 V/–0.3 V	1.2 A

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{IN} = 5.0 V, I_{OUT} = 1.0 A, unless otherwise noted)

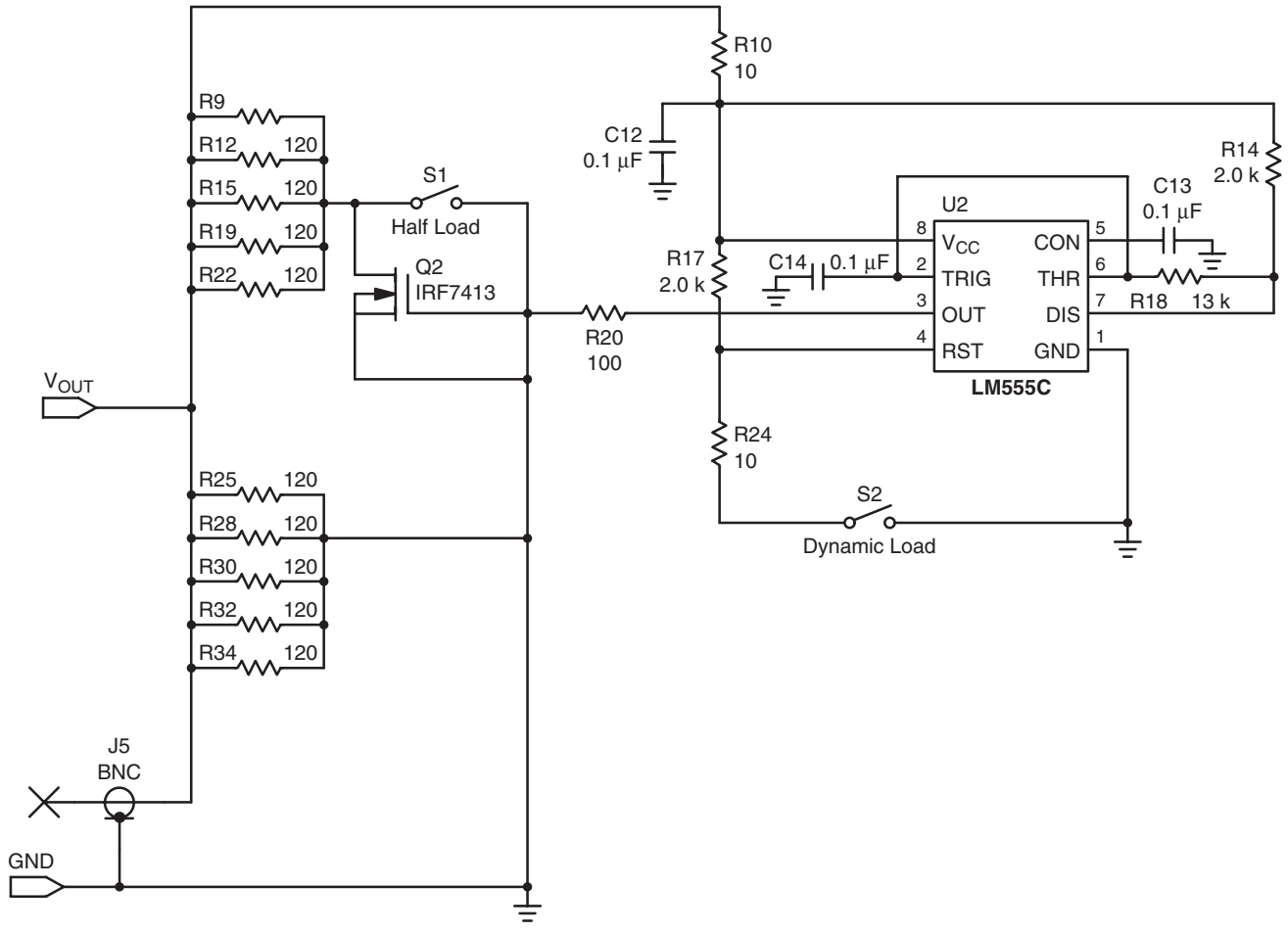
Parameter	Test Conditions	Min	Typ	Max	Unit
Output Specifications					
Voltage Accuracy	–	–	±1.5	±2.0	%
Line Regulation	4.75 V ≤ V_{IN} ≤ 52.5 V	–	0.03	0.05	%
Load Regulation	0.1 A ≤ I_{OUT} ≤ 1.0 A	–	0.3	0.5	%
Ripple and Noise 20 MHz	pk–pk	–	150	300	mV
Transient Response	Half Load to Full Load	–	±1.6	±2.0	%
Transient Response Time	Within ±1%	–	100	200	μs
Minimum Load	–	100	–	–	mA
Input Specifications					
Start Threshold	–	4.4	4.6	4.7	V
Stop Threshold	–	3.2	3.7	4.1	V
General Specifications					
Frequency	Measure at C_T pin	270	300	330	kHz
Efficiency	0.5 A ≤ I_{OUT} ≤ 1.0 A	83	86.5	89	%

PIN DESCRIPTION

Reference	Symbol	Description
J1	+5 V	Input voltage pin. Apply a voltage between 4.75 V to 5.25 V.
J2	+12 V	Output voltage pin. The maximum output current is 1.2 A.
J3	GND	Input ground.
J4	GND	Output ground.



Converter Circuitry



Test Circuitry

Figure 3. Demonstration Board Schematic

OPERATION GUIDELINES

The CS51227 Demonstration Board is configured to demonstrate the performance features of the CS51227 Enhanced Voltage Mode Controller.

- The voltage output terminal J5 is a female BNC connector, located near the load resistors. Using a standard BNC coax cable, the output voltage waveform can be observed on an oscilloscope during DC and AC load operation.
- The Load Switch S1 is SPDT type and is located on the right side of the board. The switch can be used to turn to half (0.5 A) and full (1 A) load.
- The Dynamic Load Switch S3 located on the upper middle of the board is used to enable the 555 timer circuit which is in parallel with Load Switch S1. When the Load Switch S1 is at Half Load position, turning on S3 will switch the load between half load and full load. This demonstrates the short reaction time and efficient load handling of the circuit.

THEORY OF OPERATION

Boost DC–DC Converter

Boost converter is often used to generate an output voltage greater than the input voltage. As shown in the schematic, when the switch Q1 is turned on, the input voltage is applied across the inductor L1 causing the inductor current to increase linearly. The diode D1 is reverse biased and output current is provided only by the output capacitors C1–4. When the switch Q1 is turned off, the diode D1 is forward biased and conducts the inductor current to the output. The voltage on the switch Q1 is approximately equal to output voltage. When the turn off time is expired, the power switch turns on again and starts a new switching cycle.

Feed Forward Voltage Mode Control

In a conventional voltage mode control, the ramp signal has fixed rising and falling slope. The feedback signal is deriveed solely from the output voltage. Consequently, voltage mode control has inferior line regulation and audio susceptibility. In feed forward voltage mode control, the ramp signal is generated from the input line. Therefore the ramp of the slope varies with the input voltage. At the start of each switch cycle, the FF pin capacitor C12 is charged through the resistor R7 which is connected to the 5 V line. Meanwhile, the Gate output is turned on to drive the power switch Q1. When the FF pin voltage reaches the error amplifier output V_{COMP} voltage, the PWM comparator turns off the Gate, which in turn opens the Q1. Simultaneously, C12 is quickly discharged to 0.3 V. Overall, the dynamics of the duty cycle is controlled by both input and output voltages. The output voltage is divided down through the resistor network of R2 and R6 and fed to the V_{FB} pin, the inverting input of the error amplifier. R4, C9, R5, C8, R8 and C11 constitute a frequency compensation network which ensures the loop stability and voltage regulation.

Pulse–By–Pulse Current Limit

The switching current is sensed at the I_{SENSE} pin through the resistor R3. When the I_{SENSE} pin voltage exceeds the threshold voltage of 0.3 V, the Gate output will be turned off for the remaining of the switching cycle. This feature protects the circuit during startup and overload conditions. During the short–circuit condition, the current limit prevent the IC from excessive thermal stress. However, the inductor L1 and diode D1 are still subject to detrimental current stress. Extra protecting circuits have to be implemented to limit the input current, such as using a fuse in series with input power source.

DESIGN GUIDELINES

Design Specification

V_{IN} = 4.75 V to 5.25 V, assuming a 5% input supply
V_{OUT} = 12 V ±2% @ 0.5 A to 1 A
$V_{OUT(RIPPLE)} \leq$ 300 mV
Switching Frequency = 300 kHz

Power Stage Design

Select Inductor and Input/Output Capacitors

The resonant frequency of the LC network f_{LC} is selected at one fifth of the switching frequency to restrict switching noise. Since

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} = f_{SW}/50 = 6\ k \quad (1)$$

The design uses three 22 μF tantalum capacitors in parallel to achieve low effective series resistor (ESR). The inductor value can then be calculated from

$$L = \frac{1}{(2\pi f_{LC})^2 C} = 10\ \mu H \quad (2)$$

The design chooses 6.8 μH for the inductor value.

For a boost converter in a continuous conduction mode (CCM), the duty cycle D is given by

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = 58.3\% \quad (3)$$

The peak to peak inductor current ripple has an expression of

$$I_{L(p-p)} = \frac{V_{IN} \cdot D}{f_{SW} \cdot L} = 1.4\ A \quad (4)$$

The maximum DC input current can be calculated as

$$I_{IN(MAX)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN(MIN)}} \cdot 1.2 = 3\ A \quad (5)$$

where

$I_{OUT(MAX)}$ = maximum output current

$V_{IN(MIN)}$ = minimum input current

1.2 = scale factor assuming 85% energy transfer efficiency

The peak inductor current is

$$I_{L(PEAK)} = I_{IN(MAX)} + \frac{1}{2} I_{L(p-p)} = 3.7\ A \quad (6)$$

When choosing a magnetic component, one has to consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. The peak inductor current given in Equation 5 should not cause inductor saturation and DC current given by Equation 4 should not exceed the maximum DC current rating of the inductor. In some data sheets, the RMS current rating is listed instead. For boost circuits operating in CCM, the inductor DC current is close to the RMS current if the ripple current is small compared to the DC current.

The above equations can also be referenced to select the value of the inductor based on the tolerance of the ripple current in the circuits. A small ripple current provides the benefit of small input capacitors and greater output current capability. The core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometry, such as a toroid, provides a closed magnetic loop to prevent EMI. This design uses a barrel shaped core made of power iron material for its cost and availability.

In boost circuits, the inductor becomes part of the input filter. In CCM, the input current waveform is triangular and does not contain a large pulsed current. This reduces the requirements imposed on the input capacitor selection. During CCM, the peak to peak inductor ripple current is given in Equation 3. The product of this inductor ripple current and the input capacitor's ESR determines the $V_{IN(RIPPLE)}$. In this design, two 22 μF tantalum capacitors are paralleled to further reduce the ESR. The total input ripple voltage can be calculated

$$V_{IN(RIPPLE)} = I_{L(p-p)} \cdot ESR = 1.4\ A \cdot 100\ m\Omega = 140\ mV \quad (7)$$

The output ripple voltage comes from two major sources, namely, capacitor ESR and the charging/discharging of the capacitors. In a boost circuit, when the power switch turns off, the output capacitors and their associated ESR experiences a current determined by the inductor current minus the output current. This current generates an instant voltage rise/fall. When the power switch turns on, inductor current is shunted to the ground and output current, I_{OUT}, discharges the output capacitors. As shown in Figure 5 and Figure 6 in the Typical Performance Characteristics, ESR is the major cause of the output ripple in this design. Therefore, the output capacitors are selected to fulfill the requirement of the output ripple on the full load condition. The maximum ESR of the output capacitors can be derived from

$$ESR = \frac{V_{OUT(RIPPLE)}}{I_{L(PEAK)}} = \frac{300\ mV}{3.7\ A} = 81\ m\Omega \quad (8)$$

Here we use three 200 mΩ low ESR tantalum capacitors in parallel.

The operation switches to the discontinuous conduction mode (DCM) when the load resistor R_L meets following condition,

$$R_L < \frac{2(L)(f_{SW})}{D(1-D)^2} \quad (9)$$

In the discontinuous mode, the inductor current rises linearly from 0 A at the beginning of each switching cycle. Current falls to zero during the time when Q1 turns off and D1 is forward biased. In DCM, the duty cycle is equal to

$$D = \sqrt{\frac{2(L)(f_{SW})}{R_L} \frac{V_{OUT}(V_{OUT} - V_{IN})}{V_{IN}^2}} \quad (10)$$

Equation 3 can be used to calculated inductor peak current and ripple current. Equation 6 is still applicable for input ripple voltage calculation.

Select Switching Devices

In selecting MOSFET as the active switch, the DC input current given in Equation 4 is calculated for specified maximum output current and minimum DC input voltage. Then for this current, a MOSFET of R_{DS} (drain–to–source on resistance) is chosen so that the on drain–to–source voltage ($R_{DS} \cdot I_{IN(MAX)}$) is a small percentage (usually no more than 2 percent) of the minimum supply voltage so as to rob no more than 2 percent of the transformer's minimum primary voltage. In selecting a device with a desired R_{DS}, it should be remembered that the data sheet gives it at a case temperature of 25°C. Also noteworthy is the fairly large variation of R_{DS} with temperature. The MOSFET power dissipation at maximum output current, including both conduction and switching losses, are given by

$$P_{MOSFET} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} (I_{MAX})^2(1 + \delta)R_{DS(on)} + K(V_{OUT})^2(I_{MAX})(C_{RSS})(F_S) \quad (11)$$

where δ is the temperature dependency of $R_{DS(on)}$ and K is a constant inversely related to the gate drive current. The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(on)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant K = 1.7 can used to estimate the contributions of the switching loss.

The selected MOSFET FS70VSJ–03 has maximum $R_{DS(on)}$ of 22 mΩ @ V_{GS} = 4 V and C_{RSS} of 450 pF. Therefore, the total power loss of the MOSFET can be calculated based on Equation 8 and is equal to 0.046 W at 25°C.

In a boost converter, the maximum voltage applied to the MOSFET is equal to the output voltage plus the forward voltage drop on the power diode.

Diode Selection

In a boost converter, the diode conducts inductor current when the power switch is turned off. The diode DC current is equal to the output current. So select the diode has current rating twice the maximum output current. The breakdown voltage of the diode has to be greater than the output voltage. The Schottky barrier diodes are often favored for their low forward voltage drop and fast reverse recovery time. The selected Schottky diode has current rating of 3 A and maximum peak reverse voltage of 20 V. The power dissipation on the diode is equal to

$$W_D = (I_{OUT})(V_F) \quad (12)$$

where V_F is diode forward voltage, which is equal to 0.5 V for the selected part.

Feedback Control Design

Boost Converters have a duty cycle to output small signal gain expressed as:

$$\frac{\hat{v}_{OUT}}{\hat{d}} = \frac{V_{OUT}}{1-D}\,\frac{(1 + S/\omega_{ESR})\,(1 - S/\omega_{LR})}{1 + \frac{2\zeta}{\omega_{OUT}}\,s + \frac{1}{\omega_{OUT}^2}\,s^2} \quad (13)$$

$$\omega_{ESR} = \frac{1}{ESR \cdot C} \approx 2\pi \cdot 24\ kHz \quad (14)$$

$$\omega_{LR} = \frac{R_L \cdot (1-D)^2}{L} = 2\pi \cdot 50\ kHz$$

$$\omega_{OUT} = \frac{1-D}{\sqrt{LC}} = 2\pi \cdot 24\ kHz$$

$$\zeta = \frac{1}{2}\left(\sqrt{\frac{C}{L}}\,ESR(1-D) + \frac{\sqrt{\frac{L}{C}}}{R_L(1-D)}\right)$$

where

R_L = load resistance

ω_{ESR} = ESR zero provided by the ESR of the output capacitors

ω_{LR} = Right half plane zero inherent in the boost topology

ω_{OUT} = Resonant frequency of the output filter in a boost converter.

ζ = damp factor of the LC resonant tank.

To compensate this forward stage, the feedback network has to provide three frequency–domain requirements, namely,

1. high DC gain to provide good DC load and line regulation
2. high loop bandwidth to guarantee fast transient response
3. adequate phase margin at cross–over frequency to ensure system stability.

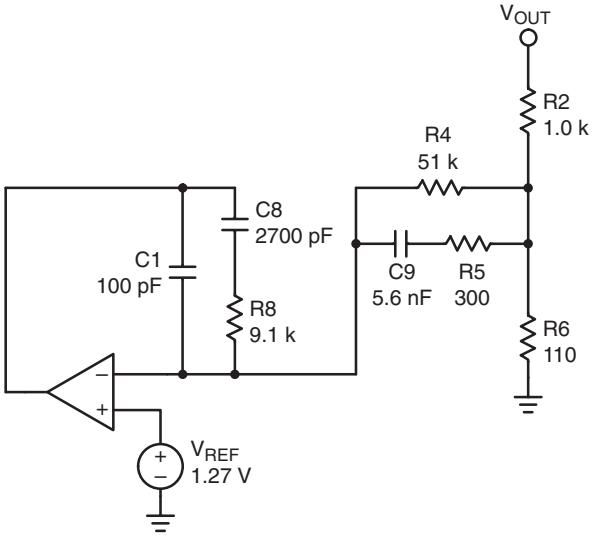


Figure 4. The Feedback Network of the CS51227 Demo Board

The compensation network design is centered around the error amplifier, which is shown in the Figure 4. The poles and zeros provided by this network are listed in the Equation 8, where fz1 and fz2 are placed near the LC resonant frequency ω_{OUT} to provide adequate phase margin. The frequency of pole fp2 is designed to counteract ω_{ESR} and ω_{LR} as it cuts down the gain once the loop gain crosses over the 0 db. The frequency of fp1 is equal to half of the switching frequency to limit the switching noises. The consequent loop frequency responses are shown in Figure 8 and Figure 9. It is noticed that the system has a cross–over frequency of 6 kHz and phase margin over 50°.

$$fz1 = \frac{1}{2\pi C8R8} = 6.5\ kHz \quad (15)$$

$$fz2 = \frac{1}{2\pi C9R4} = 557\ Hz$$

$$fp1 = \frac{1}{2\pi C11R8} = 175\ kHz$$

$$fp2 = \frac{1}{2\pi C9(R5 + R6 \parallel R2)} = 71\ kHz$$

Current Limit Design

Current limit resistor R3 is placed in series with the power switch Q1 to sense the switching current. The resistor value is selected to provide current limit threshold, which is given by

$$I_{LIMIT} = \frac{0.3}{R3} = 12\ A \quad (16)$$

When high efficiency is required, a current sense transformer can be used to monitor the current at minimum power loss.

Feed Forward Design

In this design, R7 and C12 are selected to make the COMP pin voltage stay at 1.5 V during the steady–state operation. Placing the error amplifier output at the center of its operation range provides the error amplifier with the most wide dynamic range when the COMP pin swings either high or low due to load or line variation. The R7 and C12 will have the time constant calculated by the following,

$$R7 \cdot C12 = (V_{IN})(T_S)\frac{V_{OUT} - V_{IN}}{1.2(V_{OUT})} \quad (17)$$

where t_S = switching period.

In this design, R7 and C12 are picked at 9.31 k and 1 nF respectively to satisfy the above restriction.

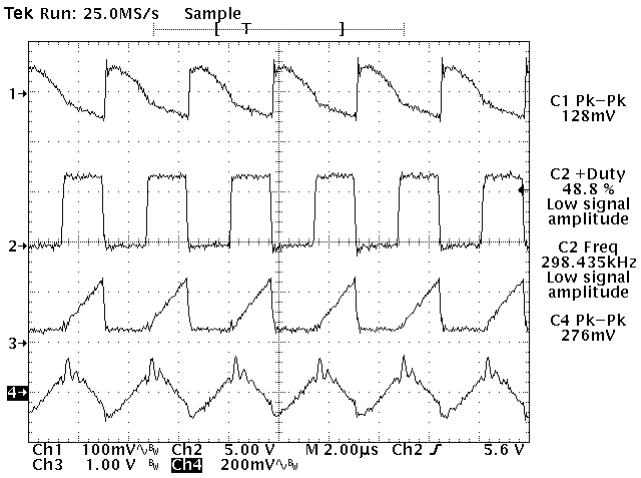
Switch Frequency Selection

The switching frequency is programmed by connecting a capacitor to the C_T pin. The capacitor at C_T pin is charged/discharged between 1 V and 2 V. The charge current is 100 μA, while the discharge current is 900 μA. For an intended switching frequency f_S, the C_T pin capacitor should be equal to

$$C_T = \frac{9e - 5}{f_S} \quad (18)$$

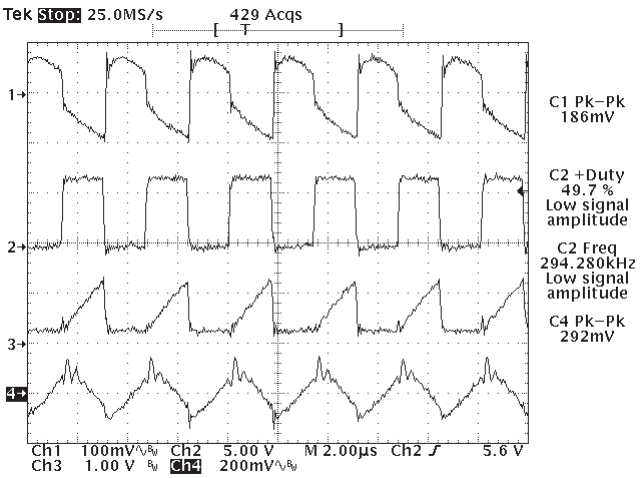
For switching frequency of 300 kHz, Equation 14 gives C_T of 300 pF and 330 pF is used in the design.

TYPICAL PERFORMANCE CHARACTERISTICS



Ch1: Output Ripple Ch2: Gate Signal Ch3: FF Pin Voltage
Ch4: Input Ripple

Figure 5. Steady–State Operation at Half Load



Ch1: Output Ripple Ch2: Gate Signal Ch3: FF Pin Voltage
Ch4: Input Ripple

Figure 6. Steady–State Operation at Full Load

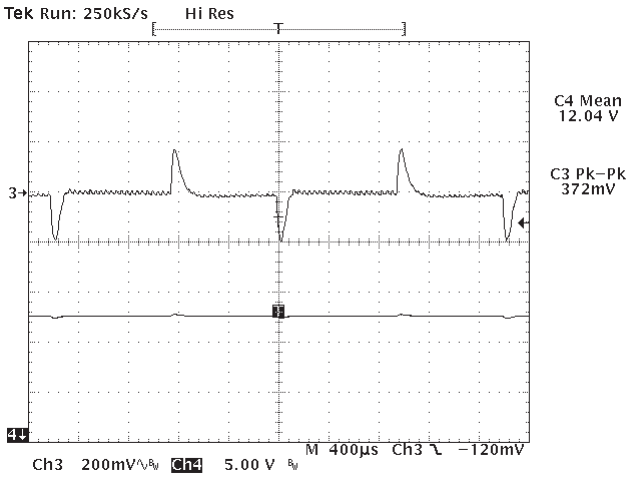


Figure 7. Load Transient Response Between Half Load and Full Load

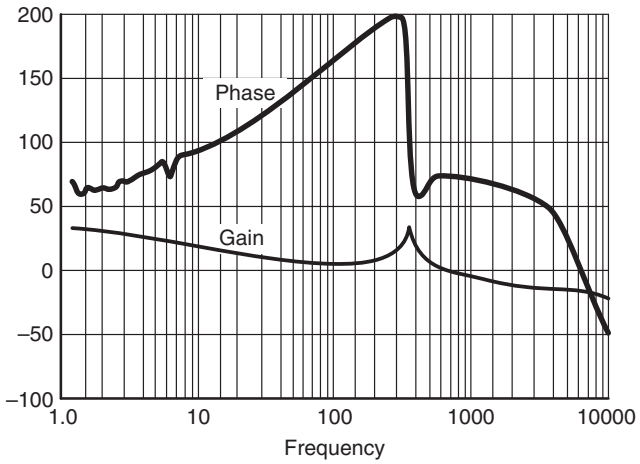


Figure 8. Loop Frequency Response at Full Load

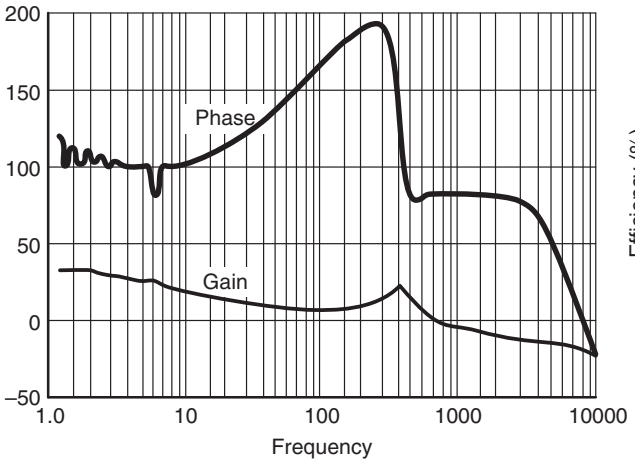


Figure 9. Loop Frequency Response at Half Load

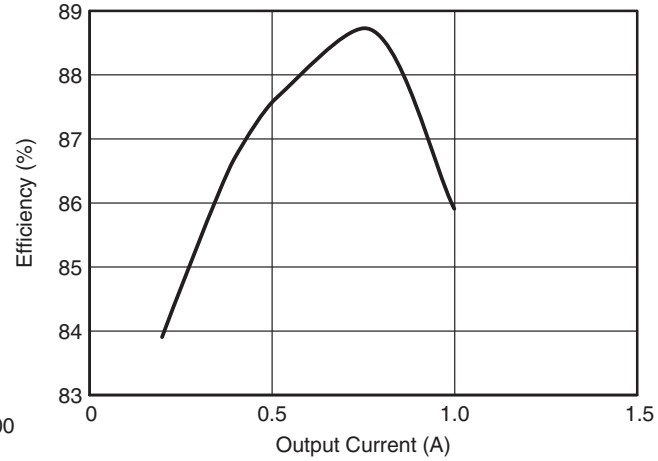


Figure 10. Energy Transfer Efficiency vs Output Current, V_{IN} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

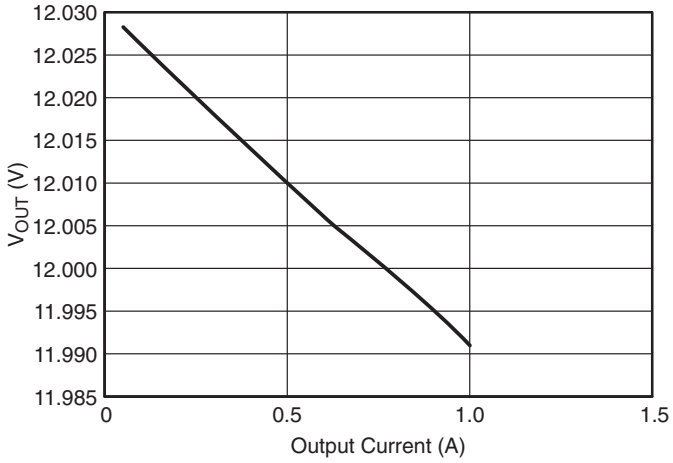


Figure 11. CS51227 Demo Board Load Regulation

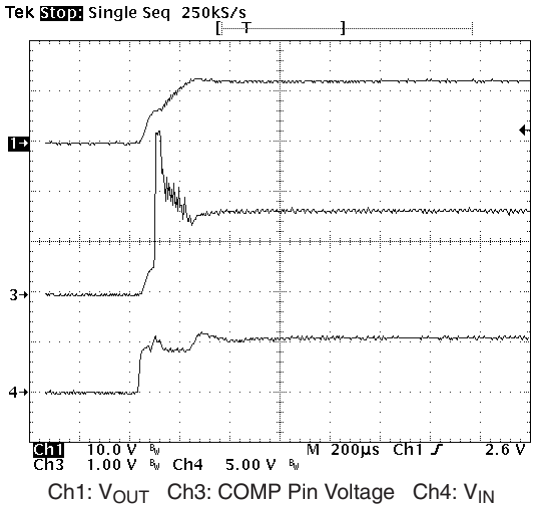


Figure 12. Start–Up Waveform Measured at Half Load with a Fast Rising Input Voltage

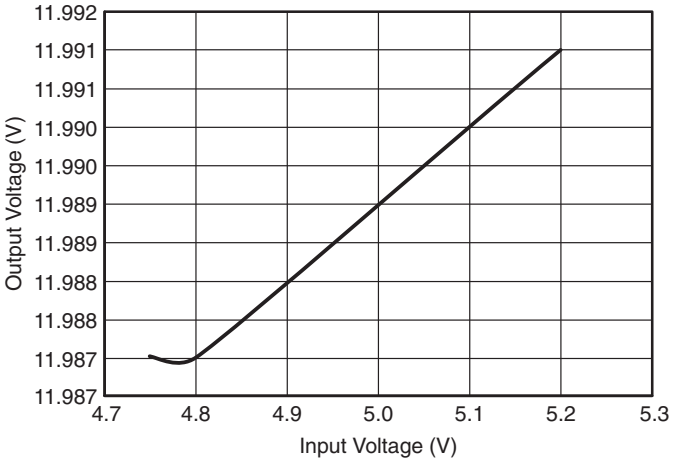


Figure 13. CS51227 Demo Board Line Regulation Measured at Half Load

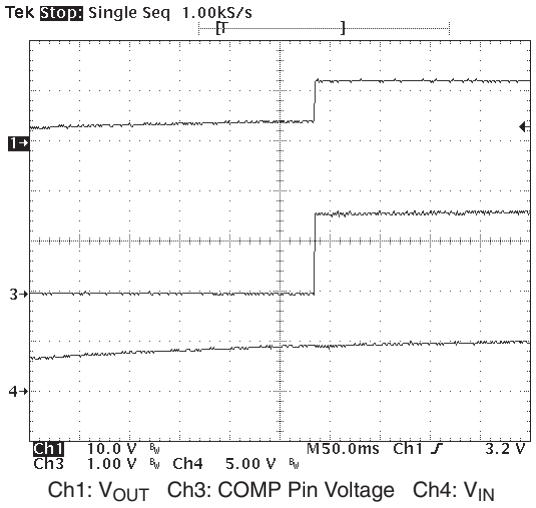


Figure 14. Start–Up Waveform Measured at Half Load with a Slow Rising Input Voltage

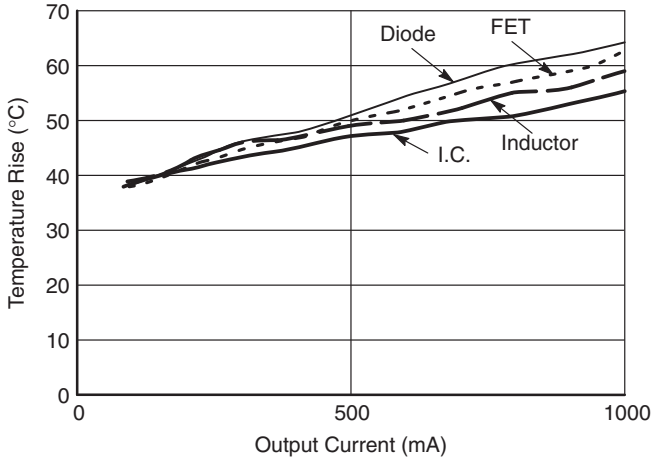


Figure 15. Component Temperature Rise vs Output Current, Tested at Room Temperature

BILL OF MATERIALS

Qty.	Ref. Des	Description	Pkg.	Manufacturer	Distributor	Distr./Man. PN	Distr./Man. Phone
5	C1, C2, C3, C6, C7	22 μF	C	Avx	Future Electronics	TPSC226K016R0375	1–800–444–0050
5	C4, C5, C12, C13, C14	0.1 μF	1206	Panasonic	Digi–Key	PCC104BCT–ND	1–800–344–4539
1	C8	0.047 μF	1206	Panasonic	Digi–Key	PCC473BCT–ND	1–800–344–4539
1	C9	5.6 nF	1206	Panasonic	Digi–Key	PCC5R6CCT–ND	1–800–344–4539
1	C10	330 pF	1206	Panasonic	Digi–Key	PCC331BCT–ND	1–800–344–4539
1	C11	100 pF	1206	Panasonic	Digi–Key	PCC101CCT–ND	1–800–344–4539
1	C12	1.0 nF	1206	Panasonic	Digi–Key	PCC102CCT–ND	1–800–344–4539
1	D1	Diode	SMC	Vishay	Digi–Key	B320DICT–ND	1–800–344–4539
1	J1, J2, J3, J4	Turret Pin	Turret	NA	Newark	40F6023	1–800–463–9275
1	J5	BNC	NA	Multicomp	Newark	583–558	1–800–463–9275
1	L1	6.8 μH	DRUMCORE	Coiltronics	Coiltronics	UP4–6R8	1–561–241–7876
1	Q1	MOSFET	D^2PAK	Mitsubishi	Richardson Electronics	FS70VSJ–03	1–978–657–5900
1	Q2	IRF7413	SO–8	IR	Digi–Key	IRF7413–ND	1–800–344–4539
1	R1	0.1 Ω	1206	Panasonic	Digi–Key	P.10PCT–ND	1–800–344–4539
1	R2	23.7 kΩ	1206	Panasonic	Digi–Key	P23.7KFCT–ND	1–800–344–4539
1	R3	0.025 Ω	NA	Panasonic	Newark	96F7806	1–800–344–4539
1	R4	51 kΩ	1206	Panasonic	Digi–Key	P51.1K	1–800–344–4539
1	R5	300 Ω	1206	Panasonic	Digi–Key	P301FCT–ND	1–800–344–4539
1	R6	2.7 kΩ	1206	Panasonic	Digi–Key	P2.74KFCT–ND	1–800–344–4539
1	R7	9.31 kΩ	1206	Panasonic	Digi–Key	P9.31KFCT–ND	1–800–344–4539
1	R8	9.1 kΩ	1206	Panasonic	Digi–Key	P9.09KFCT–ND	1–800–344–4539
10	R9, R12, R15, R19, R22, R25, R28, R30, R32, R34	120 Ω	3 W	Panasonic/ Yageo	Digi–Key	P120W–3BK–ND	1–800–344–4539
2	R24, R10	10 Ω	1206	Panasonic	Digi–Key	P10.0FCT–ND	1–800–344–4539
2	R17, R14	2.0 kΩ	1206	Panasonic	Digi–Key	P2.00KFCT–ND	1–800–344–4539
1	R18	13 kΩ	1206	Panasonic	Digi–Key	P13.0KFCT–ND	1–800–344–4539
1	R20	100 Ω	1206	Panasonic	Digi–Key	P100FCT–ND	1–800–344–4539
1	S1	SPDT	NA	C+K	Digi–Key	CKN1004–ND	1–800–344–4539
1	S2	SPDT	NA	C+K	Digi–Key	CKN1091–ND	1–800–344–4539
1	U1	CS51227	SO–8	ON Semiconductor	ON Semiconductor	CS51227	1–800–282–9855
1	U2	555 Timer	SO–8	National Semiconductor	Digi–Key	LMC555CN–ND	1–800–344–4539

DEMO BOARD LAYOUT

1:1 IMAGE

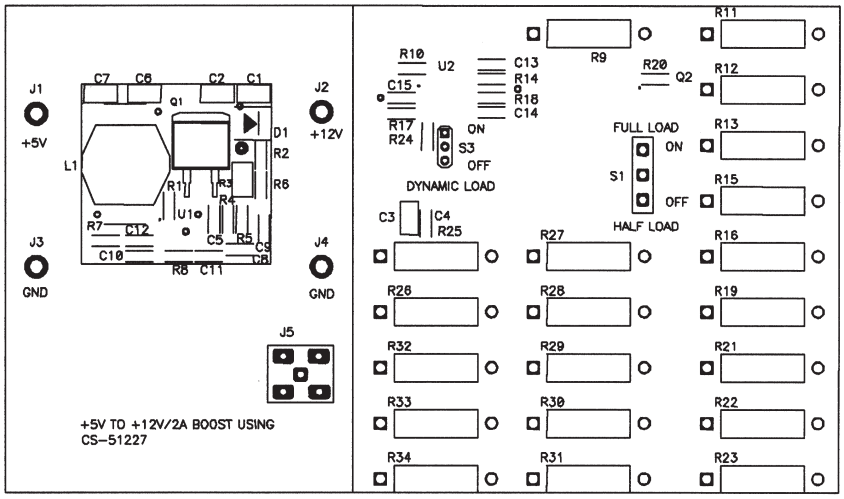


Figure 16. Silk Screen

1:1 IMAGE

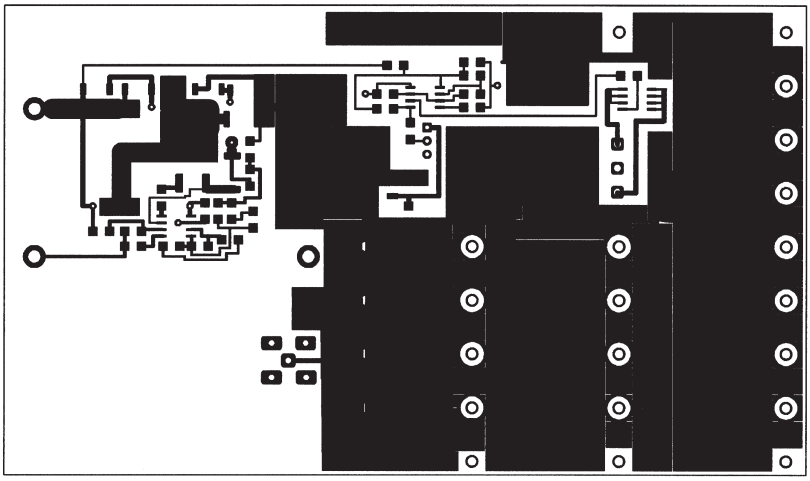


Figure 17. Top Layer

1:1 IMAGE

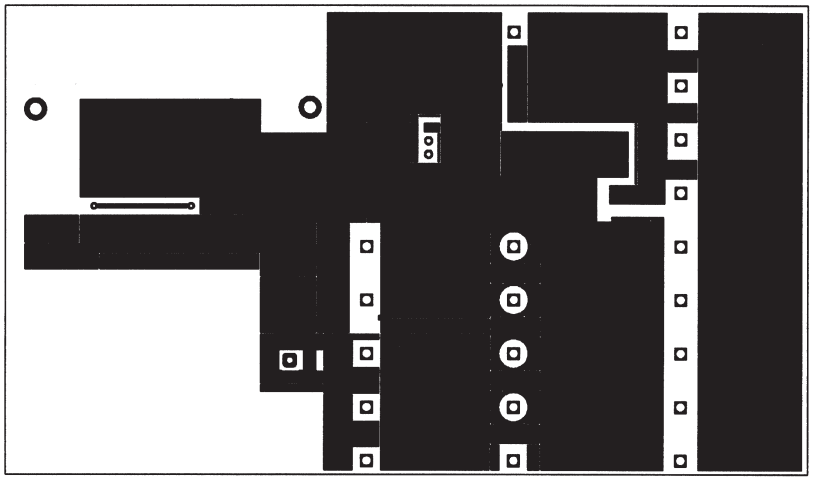


Figure 18. Bottom Layer

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