TEXAS INSTRUMENTS

PanelBus™ TFP201EVM

User's Guide

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Mixed-Signal Products

SLDU001

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the PanelBus™ TFP201 evaluation module (EVM) kit.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Overview
- ❏ Chapter 2 – Physical Description
- ❏ Chapter 3 – Circuit Description

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Data Sheets:

- TFP201 Literature No. SLDS116
- TFP6422, TFP6424 Literature No. SLDS118

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Chapter 1

Overview

This chapter gives a general overview of the TFP201 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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1.1 Purpose

The TFP201 EVM can be used to evaluate the TFP201 performance and device parameters, while acting as a guide for high-speed board layout. The board allows the designer the ease of connecting directly from the output of an existing system to the input of the flat panel display through a DVI connector. The board receives encoded serial data sent over three differential pairs and one clock signal over a fourth differential pair that deserializes the data. Parallel data and a clock signal are provided to an onboard transmitter, which reserializes the data and the outputs to the connector, and then sends to the digital connector of the display.

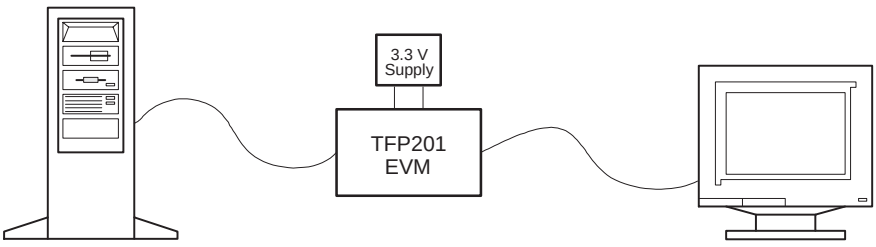
1.2 EVM Basic Function

The Texas Instruments TFP201 EVM kit is used to evaluate the performance and design of the TFP201 using an existing system with a DVI interface. The board allows the designer to connect to a video card where the data and clock are serialized and transmitted along four differential pairs. The receiver then deserializes the data, providing 24 bits (48 bits in 2 pix/clk) of data and a clock. The receiver than sends the data to an onboard transmitter that reserializes the data and outputs the four differential pairs through the DVI connector to the display. The TFP201EVM will support up to SXGA resolutions.

Overall, the board is designed and optimized to support high-speed operation. In general, the board impedance should be controlled to 50 Ω and impedance mismatches should be kept to a minimum by designing the component pad size to be as close as possible to the width of the connecting transmission line. In addition, to reduce board skew, trace lengths should be matched as closely as possible.

Some features offered by this board include:

- ❑ PCB and DVI cable are designed for high-speed signal integrity.
- ❑ The PCB can be configured for additional power supply options.
- ❑ All input/output signals are accessible.



1.3 TFP201 EVM Board Configuration and Operation

The TFP201 EVM board is simple to use, requiring only a few steps to operate:

1) Connect power supply GND and 3.3 V V_{CC}.
2) Connect DVI input cable from PC (typically 2–3M cable).
3) Connect DVI output cable to monitor (typically 2–3M cable).
4) Power on the supply.

The TFP201 EVM board has various options for different modes of operation, selectable by jumpers and switches. When shipped, the board is fully operational and all jumpers are in the default positions.

Note:

When handling board, ESD protection is needed.

1.3.1 Power Supply

A 3.3-V dc power supply is needed to operate the TFP201 EVM. This board is designed for use with one or two power supplies. Two supplies can be used if there is a desire to separate power to the TFP201 from the onboard transmitter. If two supplies are used, jumper P14 must be removed; if one supply is used, P14 must be connected. The default configuration is jumper P14 on.

1.3.2 High-Speed Data Line Probe Point

The high-speed data lines can be monitored on an oscilloscope via the SMA connectors on the TFP201 EVM. Each data line has a 1-kΩ resistor in series with the SMA connector. This creates a 21:1 test probe point; thus the signal is attenuated by a factor of 21. This 21:1 probe point is used to compensate for rise time degradation through scope probes.

1.3.3 Impedance Matching

The TMDS inputs to the TFP201 Receiver have a fixed signal-ended termination to AVDD. The TFP201 is internally optimized using a laser trim process to precisely fix the impedance at 50 Ω. The device will function normally with or without a resistor on the EXT_RES terminal. The fixed impedance eliminates the need for an external resistor while providing optimum impedance matching to standard 50 Ω DVI cables.

1.3.4 Transmitter Voltage Swing

The voltage swing on the transmitter can be adjusted via resistor R21. The voltage swing can be adjusted depending on the length of the cable being used. The larger the voltage swing, the better the signal to noise ratio.

1.3.5 Jumper Configuration

Table 1–1 and Table 1–2 reflect the default configuration of jumpers on the TFP201 EVM board.

Table 1–1. Default $\overline{PDO}$ Jumper Configuration

Designator	Function	Condition
P19	Jumper SCDT to $\overline{PDO}$	Off
P20	Jumper $\overline{PDO}$ to SW1	On

Table 1–2. Default Power Supply Jumper Configuration

Designator	Function	Condition
P14	Jumper Vcc1 to Vcc2	On
P6	Jumper Vcc1 to PVCC	On
P7	Jumper Vcc1 to AVCC	On
P8	Jumper Vcc1 to OVCC	On
P13	Jumper Vcc1 to DVCC	On
P9	Jumper Vcc2 to IVCC	On
P10	Jumper Vcc2 to PVCC1	On
P11	Jumper Vcc2 to VCC	On
P12	Jumper Vcc2 to AVCC_tx	On

Note: Power supply jumpers should only be removed and replaced with power turned off. Power supply supply jumpers can be removed to monitor individual supply currents.

1.3.6 Switch 1 Configuration

Table 1–3 reflects the default configuration of Switch 1 on the TFP201 EVM board to operate the TFP201 in normal mode. Refer to the data sheet for specific terminal functions.

Table 1–3. Default TFP201 EVM Switch 1 Configuration

Designator	Function	Condition
1	TFP201 RSVD	Off (high)
2	TFP201 STAG select	Off (high)
3	TFP201 DFO select	On (low)
4	TFP201 PIXS	On (low)
5	TFP201 ST	Off (high)
6	TFP201 OCK_INV select	On (low)
7	TFP201 $\overline{PD}$ select	Off (high)
8	TFP201 $\overline{PDO}$ select	Off (high)

1.3.7 Switch 2 Configuration

Table 1–4 reflects the default configuration of Switch 2 on the TFP201 EVM board to operate the transmitter in normal mode.

Position 1 – Sync_cont: This pin is reserved; under normal operation it should be kept in the off position.

Position 2 – PD: Power down select, this pin controls the transmitter power down mode. Under normal operation this pin should be in the off position.

Position 3 – PIXS: Pixel select, this pin selects 1 pix.clk input for TFT or DSTN when in the on position or 2 pix.clk input for TFT when in the off position. The default configuration for this pin should be in the on position.

Position 4 – EDGE: Input signal latch edge, when in the on position signals are latched on the falling edge of IDCK. When in the off position, signals are latched on the rising edge of IDCK. The default position for this pin is in the on position.

Table 1–4. Default TFP201 EVM Switch 2 Configuration

Designator	Function	Condition
1	Transmitter Sync_cont (reserved)	Off (high)
2	Transmitter PD select	Off (high)
3	Transmitter PIXS select	On (low)
4	Transmitter EDGE select	On (low)

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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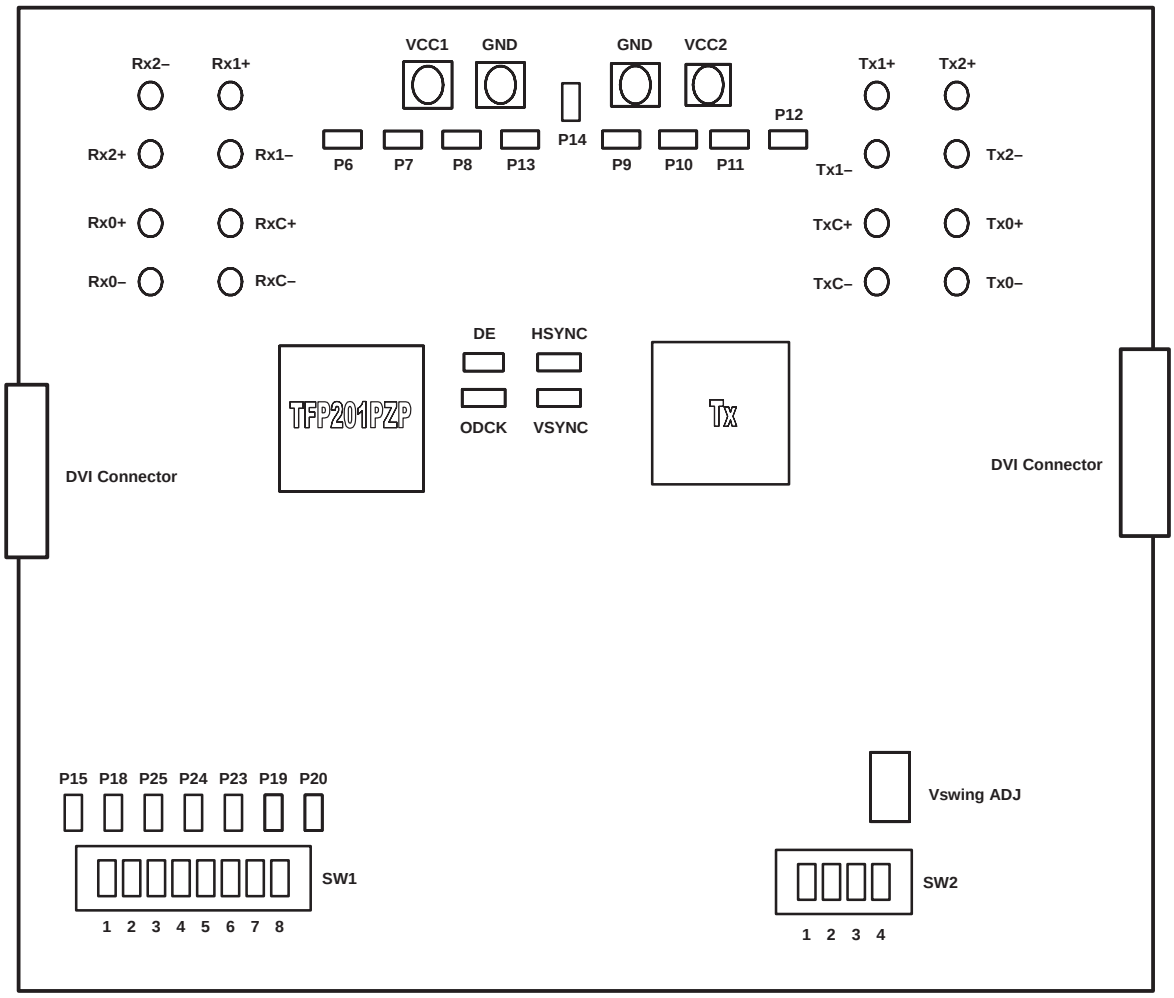
2.1 TVP201 EVM Board Diagram



2.2 Component List

Table 2–1 lists the components used in constructing the EVM.

Table 2–1. TFP201 EVM Bill of Materials

Item	QTY.	MFG.	MFG. Part#	Ref. Description	Description	Value or Function
10	22	Any	Header, male, 2PI	P6–P15,P18,P19 P20–P25,P30 P31,P32,P36	Header	Male, 2 pin, 0.100 cc
12	1		DUT_TQFP_PZP100	U1	IC,TQFP/PZP,100pin	DUT–user defined
44	13	Murata	GRM36COG101J50S	C45–C57	Capacitor,SMT0402	50V,±5%,100pF
45	32	Murata	GRM36Y5V103Z50	C8–C39	Capacitor,SMT0402	50V,+80%–20%, 0.01 μF
46	2	Panasonic	ECS–T1CX106R	C58,C59	Capacitor,SMT,TANT	20%, 16V, 10 μF
47	7	AVX	TPSE226K035R030	C1–C7	Capacitor,SMT,TANT	10%, 50V, 22 μF
48	5	AVX	08051C104JATMA	C42–C44,C60, C61	Capacitor,SMT0805	0.1 μF long lead time 16 W
49	2	TBD	DVI1.0D	P1,P2	Connector,Thru,24P	Digital only receptacle
50	16	Macom	2262–0000–09	J4–J19	Connector, SMA	SMA coax straight PCB
51	1	AMP	745783–4	J1	Connector,D–SUB	25Pin,RA,female
52	8	Murata Erie	BLM11A601A	L1–L8	Filter,SMT0805	Ferrite,600 Ω, 200 mA
53	1	Silicon Image	SiI150A	U2	IC,SMT,100P	Panelink digital transmit
54	2	Pomona	3267–PK10X2	J2,J3	JACKS, BANANA, TWO	Qty(2)ea. 3267–PK10
55	1	Dale	CRCW08054020F	R1	Resistor,S M, 1/10w, 1%	402 Ω
56	16	Panasonic	ERJ–2GEJ102	R3–R9,R12,R13 R14–R20	Resistor, SMT0402	±5%, 1.0
57	2	Panasonic	ERJ–6GEY103	R57,R58	Resistor, SMT0805	±5%,10K
58	2	Panasonic	ERJ–3GSYJ102	R10,R11	Resistor, SMT0603	±5%,1.0K
59	18	Panasonic	ERJ–3GSYJ333	R38–R49,R51 R52–R56	Resistor, SMT0603	±5%,33K
60	1	C&K	BD08	SW1	Switch, SPST, Dip16	Switch, 16P, SPST × 8
61	1	C&K	BD04	SW2	Switch, SPST, Dip8	Switch 8, SPST × 4
63	1	Bourns	3292W–201–ND	R75	TRIMPOT, 3P	200 Ω
64	1	Bourns	3296W–202–ND	R21	TRIMPOT, 22_TURN	12 K Ω

Chapter 3

Schematics

This chapter contains the EVM schematic diagrams.

Figure 3–1. TFP201 Receiver Schematic

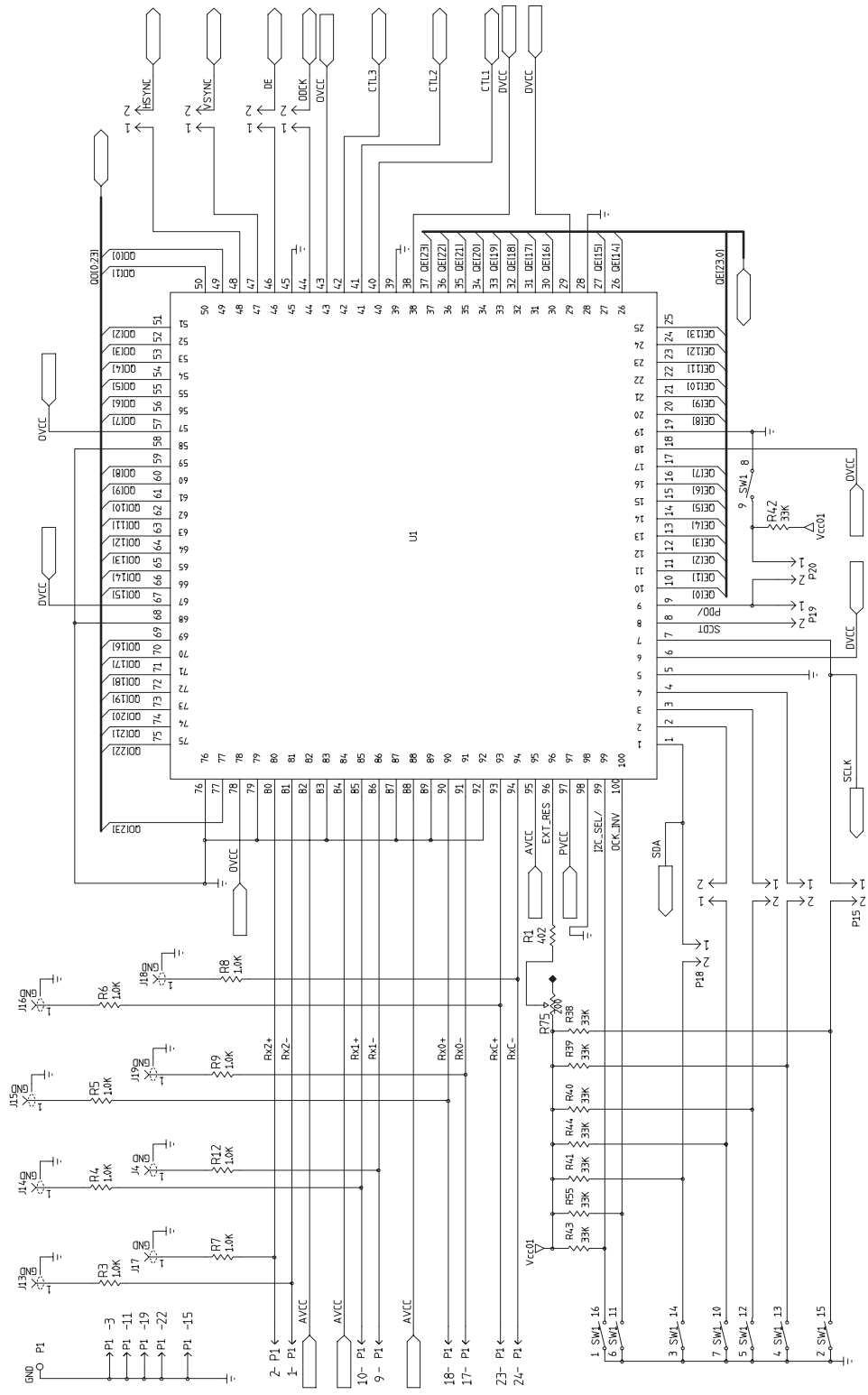


Figure 3–2. Transmitter Schematic

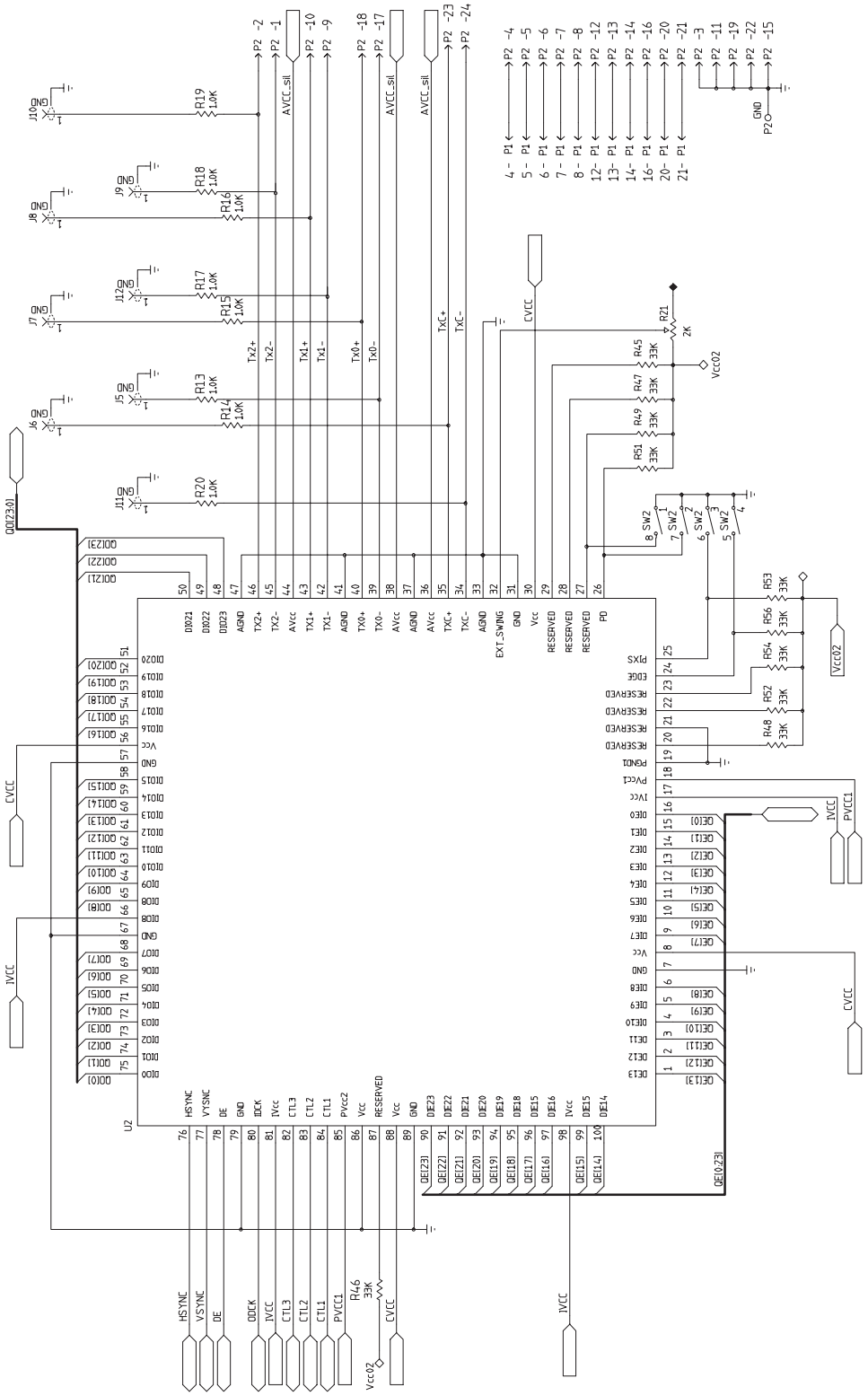


Figure 3–3. Power Supply Decoupling Schematic