Application Report
SLLA044

TSB12LV32 (GP2Lynx)/TSB41LV03 Reference Schematic

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Abstract

This application report describes the electrical connections between the Texas Instruments (TI™) TSB12LV32 (GP2Lynx) and TSB41LV03 (400-Mbps 3-port PHY) for common modes of operation. This document should be used in conjunction with the TI application report, *PHY Layout* (literature number SLLA020), to successfully design a 1394 system.

The TSB12LV32 (GP2Lynx) is a high-performance, general-purpose IEEE 1394.A link-layer controller (LLC) capable of transferring data between a host controller, the 1394 PHY-link interface, and external devices connected to the Data Mover port (local bus interface). For more information on the GP2Lynx device, see the TI data sheet, *General-Purpose Link Layer Controller (GP2Lynx)* (literature number SLLS336).

The TSB41LV03 is a three-port 400-Mbps physical layer device that fully supports provisions of the IEEE 1394-1995 standard and P1394a supplement (version 2.0). The TSB41LV03 can operate at 100 Mbps and 200 Mbps. For more information on the TSB41LV03, see the TI data sheet, *IEEE 1394a Three Port Cable Transceiver/Arbiter* (literature number SLLS317), and the *Errata to the TSB41LV03 Data Sheet* (literature number SLLS316A).

NOTE:
This reference schematic does not represent an actual test board constructed by Texas Instruments, Inc.

Contents

Schematic

The Cable Interface

The schematic for the cable interface is shown on sheet 1 and includes two 1394 ports that connect to the PHY. The third 1394 port is not implemented to show how to correctly terminate an unused port. Please note that if three or more 1394 ports are implemented, a 1.5-A current-limited fuse must be connected between each port and the bus power.

- The cable power from each cable (pin #1, PWR, on the 6-pin 1394 connector) is connected to the other ports and is available as bus power. The PHY operates off of bus power on the schematic. A voltage regulator regulates the bus power to 3.3 V. To be 1394 compliant, the regulator must maintain 3.3 V when the input voltage ranges between 8 VDC and 33 VDC. The voltage regulator is shown on Sheet 1 of the GP2Lynx/TSB41LV03 schematic. When cable power is not active, the PHY may also be powered from a 12-V source, such as a PC power supply. A diode determines which power source is used. For protection, a 0.75-A fuse should also be used.

- The cable shield from each cable (pins #7 and #8 on the 6-pin 1394 connector) is connected to chassis ground through an R-C network. The R-C network is designed to prevent current from flowing on the cable shield in case of potential differences between chassis grounds. We suggest a combination of a 1-kΩ resistor, two 0.001-µF capacitors, and two 0.01-µF capacitors placed next to each 1394 connector. This helps prevent the cable shield noise from one port from coupling onto the other.

- The cable ground (pin #2 on the 6-pin 1394 connector) is tied directly to PHY ground. According to the IEEE 1394 standard, all PHYs in a network must be at the same ground potential for common mode signaling to work properly.

- The drivers on each port (TPA and TPB) are designed to work with an external 112-Ω termination-resistor network. This is to match the 110-Ω cable impedance. One network is provided at each end of the twisted-pair cable. The midpoint of the TPA resistor network is directly connected to TPBIAS. The midpoint of the TPB resistor network is coupled to ground through a parallel RC network. These termination resistor networks should be placed as close as possible to the PHY.

- The TPBIAS lines indicate the presence of an active connection to other nodes on the bus. A 1-µF capacitor external filter must stabilize the TPBIAS lines. A 1-µF capacitor to ground filter must be connected to the TPBIAS line of any unused ports as well.

The Physical Layer Device—TSB41LV03 (400-Mbps, 3-Port PHY)

The electrical connection for the physical layer device is shown on Sheet 2 of the GP2Lynx/TSB41LV03 schematic.

All power pins on the TSB41LV03 PHY should be tied together, then coupled to the associated power pins and ground pins through a series of high-frequency decoupling capacitors. The following rules apply to the decoupling capacitors:

1) Place one 0.1-µF capacitor as close as possible to each single power pin on the PHY. A single power pin is one that is not adjacent to another power pin. For example, pin #73 (PLLVDD) is a single power pin.

2) Place one 0.001-µF capacitor as close as possible to each power pin. If two or more power pins are adjacent, only one 0.001-uF capacitor is required for the group. For example, pins #47 and #48 must be connected only to a single 0.001-uF capacitor because they constitute a power pin group.

NOTE:
Refer to Figure 8 in the TSB41LV03 data sheet, *IEEE 1394a Three Port Cable Transceiver/Arbiter* (literature number SLLS317), for detailed information on capacitor placement.

- The TSB41LV03 has 5-V tolerant inputs. When interfacing to a 5-V device, these input pins should be tied to a 5-V source; otherwise they should be connected to the 3.3-V supply voltage of the PHY. The 3.3-V implementation is shown in the schematic.

- The /ISO pin is used to control the output differentiation logic of the CTL and D lines on the link layer interface for the Annex J method of isolation. If the IEEE 1394-1995 Annex J method of isolation is used, the /ISO pin should be tied low. If either the Texas Instruments bus-holder method of isolation or no isolation is used, this terminal should be tied high (to PHY power through a 10-kΩ pull-up resistor). No isolation is implemented in the schematic.

- The CPS pin detects the presence of cable power and is connected to the cable power through a 400-kΩ resistor. A common resistor value of 390 kΩ may be used. For a six-pin 1394 connector, the node should always have the CPS pin connected to cable power through a 400-kΩ resistor, even if the PHY does not use cable power. The only instance in which the CPS pin may not be connected to cable power is the case of a 4-pin 1394 connector or 6-pin connector with power class 000. In this case, the CPS may be tied directly to PHY ground, indicating that cable power is not available.

NOTE:
For a 200-Mbps PHY, the CPSInt internal interrupt will continuously be set after it is cleared, if the CPS pin is tied low. The software should ignore this interrupt. If the software cannot ignore this interrupt, the CPS pin may be directly tied to VDD, but the PHY will report the wrong cable power status to the node.

- When a 1394 port is not brought out to a connector, it must be terminated correctly. To terminate a non-implemented port, the TPB+ and TPB- pins must be tied together and connected to ground. The TPBIAS should be tied to ground through a 1-µF capacitor. The TPA+ and TPA- lines can be left unconnected. Port 1 in the schematic is not brought out to a connector to illustrate a properly terminated port.

- The FILTER0 and FILTER1 function as a filter for the internal PLL. A 0.1-µF (10% or better) is the only external requirement needed to complete this filter.

- The SE and SM pins are test-input pins used in the manufacturing testing of TSB41LV03. For normal use, these pins should be tied to ground separately through a 1-kΩ resistor.

- The /RESET pin must be asserted low for a minimum of 2 ms from the time PHY power reaches the minimum required supply voltage to ensure proper operation. When using a passive capacitor on the /RESET pin to generate a power-on reset signal, the minimum reset time will be guaranteed, if the capacitor has a minimum value of 0.1-µF and satisfies the following equation:

  $$C_{min} = (0.0077 \times T) + 0.085\ \mu F$$

  where

  C_{min} : is the minimum capacitance on the RESET pin in µF.
  T : is the VDD ramp time from 10%-90% in ms.

  Additionally, an approximately 120-kΩ resistor should be connected in parallel with the reset capacitor to ensure that the capacitor is discharged when PHY power is removed. An alternative to the passive reset is to actively drive /RESET low for the minimum reset time following power on.

- The R0 and R1 terminals set the internal operating currents and the cable driver output current. To meet the IEEE 1394-1995 standard output voltage limits, a 6.3-kΩ ±0.5% resistance is required. To achieve this, a 6.34-kΩ ±0.5% and 1-MΩ ±10% resistor are placed in parallel.

- The X0 and XI terminals are the crystal oscillator inputs. These terminals connect to a 24.576-MHz parallel resonant fundamental mode crystal. There is a strict total tolerance of 100 pulse-position modulation (ppm) on the 24.576-MHz crystal. This tolerance must be met to comply with the overall requirement of 100 ppm per the IEEE 1394-1995 standard. For every crystal, loading requirements depend on the board technology and distance from the PHY.

  Crystal Selection: To ensure that the PHY crystal starts under all operational conditions, we recommend using a fundamental parallel mode crystal with a CL of 15 pF or less. The termination capacitor values that should be placed on each leg of the crystal can be calculated with the following equation:

  $$C_{termination} = (C_L - C_{board}) \times 2$$

  where

  C_{board} = (Board trace capacitance + PHY input capacitance)

  If the crystal is placed close to the PHY, $C_{board} \cong 4$ pF and $C_{termination} \cong 22$ pF.

- TESTM is the test control input used during the manufacturing of the TSB41LV03 PHY. It should be tied to VDD.

- The power class pins (PC0-PC2) program the power class value into the PWR field of the transmitted self-ID packet. This allows other nodes on the bus to understand what kind of power requirements the node requires. These pins are programmed according to the Power Class Descriptions in the IEEE 1394.a Standard, Table 7-3. The schematic is programmed to a power class of “100” or decimal 4. This indicates that the node:

  1) May be powered from the bus
  2) Is capable of repeating power
  3) Is using up to 3 W
  4) Needs no additional power to enable the link

  The power class pins are hard-wired to their values on the schematic.

The PHY-Link Interface

- The PHY link interface electrical connection is shown on Sheet 2 of the GP2Lynx/TSB41LV03 schematic. The PHY-link interface follows the IEEE 1394-1995 and 1394.a standards. No isolation is implemented in this schematic. The PHY and link operate off of the same ground plane.

- To reduce EMI emissions and reduce reflections on the SYSCLK line, a series-damping resistor is recommended. The schematic shows a 0-Ω resistor, which is essentially a placeholder on the board. To reduce EMI, a 22-Ω resistor on the SYSCLK line is recommended. This resistor should be placed as close to the PHY as possible. Its value can be adjusted to reduce emissions. By slowing down the edge rates on SYSCLK, this 22-Ω resistor will significantly reduce reflections that may occur when the distance between the PHY and link is large (greater than 4 inches in this case).

- The Link Request signal (LREQ) is input to the PHY from the link. The link uses this to initiate a service request to the PHY. CTL0 and CTL1 are bi-directional signals used to control communication between the PHY and the link. These signals should be directly connected between the PHY and link.

- The TSB12LV32 is a 400 Mbps-link layer device that uses all data I/O lines (D0-D7) to communicate with the PHY. When status information is received from the PHY, only D0 and D1 are used. The TSB41LV03 is also capable of speeds up to 400 Mbps and provides eight data I/O lines. The Link-On output from the PHY (C/LKON) notifies the link layer to power up and become active. The Link-On output is a square wave signal with a period of approximately 163 ns (8 SYSCLK cycles). The Link-On output is de-asserted (low value) once the LPS input terminal is active. A 1-kΩ series resistor between the C/LKON pin of the PHY and the LINKON pin of the link is recommended. This is a precaution step to prevent a possible bus contention situation. The contender status is part of the self-ID packet. The 4.7-kΩ pull-down resistor guarantees a low value on the LINKON input terminal during the hardware-reset process.

- To power down the PHY and link for lower power consumption when not in use, the LPS and C/LKON method should be used. In this method, the link LPS output terminal controls the PHY LPS input terminal. If the last active port on the PHY is disconnected, a bus reset will occur and a self-ID packet will be sent to the link. From the port status information contained in the self-ID packet, the link will know that there are no connected ports on the PHY and consequently de-assert its LPS pulsed output. With LPS de-asserted, the PHY disables the PHY/Link interface. Also, when all cables are disconnected, the TSB41LV03 PHY automatically shuts down the cable side of the PHY. When an active cable is plugged in, the TSB41LV03 PHY can be configured to automatically start pulsing the C/LKON pin. The link responds by re-asserting the LPS pulse. The PHY then stops sending the Link-On pulse.

- If no power down option is implemented, the PD pin on the PHY (pin 18) should be tied to ground.

The Link-Layer Controller—TSB12LV32 (GP2Lynx)

- The TSB12LV32 is a 400-Mbps general-purpose IEEE 1394.A link-layer controller. The GP2Lynx was intended for use in PC peripherals, such as printers, scanners, and desktop cameras. It can transfer data between a host controller, 1394 PHY-link interface, and external devices connected to the data mover port (local bus interface).

- The GP2Lynx DIRECT pin is sampled during hardware reset to determine if galvanic isolation is present. If the terminal is high, no isolation is present. If the terminal is low, either the TI bus-holder isolation or the Annex J isolation scheme is used.

- The CONTNDR terminal on the link defaults to being an input on a hardware reset. In the schematic, CONTNDR is tied to ground. This tells the link that the node is not contender for Isochronous Resource Manager (IRM) or Bus Manager functions. However, after power-on, the value of this pin may be driven internally from the CTNDRSTAT bit inside the link layer controller.

- The GP2Lynx has a programmable microcontroller interface with 8-bit or 16-bit data bus, five different modes of operations including burst mode, and a clock frequency up to 50 MHz. In this schematic, it is set up to operate in 16-bit fixed-timing mode with a Motorola 68000-style processor. To configure the GP2Lynx for this mode, the MCMODE/SIZ1 and M8BIT/SIZ0 pins are tied to ground. Because the device is not configured for the Motorola ColdFire mode, the ColdFire terminal is also tied to ground.

- The /MCS (Cycle Start) terminal is an active-low input terminal to the GP2Lynx. It signals the beginning of a microcontroller access to the GP2Lynx. The MCS is connected to the TSZ line on the Motorola 68000. The /MCA is an active-low output signal representing the cycle acknowledge sent from the GP2Lynx to the TAZ terminal on the 68000. MWR is the read/write indicator. When asserted high, this input terminal indicates a read access from the GP2Lynx. When asserted low, it indicates a write access to the GP2Lynx. All data transfers on the microcontroller interface are synchronized with the rising edge of BCLK.

- The GP2Lynx device follows the big-endian architecture; to configure the microinterface for little-endian mode, the LENDIAN pin must be set high. In little-endian mode, the MD[0:15] lines are byte-swapped before it is written into the device's internal FIFO or configuration register (CFR). In the schematic, big-endian mode is used; therefore, LENDIAN is tied to ground. Because the Motorola 68000 processor uses bit 15 as the MSB (most significant bit) and the GP2Lynx uses bit 0 as the MSB, the data interface is swapped between the two devices. (i.e., bit 15 on the GP2Lynx and bit 0 on the 68000 are connected together). The microinterface can also be configured for data-invariant or address-invariant modes using the MDINV and MCMODE/SIZ0 terminals. However, MDINV is meaningful only when LENDIAN is enabled (high).

- All GP2Lynx internal registers are 32 bits wide. However, because the Motorola 68000 processor operates on word boundary accesses, the GP2Lynx internally stacks 2 word writes before transferring them to the link registers. No external byte stacking is needed.

- Accessing all GP2Lynx internal registers requires only 7 bits of address lines. Because MA[0] is the MSB bit on the TSB12LV32, it is connected to A[6] of the 68000 processor. Consequently, MA[6] is connected to A[0] of the 68000 processor.

- The /TEA output terminal is connected to the Motorola TEAZ input terminal. This signal indicates the presence of an error in the data transfer operation.

- The STAT0-STAT2 are general status output terminals. These pins can be independently programmed to show one of fourteen possible internal hardware statuses. See the TI data sheet, *General-Purpose Link Layer Controller (GP2Lynx)* (literature number SLLS336), for details regarding the programming of these terminals.

- The CYCLEIN input terminal is an optional external 8-kHz clock used as the isochronous cycle clock. This terminal is tied to VDD because it is not used in this case.

- /INT is an active-low output terminal representing the logical NOR of all internal interrupts.

- The data mover (DM) port is an 8/16-bit high-speed port that supports isochronous, asynchronous, and asynchronous streaming transmit/receive from an unbuffered port @ 25 MHz. It is meant to handle an external memory interface of large data packets. The DM port has eight modes of operation and can support four-channels for isochronous transmit.

- The DM port has seven control pins. See the TI data sheet, *General-Purpose Link Layer Controller (GP2Lynx)* (literature number SLLS336), for more information on the functionality of these pins.

NOTE:

Test headers at the bottom of Sheet 1 of the schematic are not part of the reference schematic. The test headers are optional and when designed in provide an excellent way of monitoring signals on the different interfaces of the TSB12LV32 (GP2Lynx) link. Some test headers may also be used to generate various bit patterns, which can drive signals on the microcontroller or the data mover interface ports.

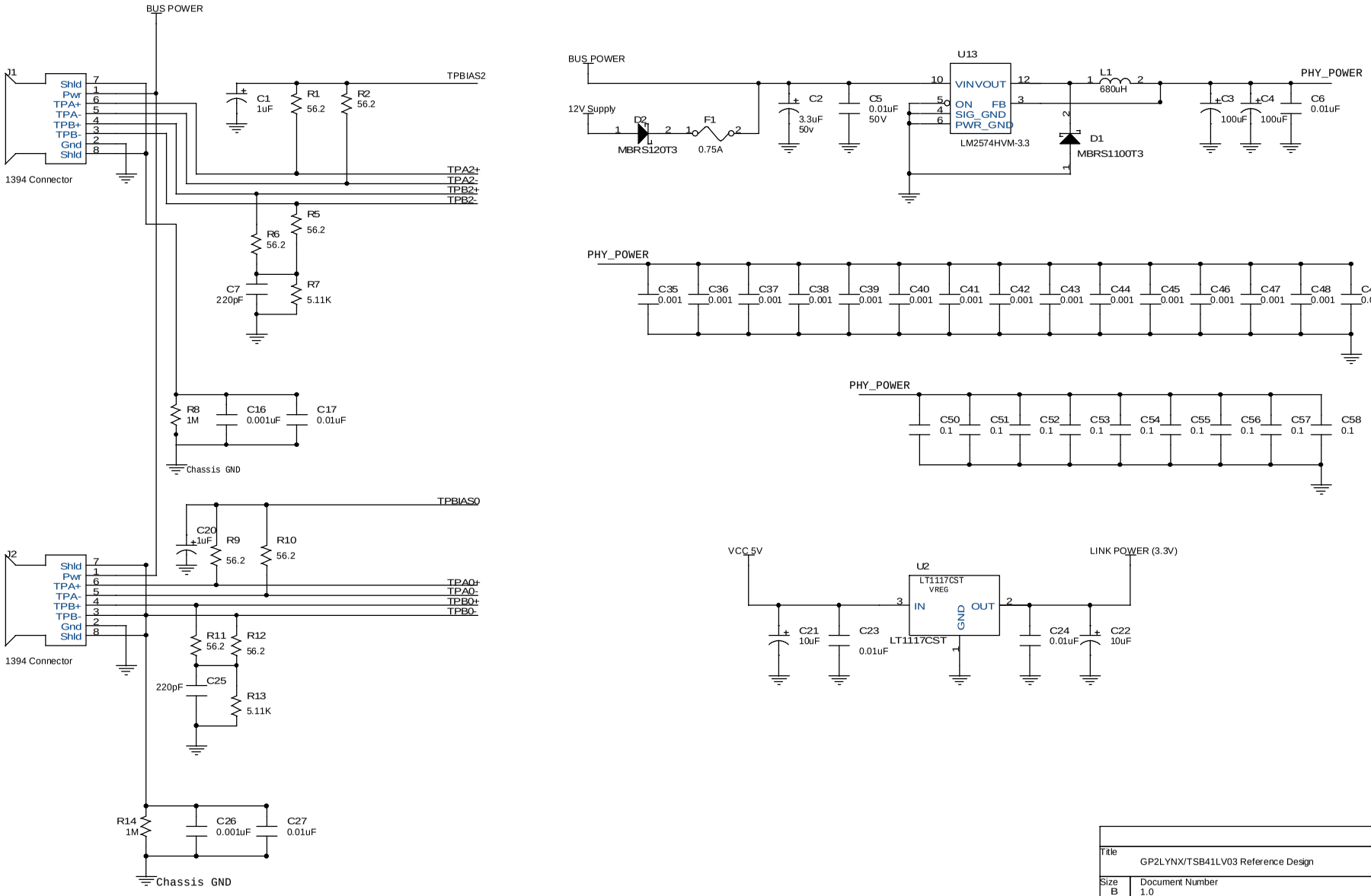
Appendix A. Parts List for Schematic

The following parts are represented on the schematic pages. Other parts may be used as long as their function and/or parameters meet the IEEE 1394-1995 and IEEE 1394.a specifications.

Description	Supplier	Part Number	Package	Quantity	Reference Designator
22-pF 5% Capacitor	Digi-Key	PCC120CNCT-ND	0805	2	C30, C31
220-pF Capacitor	KEMET	C0805C221J5GAC	0805	2	C7, C25
0.001-µF Capacitor	KEMET	C0805C102K5RAC	0805	19	C16, C26, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49
0.01-µF 10% Capacitor	KEMET	C0805C103K5RAC	0805	8	C5, C6, C17, C23, C24, C27
0.1-µF 10% Capacitor	KEMET	C0805C104K5RAC	0805	11	C33, C34, C50, C51, C52, C53, C54, C55, C56, C57, C58
1-µF 50 V Capacitor	KEMET	T491A105M016AS	0805	3	C1, C20, C32
3.3-µF 50 V Capacitor	KEMET	T491D335K050AS	2816	1	C2
10-µF 20% 25-V Capacitor	KEMET	T491D106K025AS	2816	2	C21, C22
100-µF 20% 10-V Capacitor	KEMET	T495X107M010AS	2816	2	C3, C4
DIODE	MOTOROLA	MBRS1100T3	1815	1	D1
DIODE	MOTOROLA	MBRS340T3	2824_dio1	1	D2
FUSE, 0.75-A	RayChem	SMD075-2	2920_FUSE	1	F1
1394 R/A Flat Header	MOLEX	53462-0611	Socket_6	2	J1, J2
0-Ω Resistor	TDK	SLF7032T-681MR16	0805	1	R35
56.2-Ω 1% Resistor	KOA	RK73H2AT56R2F	0805	8	R1, R2, R5, R6, R9, R10, R11, R12
1-kΩ 5% Resistor	KOA	RM73B2AT102J	0805	5	R32, R34, R37, R38, R39
4.7-kΩ 5% Resistor	KOA	RM73B2AT472J	0805	1	R33
5.11kΩ Resistor	KOA	RK73H2AT5111F	0805	2	R7, R13
6.34-kΩ 0.5% Resistor1	KOA	RM73H2AT6341D	0805	1	R28
10-kΩ Resistor	KOA	RM732B2AT103J	0805	5	R30, , R36
110-kΩ 5% Resistor	KOA	RM73B2AT114J	0805	1	R40
390-kΩ 5% Resistor	KOA	RM73B2AT394J	0805	1	R15
1-MΩ 1%	KOA	RK73H2AT105F	0805	3	R8, R14, R29

Description	Supplier	Part Number	Package	Quantity	Reference Designator
Resistor					
Voltage Regulator	National	LM2574HVM-3.3	so14_464	1	U13
LT1117CST-3.3 V	Liner Tech.	LT1117-CST-3.3	sot223	1	U2
1394 3-Port 400-Mbps PHY	TI	TSB41LV03	80-PIN TQFP	1	U3
GP2Lynx	TI	TSB12LV32	100-PIN PZ	1	U1
XTAL, 24.576-MHz	FOX	FE-24.576 MHz 50/50/0/+70/15 pF	XTAL_FE	1	X1

Appendix B. Schematic


BUS POWER
J1
Shld
Pwr
TPA+
TPA-
TPB+
TPB-
Gnd
Shld
1394 Connector
C1
1uF
R1
56.2
R2
56.2
TPBIAS2
TPA2+
TPA2-
TPB2+
TPB2-
R5
56.2
R6
56.2
C7
220pF
R7
5.11K
R8
1M
C16
0.001uF
C17
0.01uF
Chassis GND
TPBIAS0
C20
1uF
R9
56.2
R10
56.2
J2
1394 Connector
TPA0+
TPA0-
TPB0+
TPB0-
R11
56.2
R12
56.2
C25
220pF
R13
5.11K
R14
1M
C26
0.001uF
C27
0.01uF
Chassis GND
BUS POWER
12V Supply
D2
MBRS120T3
F1
0.75A
C2
3.3uF
50v
C5
0.01uF
50V
U13
VIN
VOUT
ON
FB
SIG_GND
PWR_GND
LM2574HVM-3.3
L1
680uH
D1
MBRS1100T3
C3
100uF
C4
100uF
C6
0.01uF
PHY_POWER
C35
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C36
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C37
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C38
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C39
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C40
0.001
C41
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C42
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C44
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C45
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C46
0.001
C47
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C48
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C49
0.001
PHY_POWER
C50
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C51
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C52
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C54
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C55
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C56
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C57
0.1
C58
0.1
VCC 5V
U2
LT1117CST
VREG
IN
GND
OUT
LT1117CST
C21
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C23
0.01uF
C24
0.01uF
C22
10uF
LINK POWER (3.3V)
Title
GP2LYNX/TSB41LV03 Reference Design
Size
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Document Number
1.0
Rev
1.0
Date:
Monday, April 12, 1999
Sheet
1
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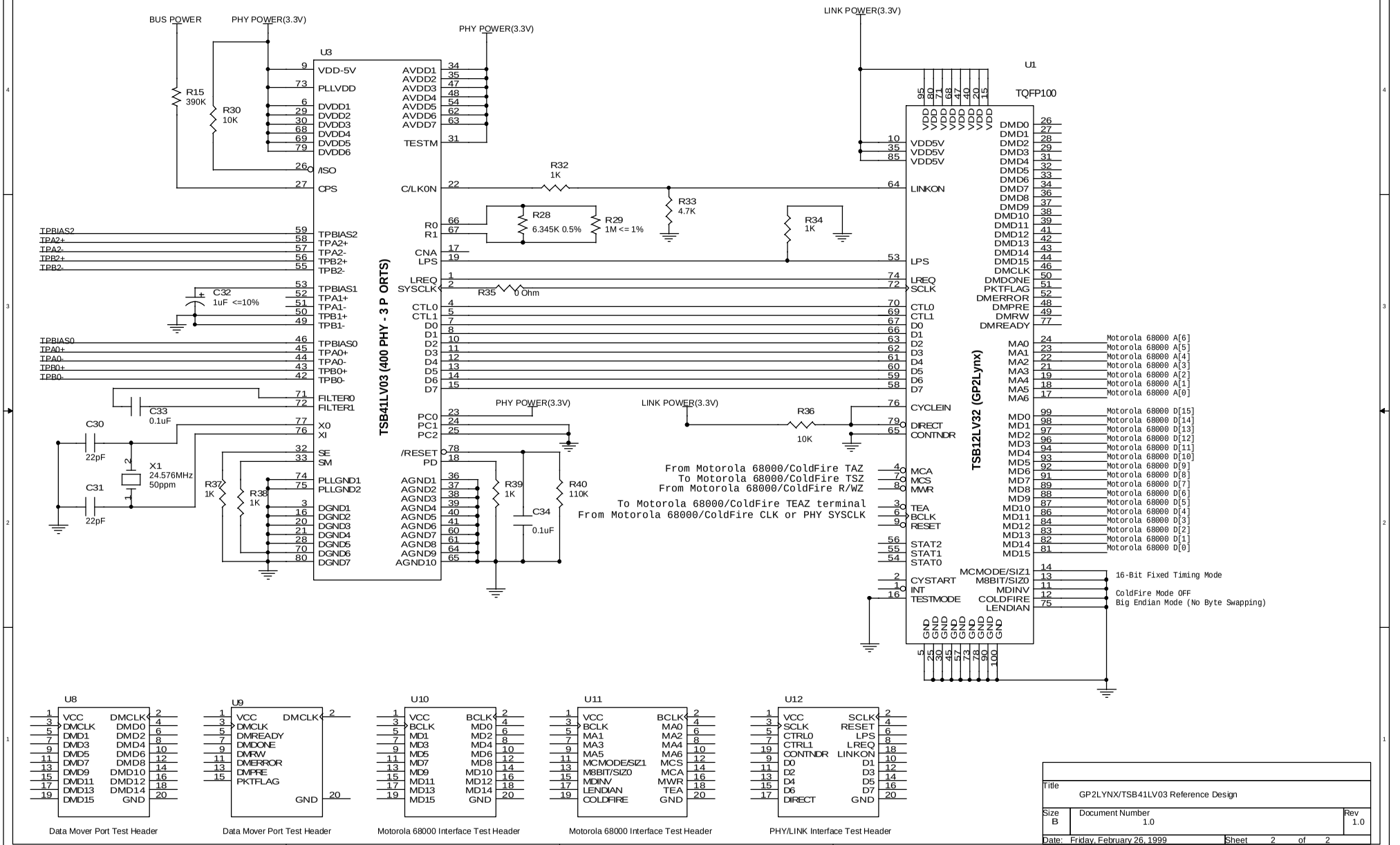
2



U8 Data Mover Port Test Header

U9 Data Mover Port Test Header

U10 Motorola 68000 Interface Test Header

U11 Motorola 68000 Interface Test Header

U12 PHY/LINK Interface Test Header

Title	GP2LYNX/TSB41LV03 Reference Design
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