Si5311-EVB

EVALUATION BOARD FOR Si5311 PRECISION CLOCK MULTIPLIER/REGENERATOR IC

Description

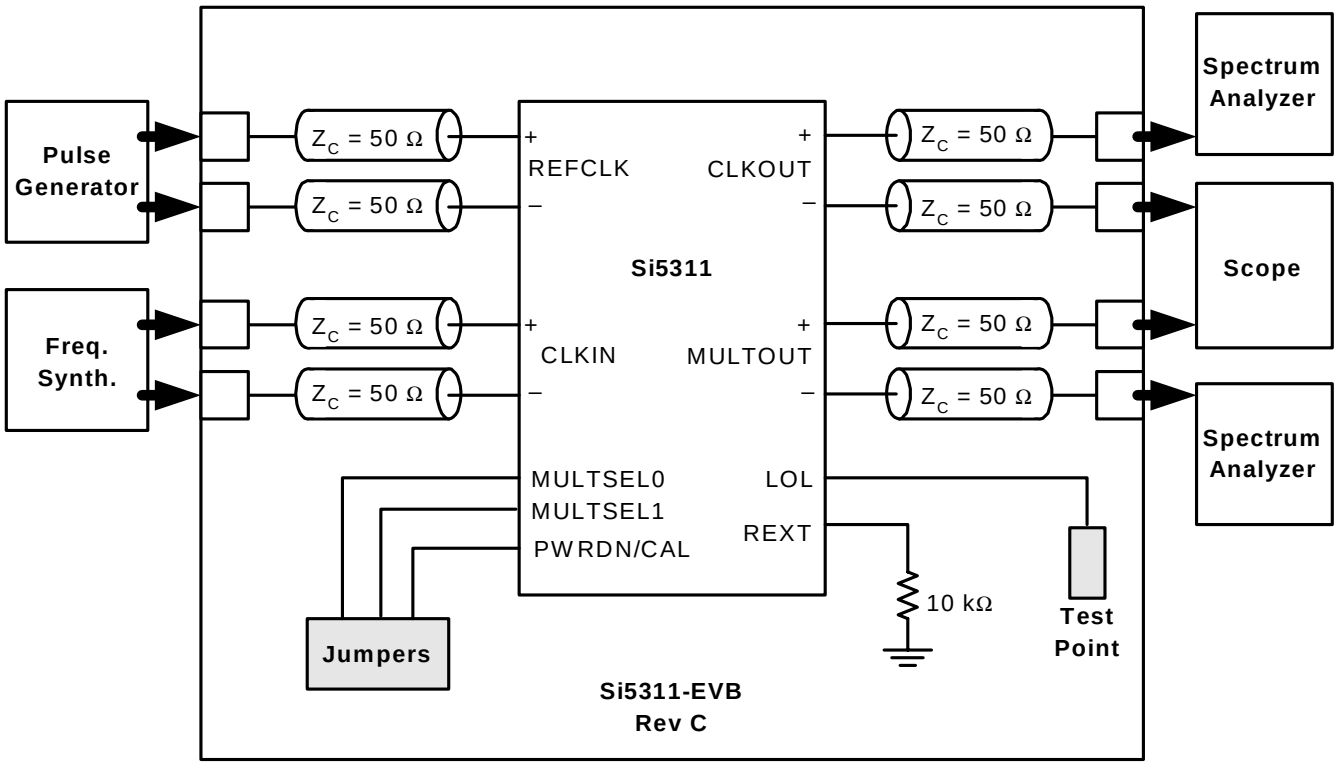
The Si5311 evaluation board provides a platform for testing and characterizing the Silicon Laboratories Si5311 precision high-speed clock multiplier/ regenerator IC.

All high-speed I/Os are ac coupled to ease interfacing to industry standard test equipment.

Features

- Single 2.5 V power supply
- Differential I/Os ac coupled
- Simple jumper configuration

Function Block Diagram



Functional Description

The evaluation board simplifies characterization of the Si5311 precision high-speed clock multiplier/ regenerator IC by providing access to all of the Si5311 I/Os. Device performance can be evaluated by following the “Test Configuration” section. Specific performance metrics include jitter tolerance, jitter generation, and jitter transfer.

Power supply

The evaluation board requires one 2.5 V supply. Supply filtering is placed on the board to filter typical system noise components; however, initial performance testing should use a linear supply capable of supplying 2.5 V ±5% DC.

CAUTION: The evaluation board is designed so that the body of the SMA jacks and GND are shorted. Care must be taken when powering the PCB at potentials other than GND at 0.0 V and VDD at 2.5 V relative to chassis GND.

Self-Calibration

The Si5311 device provides an internal self-calibration function that optimizes the loop gain parameters within the internal DSPLL™. Self-calibration is initiated by a high-to-low transition of the PWRDN/CAL signal while a valid reference clock is supplied to the REFCLK input. On the Si5311-EVB board, a voltage detector IC is utilized to initiate self-calibration. The voltage detector drives the PWRDN/CAL signal low after the supply voltage has reached a specific voltage level. This circuit is described in Silicon Laboratories application note AN42. On the Si5311-EVB, the PWRDN/CAL signal is also accessible via a jumper located in the lower left-hand corner of the evaluation board. PWRDN/CAL is wired to the center post (signal post) between 2.5 V and GND.

Device Power Down

The Si5311 device can be powered down via the PWRDN/CAL signal. When PWRDN/CAL is driven high (2.5 V) the evaluation board will draw minimal current. On the Si5311-EVB board, the PWRDN/CAL signal may be controlled via a jumper located in the lower left-hand corner of the evaluation board. PWRDN/CAL is wired to the signal post adjacent to 2.5 V.

CLKIN, CLKOUT, MULTOUT

These high-speed I/Os are wired to the board perimeter on 30 mil (0.030 inch) 50 Ω microstrip lines to the end-launch SMA jacks as labeled on the PCB. These I/Os are ac coupled to simplify direct connection to a wide array of standard test hardware. Because each of these signals are differential both the positive (+) and negative (–) terminals must be terminated to 50 Ω. Terminating only one side will degrade the performance of the Si5311 device. The CLKIN inputs are terminated on the die with 50 Ω resistors.

Note: The 50 Ω termination is for each terminal/side of a differential signal, thus the differential termination is actually 50 Ω + 50 Ω = 100 Ω.

REFCLK

REFCLK is used to center the frequency of the Si5311 DSPLL so that the device can lock to the CLKIN signal. For a given CLKIN rate, there are five choices for the REFCLK frequency. These five options are all multiples of the CLKIN frequency, as indicated in Table 1. The REFCLK frequency is automatically detected by the Si5311 device, so no digital control inputs are needed for REFCLK frequency selection. REFCLK may be synchronous or asynchronous with respect to CLKIN. However, REFCLK must be within ±100 PPM of the target CLKIN frequency multiple. REFCLK is ac coupled to the SMA jacks located on the top side of the evaluation board. The REFCLK inputs are terminated on the die with 50 Ω resistors.

Note: The 50 Ω termination is for each terminal/side of a differential signal, thus the differential termination is actually 50 Ω + 50 Ω = 100 Ω.

MULTSEL[1:0]

MULTSEL[1:0] is a 2-bit binary input to the Si5311 device that selects the frequency range for the MULTOUT clock output. The MULTOUT output frequency is a multiple of the CLKIN input frequency. The frequency for MULTOUT will be in either the 150–167 MHz frequency range, the 600–668 MHz frequency range, the 1.2–1.33 GHz frequency range, or the 2.4–2.67 GHz frequency range depending on the state of the MULTSEL[1:0] signals as indicated in Table 1. On the Si5311 evaluation board, the MULTSEL[1:0] signals are controlled via two jumpers located in the lower left-hand corner of the board. The MULTSEL[1:0] signals are wired to the center post (signal post) between 2.5 V and GND. The jumper configurations for MULTSEL[1:0] are indicated in Figure 1.

Note: The CLKOUT output signal is valid only for MULTSEL[1:0] settings of 10 or 11 (MULTOUT ranges of 600–668 MHz or 150–167 MHz, respectively). The CLKOUT connectors on the Si5311-EVB should be terminated when they are not in use and/or when using MULTSEL[1:0] settings of 00 or 01.

Table 1. CLKIN, CLKOUT, MULTOUT, REFCLK Operating Ranges

MULTSEL [1:0]	CLKIN Range (MHz)	REFCLK = 2^n x CLKIN ±100 ppm (see Note 2)	CLKOUT	MULTOUT
00 (MULTOUT = 2.4–2.7 GHz)	600.00–668.00	n = –6, –5, –4, –3, or –2	See Note 1(a)	4xCLKIN
01 (MULTOUT = 1.2–1.33 GHz)	300.00–334.00	n = –5, –4, –3, –2, or –1	See Note 1(a)	4xCLKIN
	600.00–668.00	n = –6, –5, –4, –3, or –2	See Note 1(a)	2xCLKIN
10 (MULTOUT = 600–668 MHz)	37.500–41.750	n = –2, –1, 0, 1, or 2	1xCLKIN	16xCLKIN
	75.000–83.500	n = –3, –2, –1, 0, or 1	1xCLKIN	8xCLKIN
	150.000–167.000	n = –4, –3, –2, –1, or 0	1xCLKIN	4xCLKIN
	300.000–334.000	n = –5, –4, –3, –2, or –1	1xCLKIN	2xCLKIN
	600.000–668.000	n = –6, –5, –4, –3, or –2	See Note 1(b)	1xCLKIN
11 (MULTOUT = 150–167 MHz)	9.375–10.438	n = 0, 1, 2, 3, or 4	1xCLKIN	16xCLKIN
	18.750–20.875	n = –1, 0, 1, 2, or 3	1xCLKIN	8xCLKIN
	37.500–41.750	n = –2, –1, 0, 1, or 2	1xCLKIN	4xCLKIN
	75.000–83.500	n = –3, –2, –1, 0, or 1	1xCLKIN	2xCLKIN
	150.000–167.000	n = –4, –3, –2, –1, or 0	See Note 1(b)	1xCLKIN

Note:

1. The CLKOUT output is not valid for (a) MULTSEL[1:0] = 00 or MULTOUT[1:0] = 01
   (b) MULTOUT:CLKIN ratios of 1:1 (MULTOUT = 1 x CLKIN.)
2. The REFCLK input can be set to any one of the five CLKIN multiples indicated. The REFCLK input can be asynchronous to the CLKIN input, but must be within ±100 ppm of the stated CLKIN multiple.

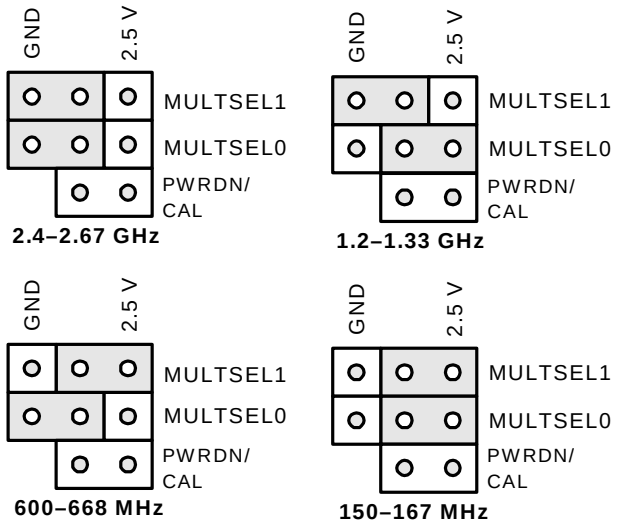


Figure 1. MULTSEL[1:0] Jumper Configurations

Loss-of-Lock (LOL)

LOL is an indicator of the relative frequency between the REFCLK input, which is nominally a multiple of CLKIN, and an internally generated multiple of CLKIN. LOL will assert when the frequency difference is greater than ±600 PPM. In order to prevent LOL from de-asserting prematurely, there is hysterisis in returning from the out of lock condition. LOL will be de-asserted (indicating a lock condition) when the frequency difference is less than ±300 PPM.

LOL is wired to a test point which is located on the upper right-hand side of the evaluation board.

Test Configuration

The characterization of clock sources typically involves measuring the output jitter or phase noise of the source. The overall output jitter is a function of the input jitter (jitter transfer) and the jitter generated (output jitter) by the internal PLL.

Jitter can be measured using several different techniques and hardware. An oscilloscope, a spectrum analyzer, and a phase-noise analyzer are three such instruments capable of measuring output jitter. A spectrum analyzer is the best choice for measuring jitter transfer.

Output Jitter

Output jitter is a measure of the output clock short-term stability. In Figure 2, either position A or B can be used when measuring this parameter.

Oscilloscope

An oscilloscope can measure jitter from the clock edges within the trigger-to-capture bandwidth. Typically the jitter measured is expressed in picoseconds (peak-to-peak and RMS) relative to the average edge position. A histogram can be used to capture the jitter distribution.

Spectrum Analyzer

A spectrum analyzer measures the power of the carrier source and its associated phase noise. Analysis of the offset power distribution provides the data from which jitter can be derived. Simple integration of the offset power distribution over the desired offset range and filtered amplitudes provides a RMS jitter value.

Phase-noise Analyzer

A phase-noise analyzer behaves similarly to a spectrum analyzer, but only provides details regarding the power offset from the carrier. Simple integration of the offset power distribution over the desired offset range and filtered amplitudes provides a RMS jitter value.

Jitter Transfer

Jitter transfer is the ratio of the input jitter spectrum to the output jitter spectrum. Comparing the power levels from the input jitter spectrum with the output jitter spectrum provides the jitter transfer details. To characterize this parameter, a modulation source is added to the synthesizer. The FM modulation frequency is the jitter frequency, and its relative amplitude on the output verses the input describes the amount transferred. In Figure 2, position A should be used when measuring this parameter.

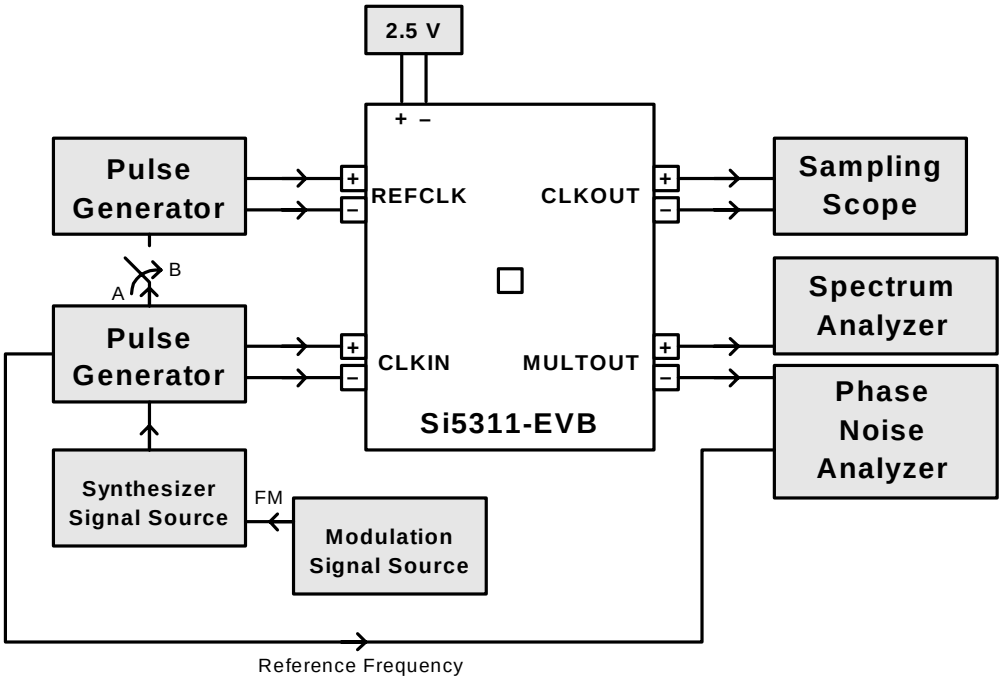


Figure 2. Test Configuration for Jitter Tolerance, Transfer, and Generation

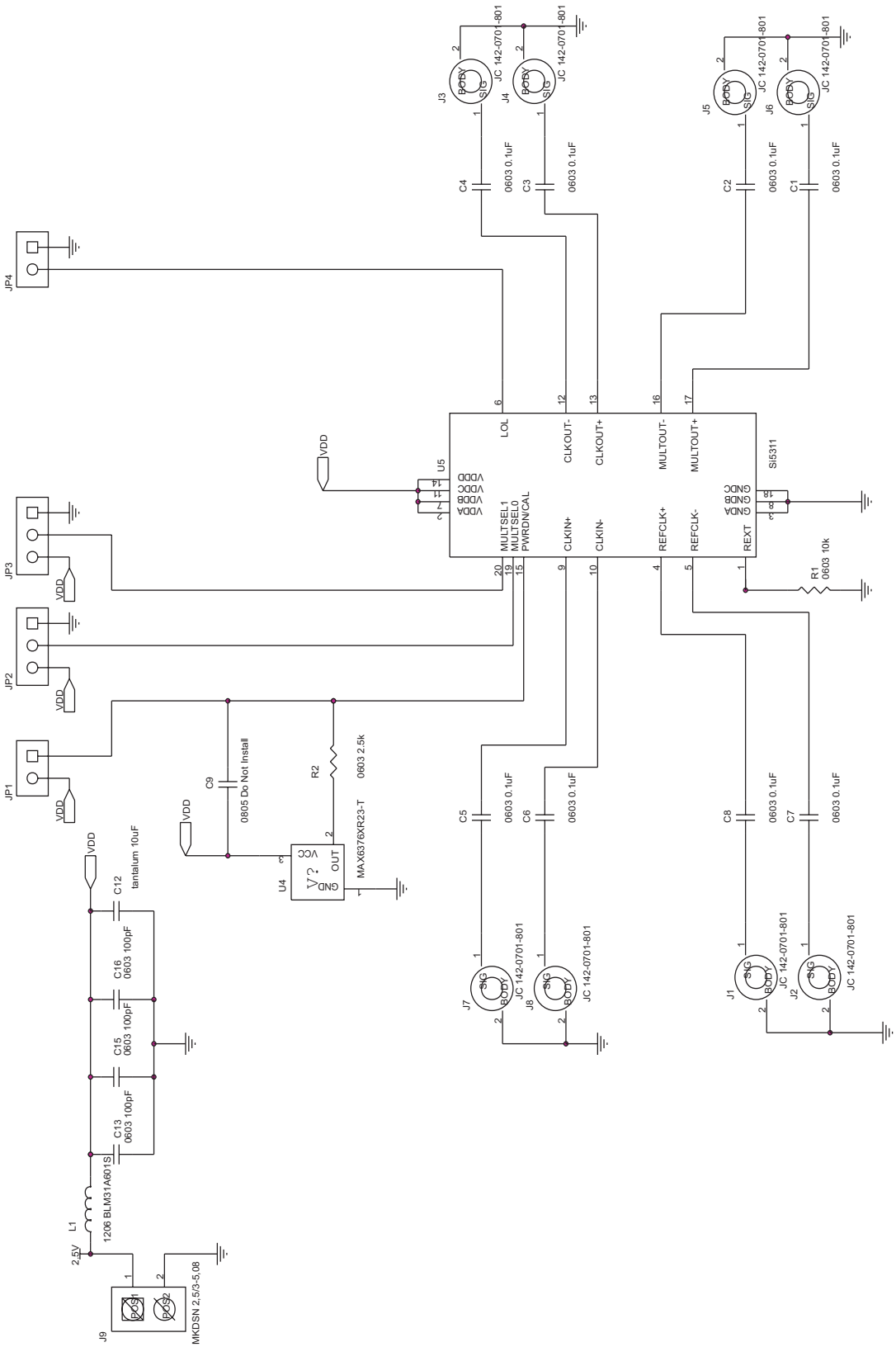


Figure 3. Si5311-EVB Schematic

Bill of Materials

Si5311EVB Assy Rev C-01 BOM			
Reference	**Part Desc**	**Part Number**	**Manufacturer**
C1,C2,C3,C4, C5,C6,C7,C8	CAP, SM, 0.1uF, 0603	C0603X7R160-104KNE	Venkel
C12	CAP, SM, 10 uF, TANTALUM, 3216	TA010TCM106KAR	Venkel
C13,C15,C16	CAP, SM, 100 pF, 16V, 0603	C0603C0G500101KNE	Venkel
JP1,JP4	CONNECTOR, HEADER, 2X1	2340-6111TN or 2380-6121T	3M
JP2,JP3	CONNECTOR, HEADER, 3X1	2340-6111TN or 2380-6121T	3M
J1,J2,J3,J4,J5, J6,J7,J8	CONNECTOR, SMA, SIDE MOUNT	901-10003	Amphenol
J9	CONNECTOR, POWER, 2 POS	1729018	Phoenix Contact
L1	RESISTOR, SM, 0 OHM, 1206	CR1206-8W-000T	Venkel
R1	RESISTOR, SM, 10K, 1%, 0603	CR0603-16W-1002FT	Venkel
R2	RESISTOR, SM, 2.55K, 1%, 0603	CR0603-16W-2551FT	Venkel
U4	MAX6376XR23-T	MAX6376XR23-T	Maxim
U5	Si5311	SI5311-BM	Silicon Laboratories
PCB	PRINTED CIRCUIT BOARD	Si5311-EVB PCB Rev C	Silicon Laboratories
No Load			
C9	SPARE,0805		

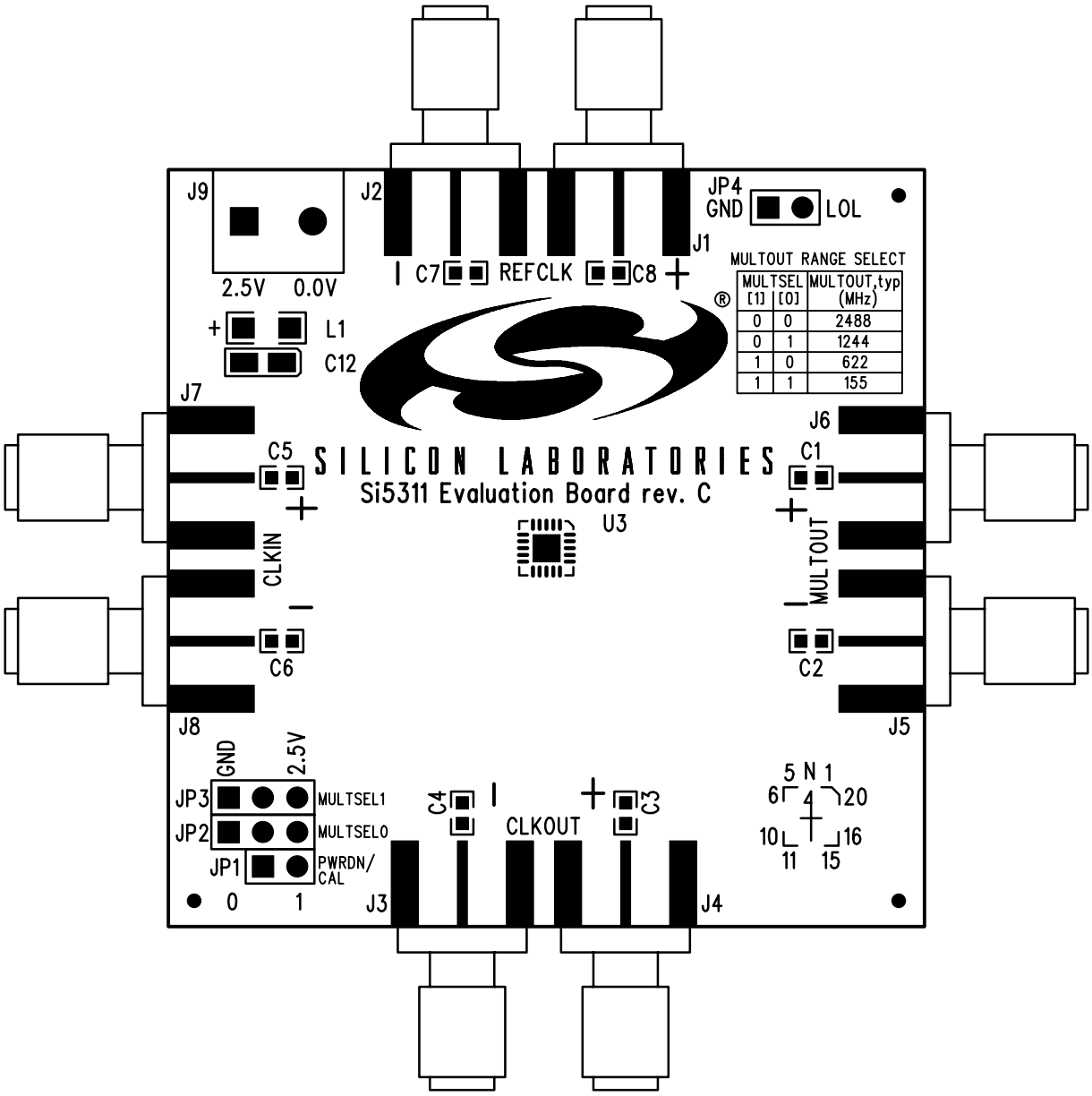


Figure 4. Si5311 Silkscreen

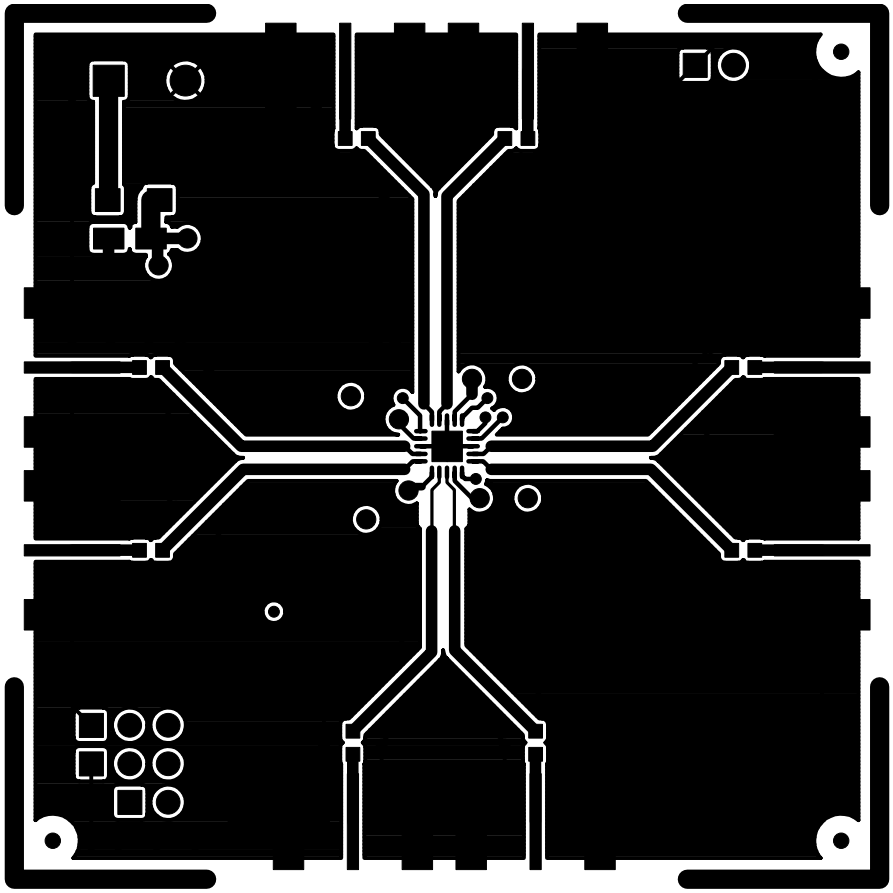


Figure 5. Si5311 Component Side

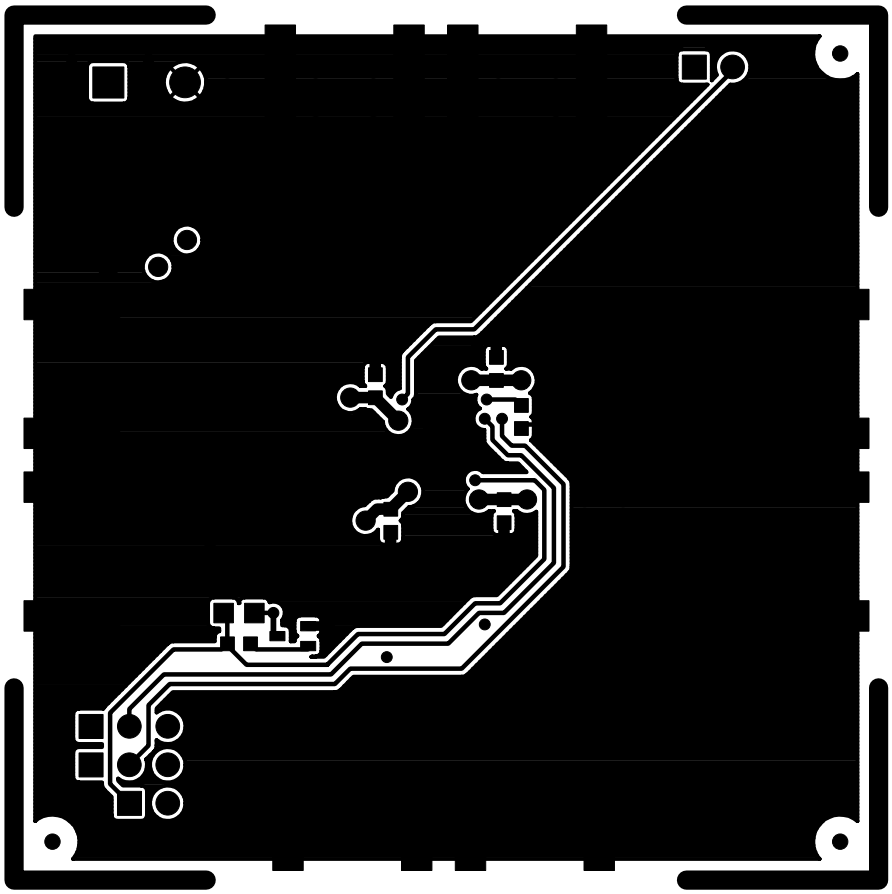


Figure 6. Si5211 Solder Side

Document Change List

Revision 0.7 to Revision 0.71

- Added bill of materials.

Evaluation Board Assembly Revision History

Assembly Level	PCB	Si5311 Device	Assembly Notes
B-01	B	B	Assemble per BOM rev B-01.
C-01	C	C	Assemble per BOM rev C-01.

Contact Information

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com