3-W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

Check for Samples :TPA6013A4

FEATURES

- **Advanced 32-Steps DC Volume Control**
  - **Steps from –40 to 18 dB**
  - **Fade Mode**
  - **Maximum Volume Setting for SE Mode**
  - **Adjustable SE Volume Control Referenced to BTL Volume Control**
- **3 W Into 3-Ω Speakers**
- **Stereo Input MUX**
- **Headphone Mode**
- **Pin-to-pin compatible with TPA6011A4 and TPA6012A4**
- **24-pin PowerPAD™ Package (PWP)**

APPLICATIONS

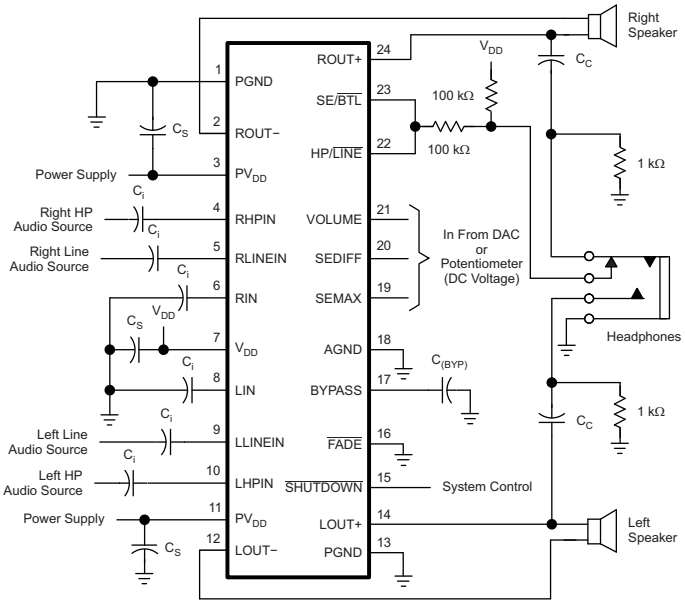
- **Notebook PC**
- **LCD Monitors**
- **Pocket PC**

DESCRIPTION

The TPA6013A4 is a stereo audio power amplifier that drives 3 W/channel of continuous RMS power into a 3-Ω load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

To simplify design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME terminal. Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

APPLICATION CIRCUIT



DC VOLUME CONTROL

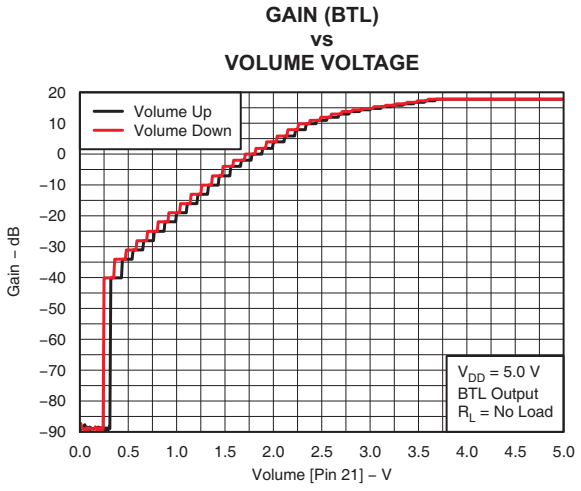


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Figure 1. Application Circuit and DC Volume Control

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PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	PACKAGE
	24-PIN TSSOP (PWP) (1)
–40°C to 85°C	TPA6013A4PWP

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6013A4PWPR).

LEAD (PB-FREE) ORDERING INFORMATION

ORDERABLE DEVICE	STATUS (1)	ECO-STATUS (2)
TPA6013A4PWPG4	Active	Pb-Free and Green
TPA6013A4PWPRG4	Active	

(1) The marketing status values are defined as follows:
- (a) **ACTIVE:** This device recommended for new designs.
- (b) **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- (c) **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- (d) **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- (e) **OBSOLETE:** TI has discontinued production of the device.

(2) **Eco-Status Information –** Additional details including specific material content can be accessed at www.ti.com/leadfree
- (a) **N/A:** Not yet available Lead (Pb)-Free, for estimated conversion dates go to www.ti.com/leadfree.
- (b) **Pb-Free:** TI defines "Lead (Pb)-Free" or "Pb-Free" to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.
- (c) **Green:** TI devices "Green" to mean Lead (Pb)-Free and in addition, uses package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{SS}	Supply voltage, V_{DD}, PV_{DD}	–0.3 V to 6 V
V_I	Input voltage	–0.3 V to V_{DD}+0.3 V
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	–40°C to 85°C
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	2.7 mW	21.8 mW/°C	1.7 W	1.4 W

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RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{SS}	Supply voltage, V_{DD}, PV_{DD}		4.0	5.5	V
V_{IH}	High-level input voltage	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{FADE}$	0.8 × V_{DD}		V
		$\overline{SHUTDOWN}$	2		V
V_{IL}	Low-level input voltage	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{FADE}$		0.6 × V_{DD}	V
		$\overline{SHUTDOWN}$		0.8	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = PV_{DD} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
| V_{OO} |	Output offset voltage (measured differentially)	V_{DD} = 5.5 V, Gain = 0 dB, SE/$\overline{BTL}$ = 0 V		2	30	mV
		V_{DD} = 5.5 V, Gain = 18 dB, SE/$\overline{BTL}$ = 0 V		2.6	50	mV
PSRR	Power supply rejection ratio	V_{DD} = PV_{DD} = 4.0 V to 5.5 V, Gain = 0 dB		–80		dB
| I_{IH} |	High-level input current (SE/$\overline{BTL}$, $\overline{FADE}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5 V, V_I = V_{DD} = PV_{DD}			1	µA
| I_{IL} |	Low-level input current (SE/$\overline{BTL}$, $\overline{FADE}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, SEDIFF, SEMAX, VOLUME)	V_{DD} = PV_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current, no load	V_{DD} = PV_{DD} = 5 V, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V		6.7	9.0	mA
		V_{DD} = PV_{DD} = 5 V, SE/$\overline{BTL}$= 5 V, $\overline{SHUTDOWN}$ = 2 V		4.5	6	
I_{DD}	Supply current, max power into a 3-Ω load	V_{DD} = 5 V = PV_{DD}, SE/$\overline{BTL}$ = 0 V, $\overline{SHUTDOWN}$ = 2 V, R_L = 3Ω, P_O = 2 W, stereo		1.5		A_{RMS}
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0.0 V		10	25	µA

OPERATING CHARACTERISTICS

T_A = 25°C, V_{DD} = PV_{DD} = 5 V, R_L = 3 Ω, Gain = 6 dB, Stereo (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, f = 1 kHz, R_L = 16 Ω (SE)			195		mW
		THD = 10%, f = 1 kHz, R_L = 16 Ω (SE)			235		mW
		THD = 1%, f = 1 kHz, R_L = 3 Ω (BTL)			2.0		W
		THD = 10%, f = 1 kHz, V_{DD} = 5.5 V, R_L =3 Ω (BTL)			3.2		
THD+N	Total harmonic distortion + noise	P_O = 0.9 W, R_L = 8 Ω (BTL), f = 20 Hz to 20 kHz			<0.1%		
		P_O = 0.1 W, R_L = 16 Ω (SE), f = 20 Hz to 20 kHz			0.03%		
V_{OH}	High-level output voltage	R_L = 8 Ω, Measured between output and V_{DD} = 5.5 V				700	mV
V_{OL}	Low-level output voltage	R_L = 8 Ω, Measured between output and GND, V_{DD} = 5.5 V				400	mV
$V_{(Bypass)}$	Bypass voltage (Nominally V_{DD}/2)	Measured at pin 17, No load, V_{DD} = 5.5 V		2.65	2.75	2.85	V
	Supply ripple rejection ratio	f = 1 kHz, Gain = 0 dB, $C_{(BYP)}$ = 1 µF	BTL (4Ω)		–66		dB
			SE (32Ω)		–60		dB
	Crosstalk		BTL		110		dB
			SE		102		dB
	Noise output voltage	f = 20 Hz to 20 kHz, Gain = 0 dB, $C_{(BYP)}$ = 1 µF	BTL		36		$µV_{RMS}$
Z_I	Input impedance (see Figure 17)	VOLUME = 5 V			12		kΩ

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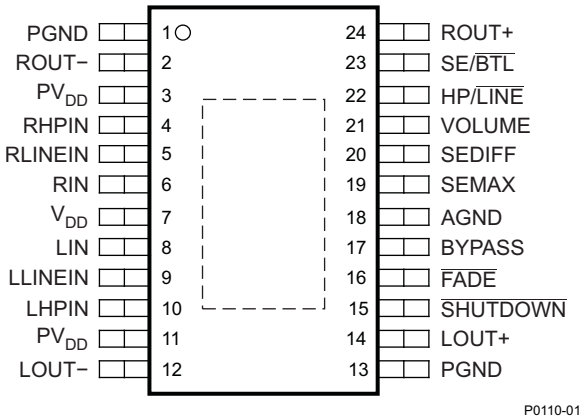
PWP Package
(Top View)



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PIN Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
PGND	1, 13	–	Power ground
LOUT–	12	O	Left channel negative audio output
PV_{DD}	3, 11	–	Supply voltage terminal for power stage
LHPIN	10	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
LLINEIN	9	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
LIN	8	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
V_{DD}	7	–	Supply voltage terminal
RIN	6	I	Common right channel input for fully differential input. AC ground for single-ended inputs.
RLINEIN	5	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
RHPIN	4	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
ROUT–	2	O	Right channel negative audio output
ROUT+	24	O	Right channel positive audio output
$\overline{\text{SHUTDOWN}}$	15	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
$\overline{\text{FADE}}$	16	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal
BYPASS	17	I	Tap to voltage divider for internal mid-supply bias generator used for analog reference
AGND	18	–	Analog power supply ground
SEMAX	19	I	Sets the maximum volume for single ended operation. DC voltage range is 0 to V_{DD}.
SEDIFF	20	I	Sets the difference between BTL volume and SE volume. DC voltage range is 0 to V_{DD}.
VOLUME	21	I	Terminal for dc volume control. DC voltage range is 0 to V_{DD}.
HP/$\overline{\text{LINE}}$	22	I	Input MUX control. When logic high, RHPIN and LHPIN inputs are selected. When logic low, RLINEIN and LLINEIN inputs are selected.
SE/$\overline{\text{BTL}}$	23	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected.
LOUT+	14	O	Left channel positive audio output.

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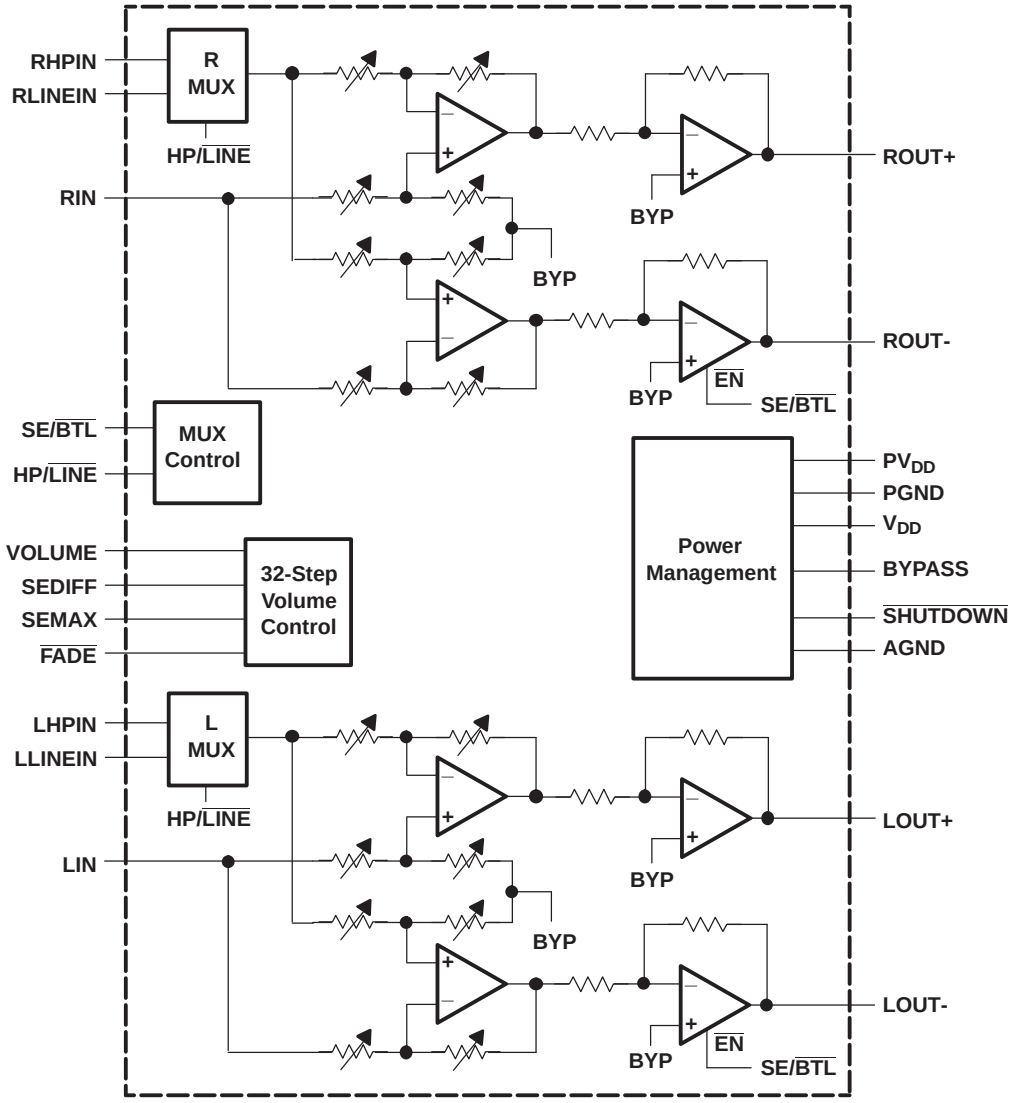
FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor wipers are adjusted with 32-step volume control.

Table 1. DC Volume Control (BTL Mode, V_{DD} = 5 V)(1)

VOLUME (PIN 21)		GAIN OF AMPLIFIER (Typ) (2)
FROM (V)	TO (V)	
0.00	0.26	–85
0.33	0.37	–40
0.44	0.48	–34
0.56	0.59	–31
0.67	0.70	–28
0.78	0.82	–25
0.89	0.93	–22
1.01	1.04	–19
1.12	1.16	–16
1.23	1.27	–13
1.35	1.38	–10
1.46	1.49	–7
1.57	1.60	–4
1.68	1.72	–2
1.79	1.83	–0
1.91	1.94	2
2.02	2.06	4
2.13	2.17	6
2.25	2.28	8
2.36	2.39	10
2.47	2.50	11
2.58	2.61	12
2.70	2.73	13
2.81	2.83	14
2.92	2.95	14.5
3.04	3.06	15
3.15	3.17	15.5
3.26	3.29	16
3.38	3.40	16.5
3.49	3.51	17
3.60	3.63	17.5
3.71	5.00	18

(1) For other values of V_{DD}, scale the voltage values in the table by a factor of V_{DD}/5.
(2) Tested in production. Remaining gain steps are specified by design.

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Table 2. DC Volume Control (SE Mode, V_{DD} = 5 V)(1)

SE_VOLUME = VOLUME - SEDIFF or SEMAX		GAIN OF AMPLIFIER (Typ)
FROM (V)	TO (V)	
0.00	0.26	–85(2)
0.33	0.37	–46
0.44	0.48	–40
0.56	0.59	–37
0.67	0.70	–34
0.78	0.82	–31
0.89	0.93	–28
1.01	1.04	–25
1.12	1.16	–22
1.23	1.27	–19
1.35	1.38	–16
1.46	1.49	–13
1.57	1.60	–10
1.68	1.72	–8
1.79	1.83	–6(2)
1.91	1.94	–4
2.02	2.06	–2
2.13	2.17	0(2)
2.25	2.28	2
2.36	2.39	4
2.47	2.50	5
2.58	2.61	6 (2)
2.70	2.73	7
2.81	2.83	8
2.92	2.95	8.5
3.04	3.06	9
3.15	3.17	9.5
3.26	3.29	10
3.38	3.40	10.5
3.49	3.51	11
3.60	3.63	11.5
3.71	5.00	12

(1) For other values of V_{DD}, scale the voltage values in the table by a factor of V_{DD}/5.
(2) Tested in production. Remaining gain steps are specified by design.

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TYPICAL CHARACTERISTICS

Test conditions (unless otherwise noted) for typical operating performance:
V_{DD} = 5.0 V, C_{IN} = 1 µF, C_{BYPASS} = 1 µF, T_A = 27°C, SHUTDOWN = V_{DD}

Table of Graphs

	Gain (BTL)	vs Volume voltage	Figure 1
THD+N	Total harmonic distortion plus noise (BTL)	vs Frequency	Figure 2, Figure 3, Figure 4
		vs Output power	Figure 7, Figure 8, Figure 9
THD+N	Total harmonic distortion plus noise (SE)	vs Frequency	Figure 5, Figure 6
		vs Output power	Figure 10
		vs Output voltage	Figure 11
P_D	Total power dissipation (BTL)	vs Total output power	Figure 12
P_D	Total power dissipation (SE)	vs Total output power	Figure 13
	Crosstalk (BTL)	vs Frequency	Figure 14
	Crosstalk (SE)	vs Frequency	Figure 15
	Inter-channel crosstalk	vs Frequency	Figure 16
	Input impedance	vs Gain	Figure 17
PSRR	Power supply rejection ratio (BTL)	vs Frequency	Figure 18
PSRR	Power supply rejection ratio (SE)	vs Frequency	Figure 19
I_{DD}	Supply current (BTL)	vs Total output power	Figure 20
I_{DD}	Supply current (SE)	vs Total output power	Figure 21

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

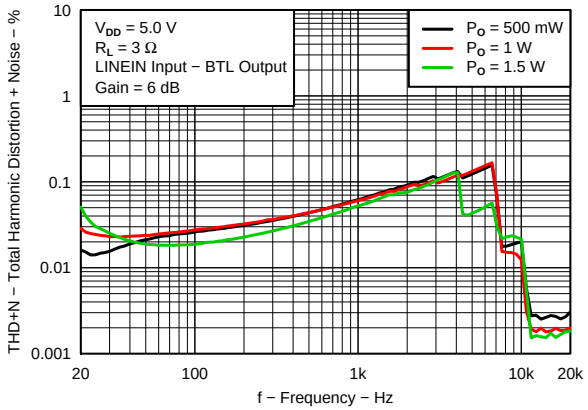

Figure 2.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

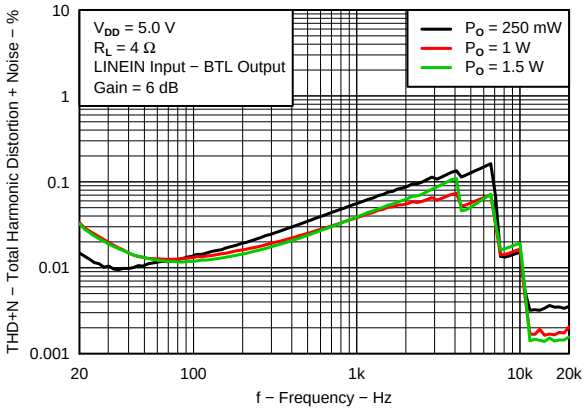

Figure 3.

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TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
FREQUENCY

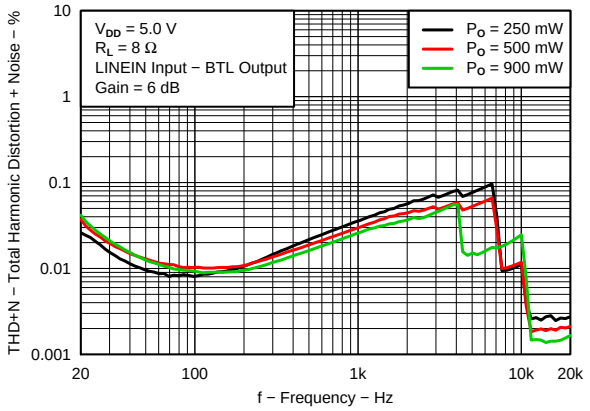

Figure 4.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

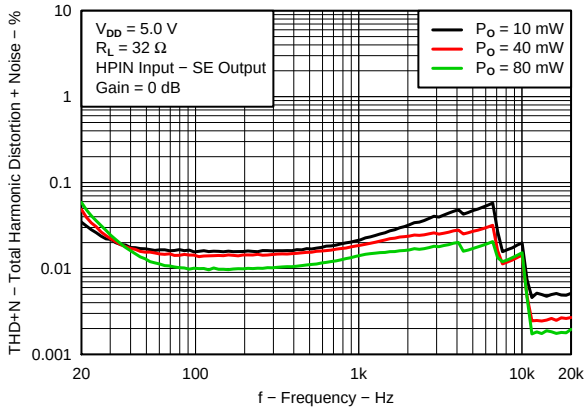

Figure 5.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
FREQUENCY

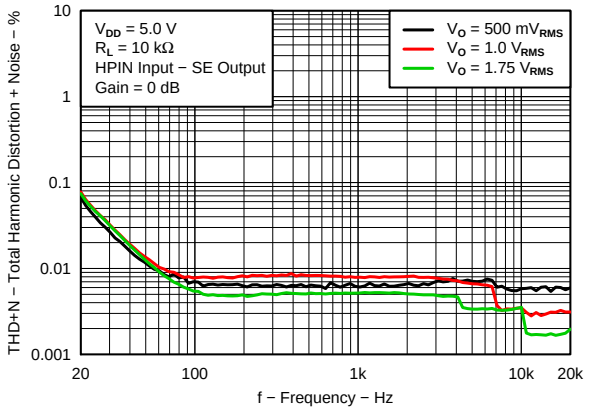

Figure 6.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

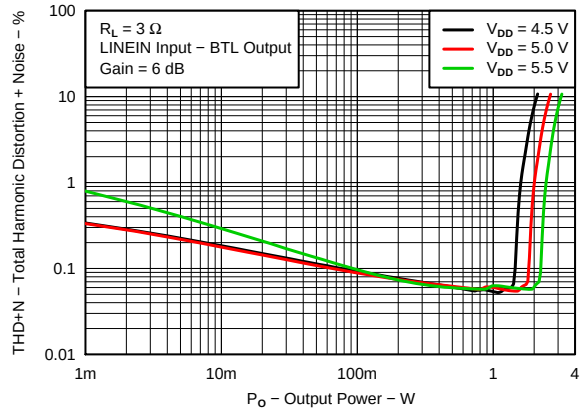

Figure 7.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

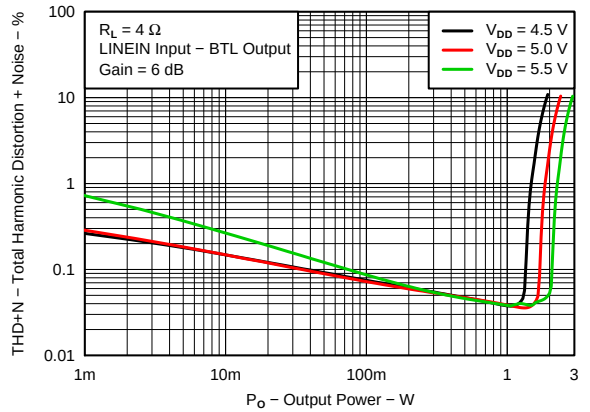

Figure 8.

TOTAL HARMONIC DISTORTION + NOISE (BTL)
vs
OUTPUT POWER

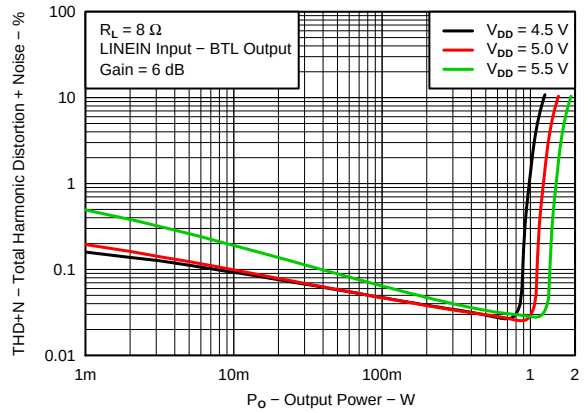

Figure 9.

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TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
OUTPUT POWER

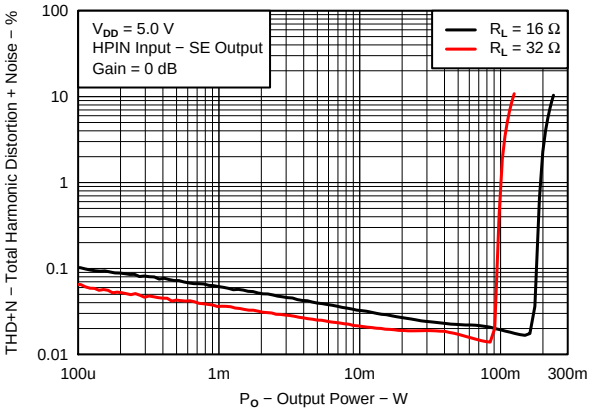

Figure 10.

TOTAL HARMONIC DISTORTION + NOISE (SE)
vs
OUTPUT VOLTAGE

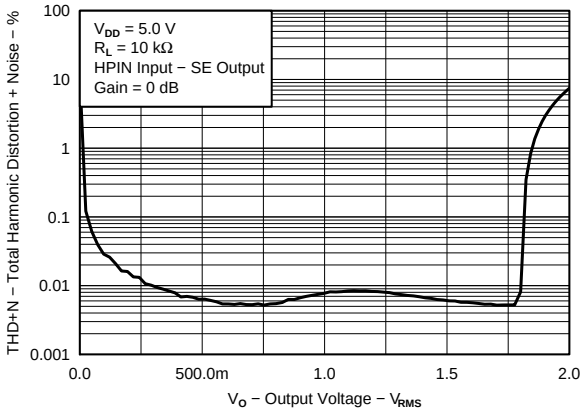

Figure 11.

TOTAL POWER DISSIPATION (BTL)
vs
TOTAL OUTPUT POWER

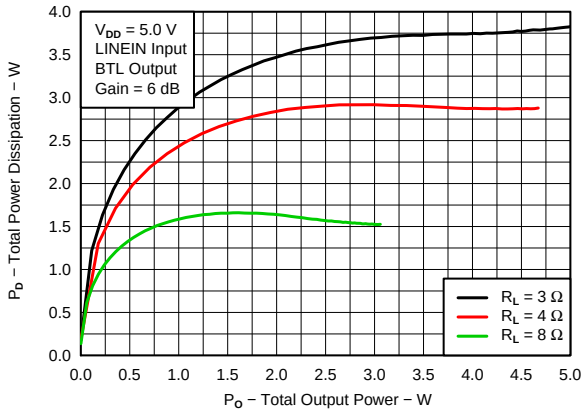

Figure 12.

TOTAL POWER DISSIPATION (SE)
vs
TOTAL OUTPUT POWER

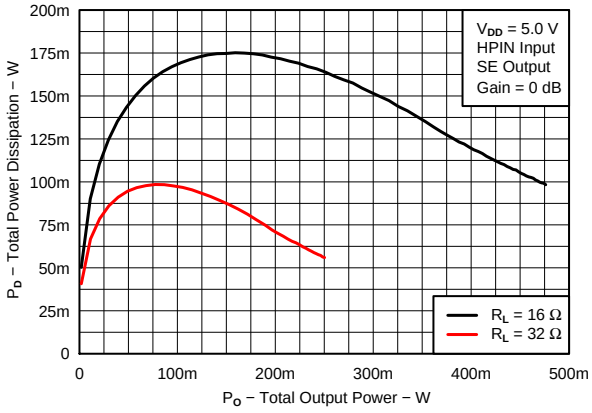

Figure 13.

CROSSTALK (BTL)
vs
FREQUENCY

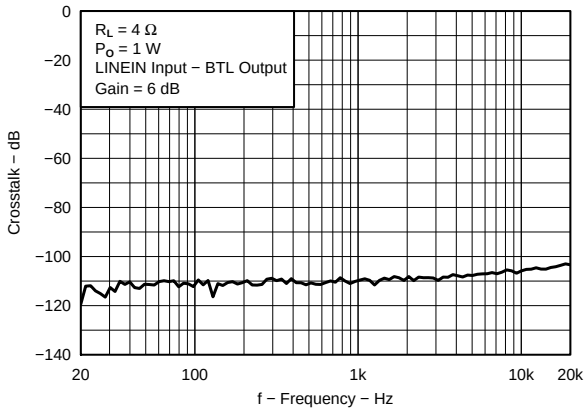

Figure 14.

CROSSTALK (SE)
vs
FREQUENCY

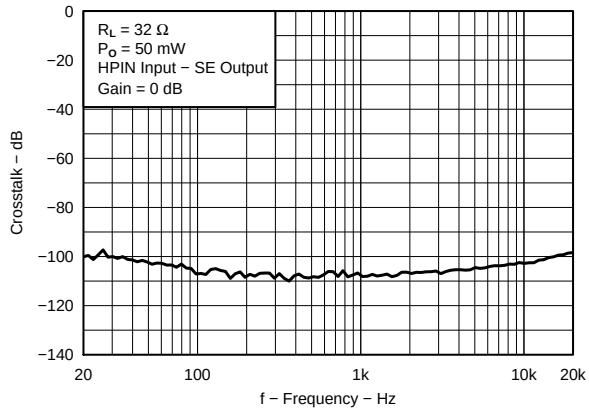

Figure 15.

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INTER-CHANNEL CROSSTALK vs FREQUENCY

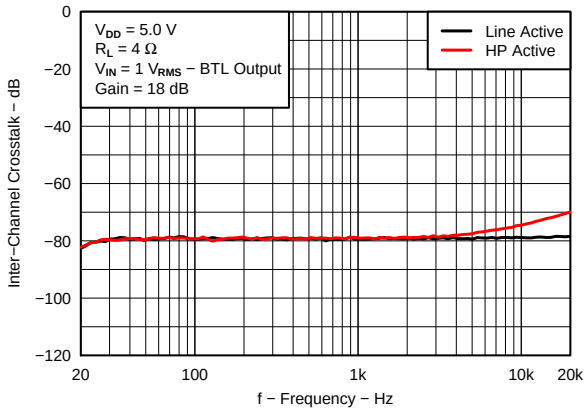

Figure 16.

INPUT IMPEDANCE vs GAIN

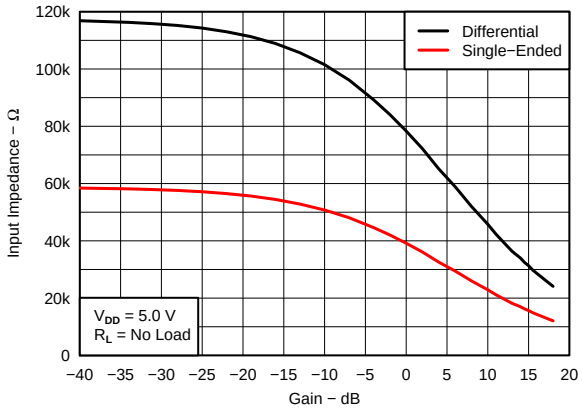

Figure 17.

POWER SUPPLY REJECTION RATIO (BTL) vs FREQUENCY

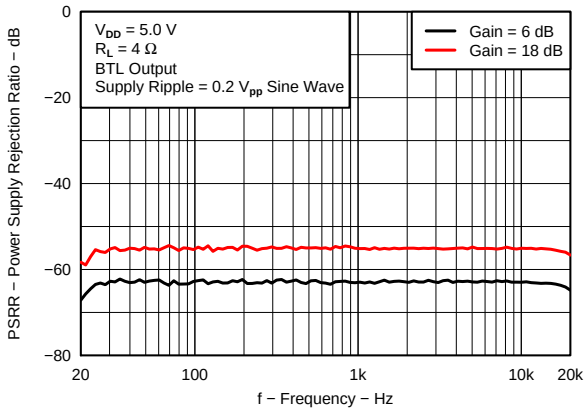

Figure 18.

POWER SUPPLY REJECTION RATIO (SE) vs FREQUENCY

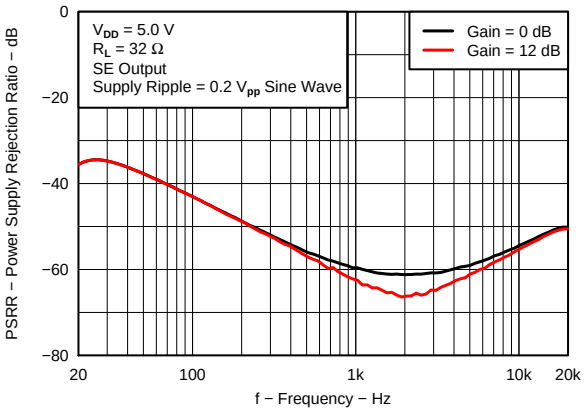

Figure 19.

SUPPLY CURRENT (BTL) vs TOTAL OUTPUT POWER

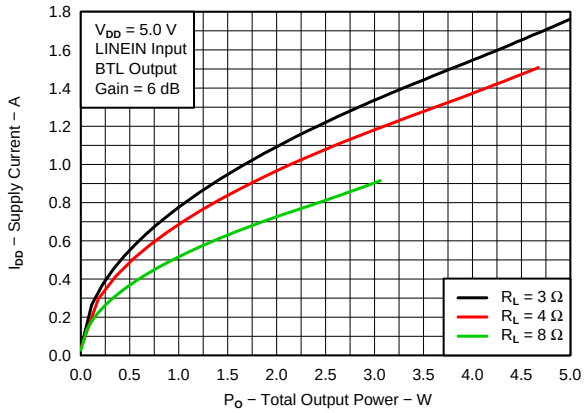

Figure 20.

SUPPLY CURRENT (SE) vs TOTAL OUTPUT POWER

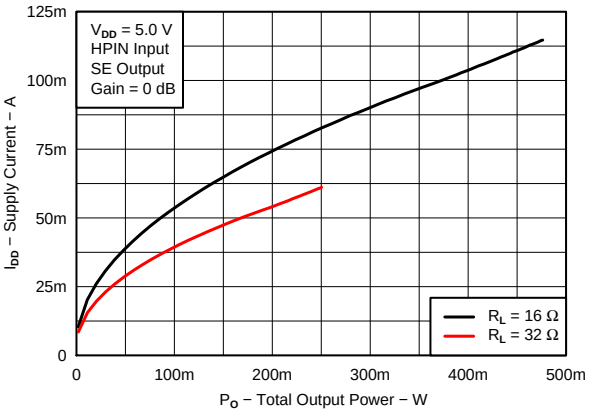

Figure 21.

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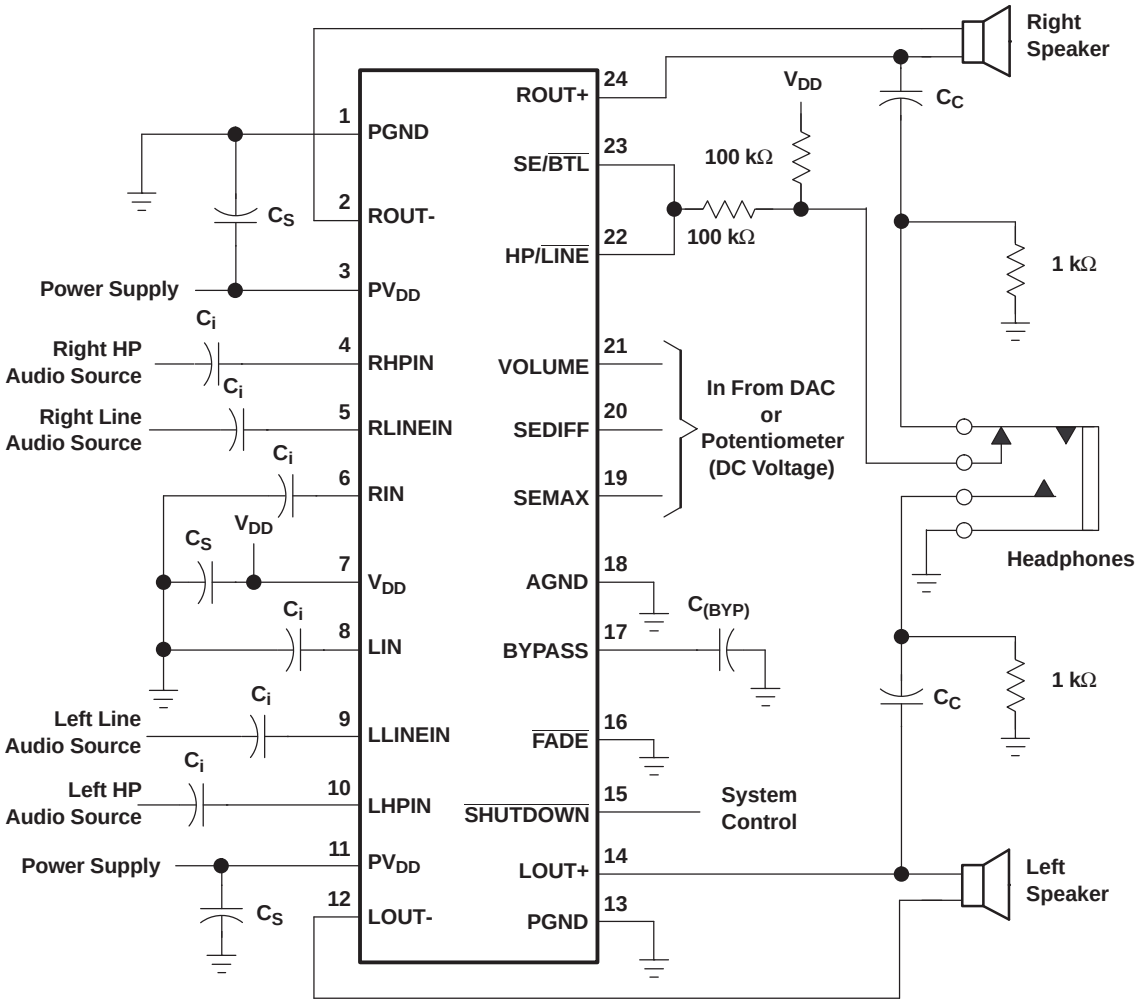
APPLICATION INFORMATION

SELECTION OF COMPONENTS

Figure 22 and Figure 23 are schematic diagrams of typical notebook computer application circuits.



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 22. Typical TPA6013A4 Application Circuit Using Single-Ended Inputs and Input MUX

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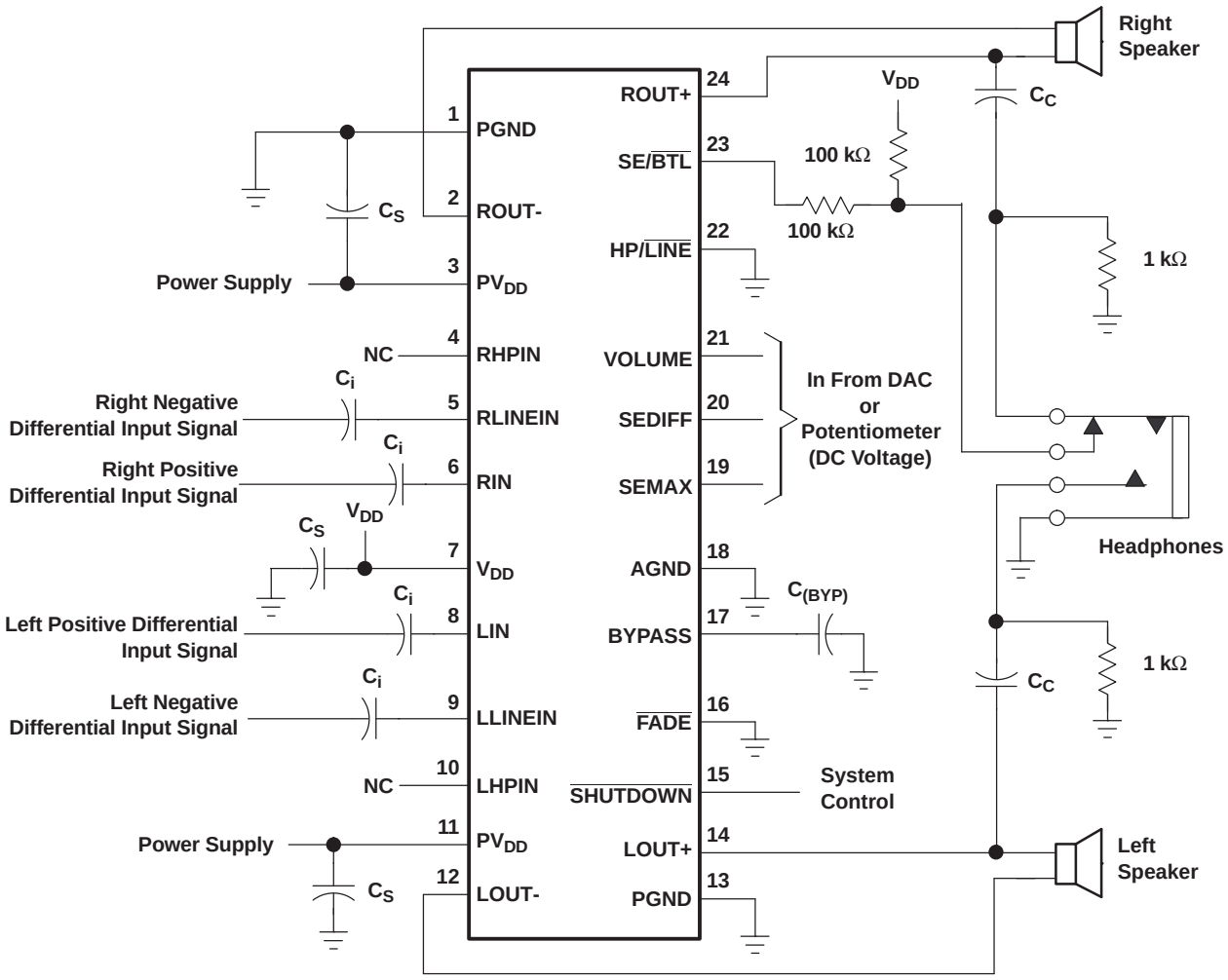

A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 23. Typical TPA6013A4 Application Circuit Using Differential Inputs

SE/$\overline{\text{BTL}}$ OPERATION

The ability of the TPA6013A4 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA6013A4, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT– and ROUT–. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA6013A4 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA6013A4 as an SE driver from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-third in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 24. The trip level for the SE/$\overline{\text{BTL}}$ input can be found in the *recommended operating conditions* table.

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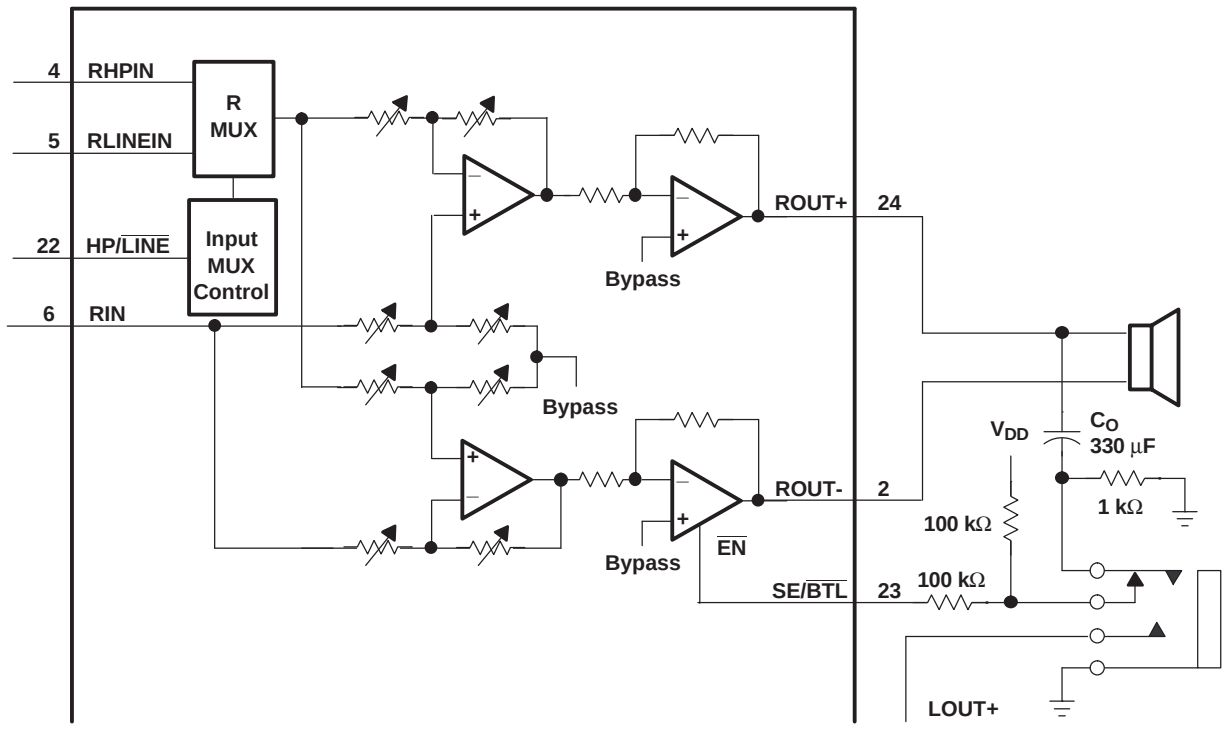

Figure 24. TPA6013A4 Resistor Divider Network Circuit

Using a 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_o) into the headphone jack.

HP/$\overline{\text{LINE}}$ OPERATION

The HP/$\overline{\text{LINE}}$ input controls the internal input multiplexer (MUX). Refer to the block diagram in Figure 24. This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the HP/$\overline{\text{LINE}}$ control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/$\overline{\text{BTL}}$ pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/$\overline{\text{BTL}}$ control input to the HP/$\overline{\text{LINE}}$ input.

When this input is logic high, the RHPIN and LHPIN inputs are selected. When this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 3 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

SHUTDOWN MODES

The TPA6013A4 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 µA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

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Table 3. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS (1)			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

(1) Inputs should never be left unconnected.

$\overline{\text{FADE}}$ OPERATION

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the $\overline{\text{FADE}}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

When a logic low is applied to the $\overline{\text{FADE}}$ pin and a logic low is then applied on the $\overline{\text{SHUTDOWN}}$pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58 Hz, this equates to 34 ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 18 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps, and multiplying by the time per step, or 34 ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of $V_{DD}/2$ to ground. This time is dependent on the value of the bypass capacitor. For a 0.47-µF capacitor that is used in the application diagram in Figure 22, the time is approximately 500 ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-µF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-µF capacitor, or 1 second. Figure 25 is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at V_{DD} when the amplifier is shut down.

When a logic high is placed on the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{FADE}}$ pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of $V_{DD}/2$, the gain increases from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

In the fade-off mode, the amplifier stores the gain value prior to starting the shutdown sequence. The output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value stored in memory. Figure 26 is a waveform captured at the output during the shutdown sequence when the part is in the fade-off mode. The gain is set to the highest level, and the output is at V_{DD} when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the $\overline{\text{FADE}}$pin does not change the power-up sequence. Upon a power-up condition, the TPA6013A4 begins in the lowest gain setting and steps up every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

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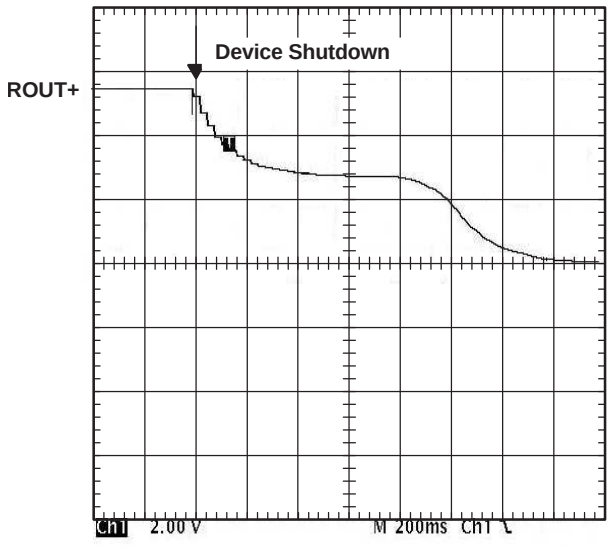

Figure 25. Shutdown Sequence in the Fade-on Mode

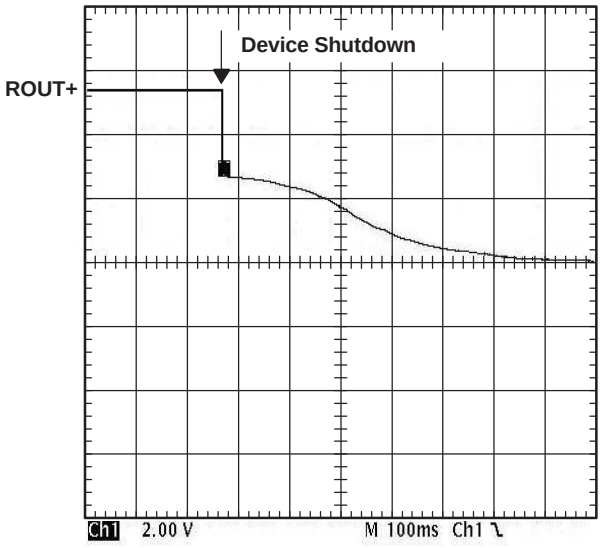

Figure 26. Shutdown Sequence in the Fade-off Mode

VOLUME, SEDIFF, AND SEMAX OPERATION

Three pins labeled VOLUME, SEDIFF, and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceed V_{DD}.

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltages listed in the table are for V_{DD} = 5 V. For a different V_{DD}, the values in the table scale linearly. If V_{DD} = 4 V, multiply all the voltages in the table by 4 V/5 V, or 0.8.

The TPA6013A4 allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the singe-ended gain proportional to the gain set by the voltage on the VOLUME pin. When SEDIFF = 0 V, the difference between the BTL gain and the SE gain is 6 dB. Refer to the section labeled *bridge-tied load versus single-ended load* for an explanation on why the gain in BTL mode is 2x that of single-ended mode, or 6dB greater. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 18 dB, the gain in the headphone channel is fixed at 12 dB. This level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode.

The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 27. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltages listed in the table are for V_{DD} = 5 V. The values must be scaled for other values of V_{DD}.

Table 1 and Table 2 show a range of voltages for each gain step. There is a gap in the voltage between each gain step. This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction. The trip point, where the gain

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actually changes, is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in Table 1 and Table 2 can also be thought of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing. If using a DAC to control the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 28. The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

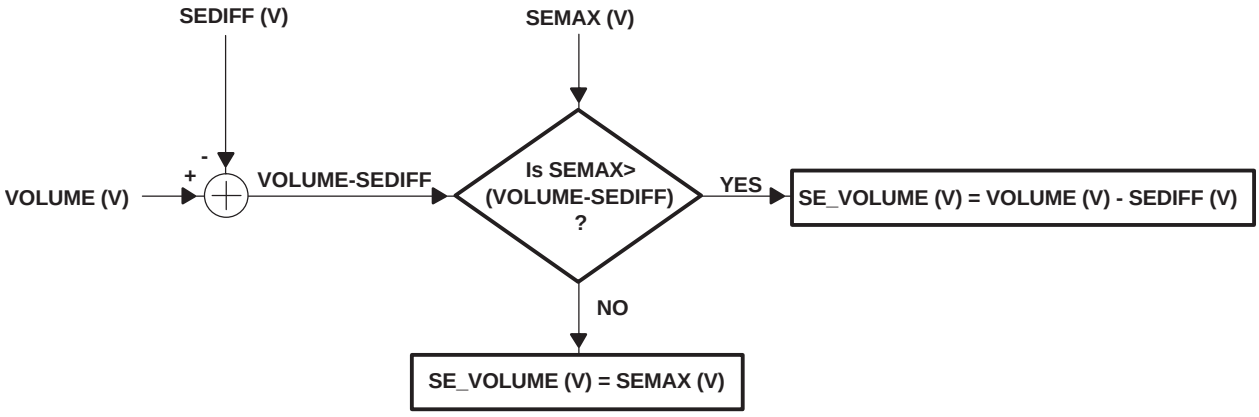


Figure 27. Block Diagram of SE Volume Control

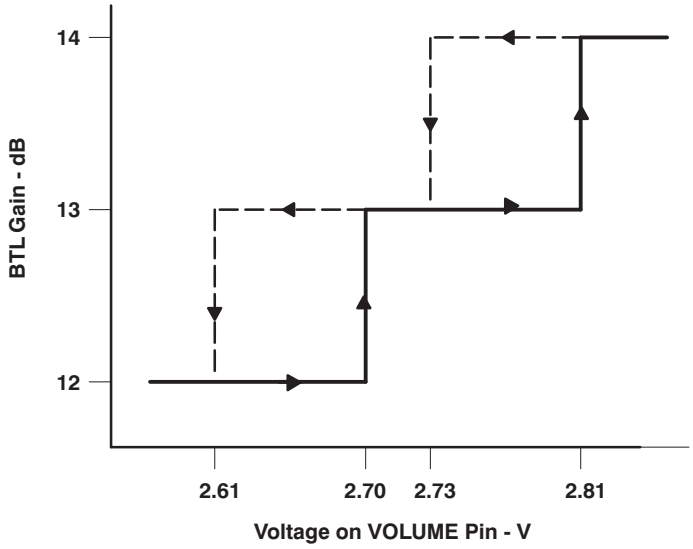


Figure 28. DC Volume Control Operation

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times.

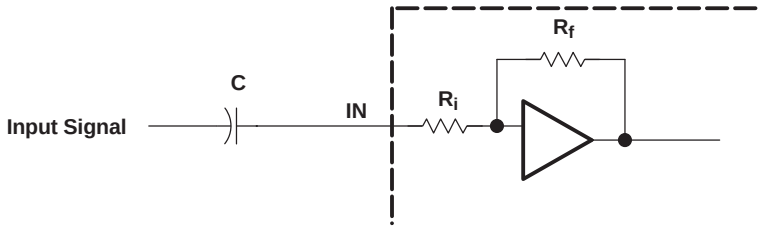


Figure 29. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 17.

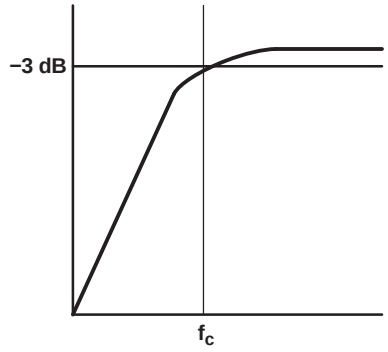
The –3-dB frequency can be calculated using Equation 1.

$$f_{-3\ dB} = \frac{1}{2\pi CR_i} \quad (1)$$

INPUT CAPACITOR, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (R_i) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi R_i C_i} \quad (2)$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 70 kΩ and the specification calls for a flat-bass response down to 40 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi R_i f_c} \quad (3)$$

In this example, C_i is 56.8 nF, so one would likely choose a value in the range of 56 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

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POWER SUPPLY DECOUPLING, $C_{(S)}$

The TPA6013A4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(BYP)}$

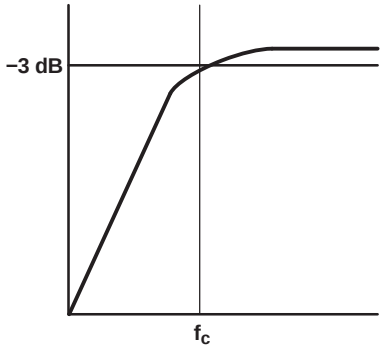
The midrail bypass capacitor ($C_{(BYP)}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{(BYP)}$) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance. For the best pop performance, choose a value for $C_{(BYP)}$ that is equal to or greater than the value chosen for C_i. This ensures that the input capacitors are charged up to the midrail voltage before $C_{(BYP)}$ is fully charged to the midrail voltage.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In the typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_{(C)}} \tag{4}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads vary from 3Ω ,4 Ω, 8Ω, 32Ω , 10 kΩ, and 47 kΩ. Table 4 summarizes the frequency response characteristics of each configuration.

Table 4. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

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As Table 4 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

BRIDGE-TIED LOAD vs SINGLE-ENDED LOAD

Figure 30 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6013A4 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging 2 × $V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (5)$$

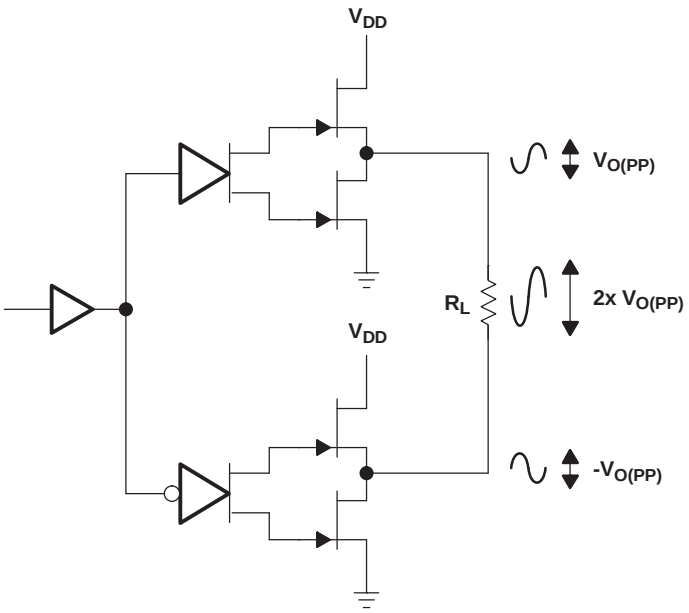

Figure 30. Bridge-Tied Load Configuration

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In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 31. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33μF to 1000μF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

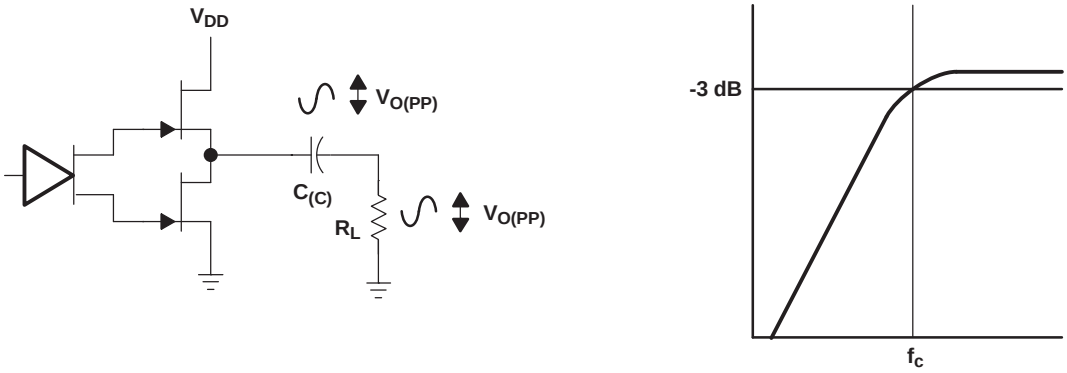

Figure 31. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

SINGLE-ENDED OPERATION

In SE mode (see Figure 31), the load is driven from the primary amplifier output for each channel (OUT+).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and effectively reduces the amplifier's gain by 6 dB.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sine-wave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 32).

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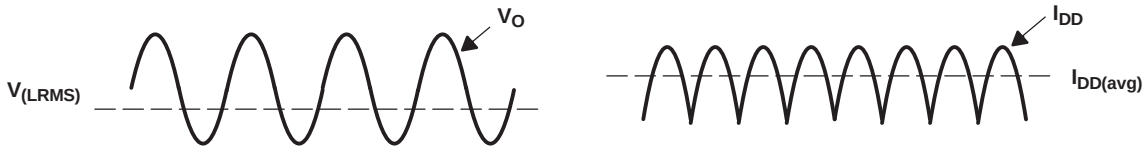

Figure 32. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\,[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\,V_{DD}\,V_P}{\pi\,R_L} \tag{7}$$

substituting P_L and P_{SUP} into Equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\,R_L}}{\frac{2\,V_{DD}\,V_P}{\pi\,R_L}} = \frac{\pi\,V_P}{4\,V_{DD}}$$

Where:

$$V_P = \sqrt{2\,P_L\,R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\,\sqrt{2\,P_L\,R_L}}{4\,V_{DD}}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

(8)

Table 5 employs Equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

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Table 5. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47(1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA6013A4 data sheet, one can see that when the TPA6013A4 is operating from a 5-V supply into a 3-Ω speaker, that 4-W peaks are available. Use equation 9 to convert watts to dB.

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4 \text{ W}}{1 \text{ W}} = 6 \text{ dB} \tag{9}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

- 6 dB – 15 dB = –9 dB (15-dB crest factor)
- 6 dB – 12 dB = –6 dB (12-dB crest factor)
- 6 dB – 9 dB = –3 dB (9-dB crest factor)
- 6 dB – 6 dB = 0 dB (6-dB crest factor)
- 6 dB – 3 dB = 3 dB (3-dB crest factor)

To convert dB back into watts use equation 10.

$$P_W = 10^{PdB/10} \times P_{ref}$$

$$= 63 \text{ mW (18-db crest factor)}$$
$$= 125 \text{ mW (15-db crest factor)}$$
$$= 250 \text{ mW (12-db crest factor)}$$
$$= 500 \text{ mW (9-db crest factor)}$$
$$= 1000 \text{ mW (6-db crest factor)}$$
$$= 2000 \text{ mW (3-db crest factor)} \tag{10}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the worst case, which is 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications significantly affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA6013A4 and maximum ambient temperatures is shown in Table 6.

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Table 6. TPA6013A4 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1 W (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 7. TPA6013A4 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3-dB crest factor)	0.55	100°C
2.5	1000 mW (4-dB crest factor)	0.62	94°C
2.5	500 mW (7-dB crest factor)	0.59	97°C
2.5	250 mW (10-dB crest factor)	0.53	102°C

The maximum dissipated power ($P_{D(max)}$) is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating $P_{D(max)}$ may be used for an 8-Ω application.

$$P_{D(max)} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3-Ω load, the $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the PWP package is shown in the *dissipation rating table*. Use equation 12 to convert this to $\theta_{JA.}$.

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel, so the dissipated power needs to be doubled for two channel operation. Given θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 13. The maximum recommended junction temperature for the TPA6013A4 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A\,\text{Max} &= T_J\,\text{Max} - \Theta_{JA}\,P_D \\ &= 150 - 45(0.6 \times 2) = 96°C \text{ (15-dB crest factor)} \end{aligned} \tag{13}$$

NOTE

Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.

Table 6 and Table 7 show that some applications require no airflow to keep junction temperatures in the specified range. The TPA6013A4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 6 and Table 7 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers increases the thermal performance by increasing amplifier efficiency.

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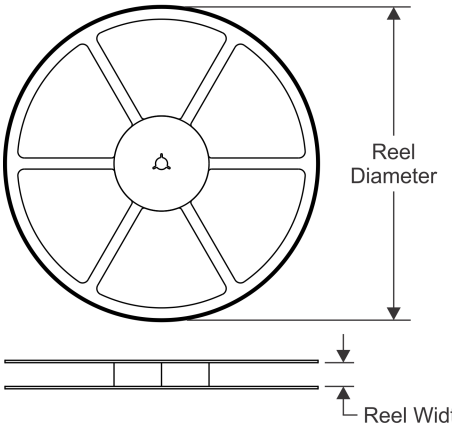
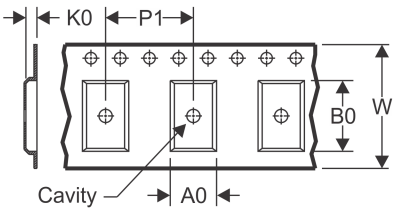
TAPE AND REEL INFORMATION

REEL DIMENSIONS

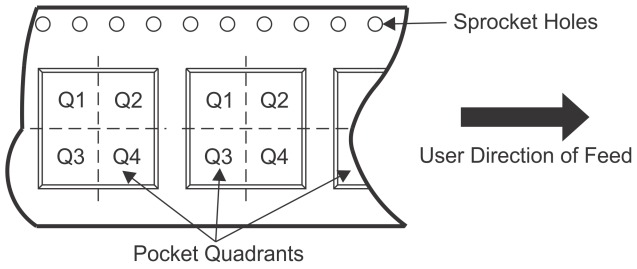


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

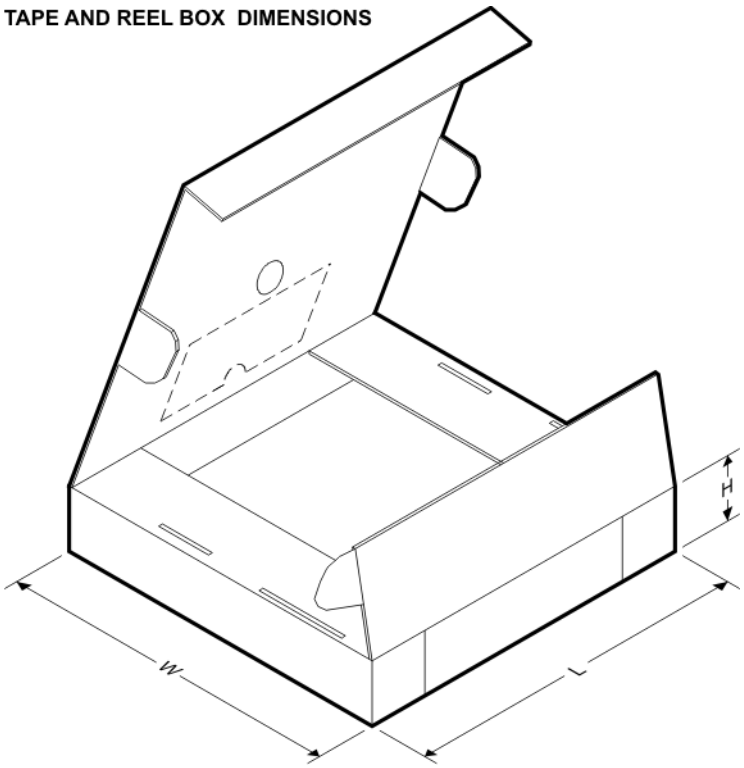
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6013A4PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

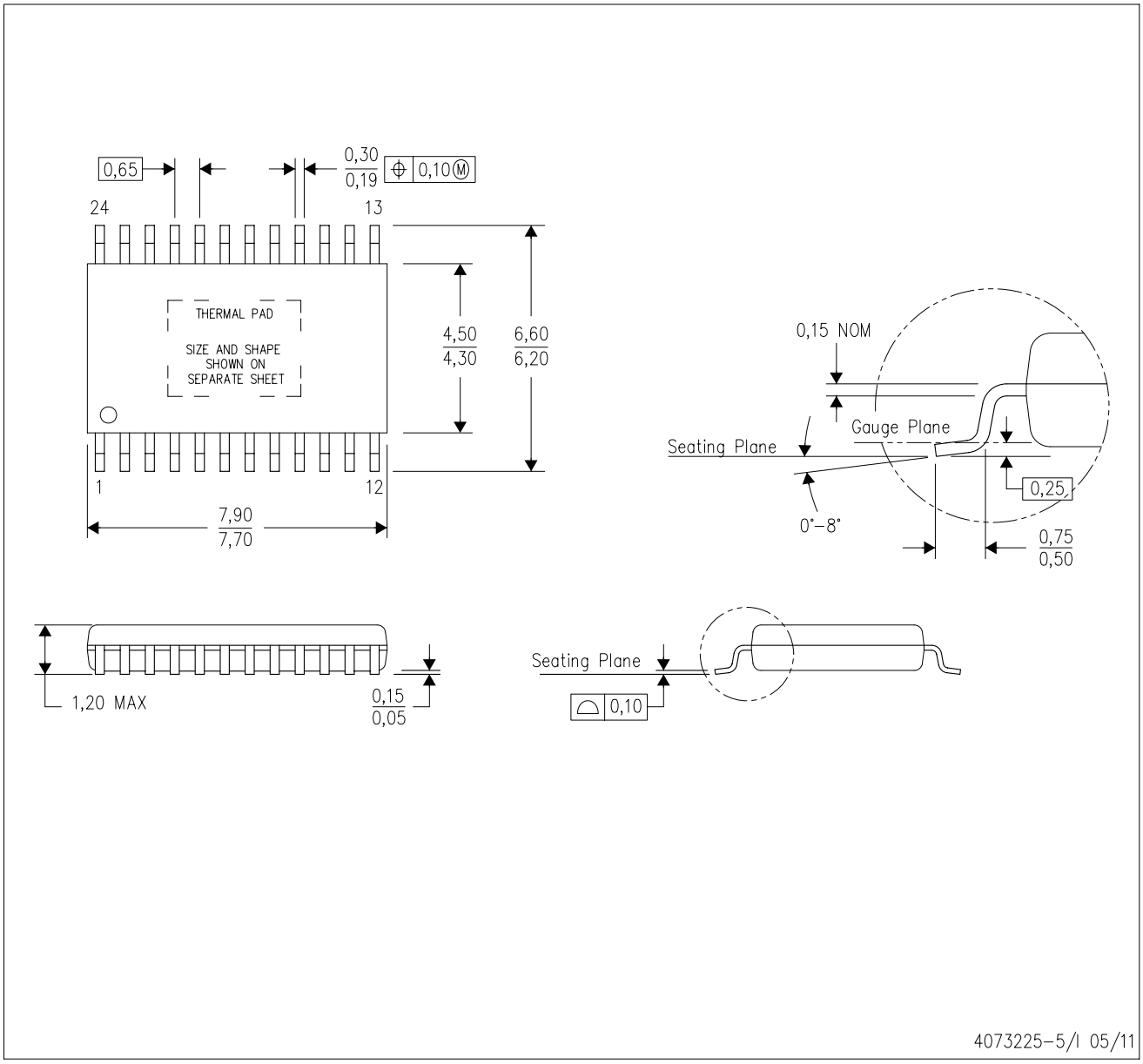
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6013A4PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

GENERIC PACKAGE VIEW

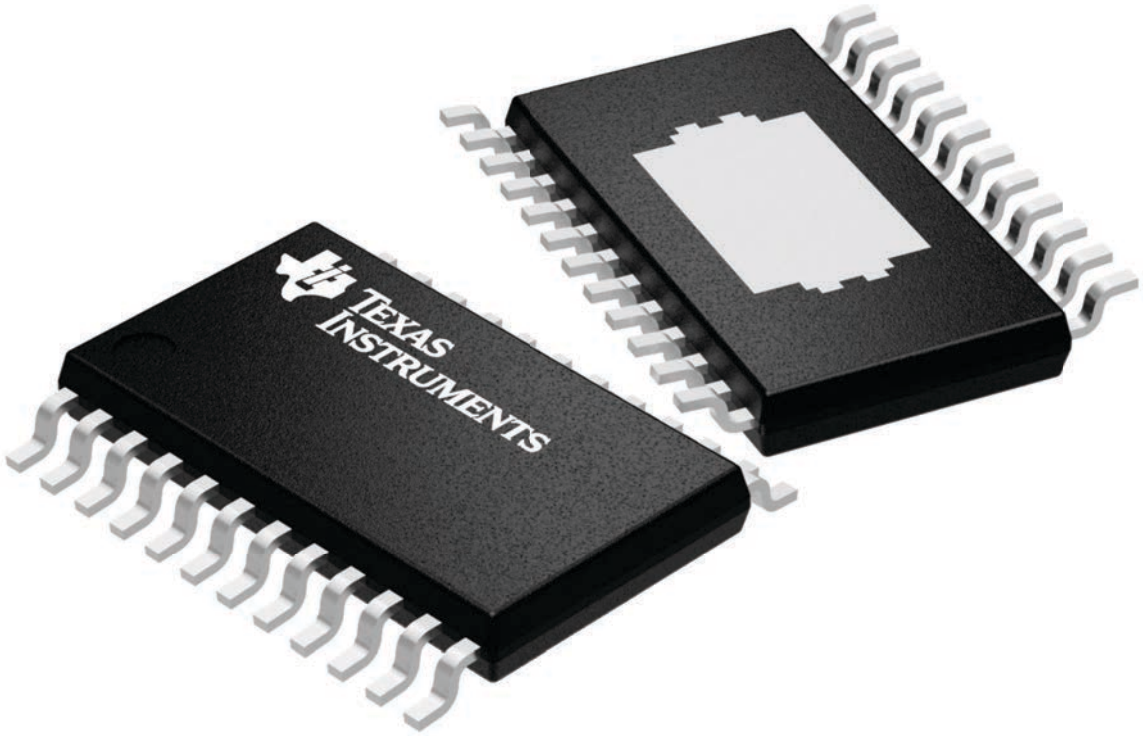
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



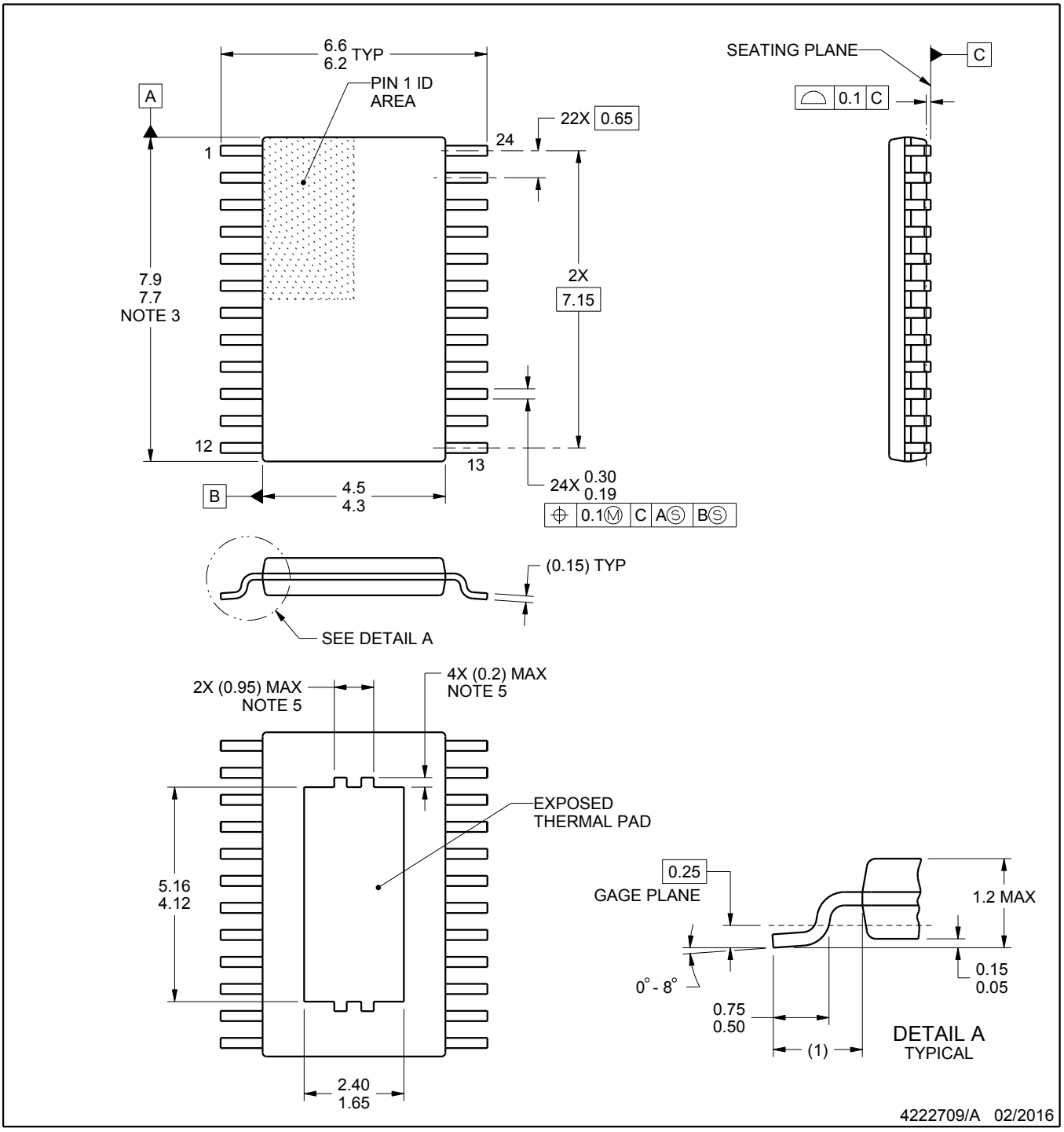
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

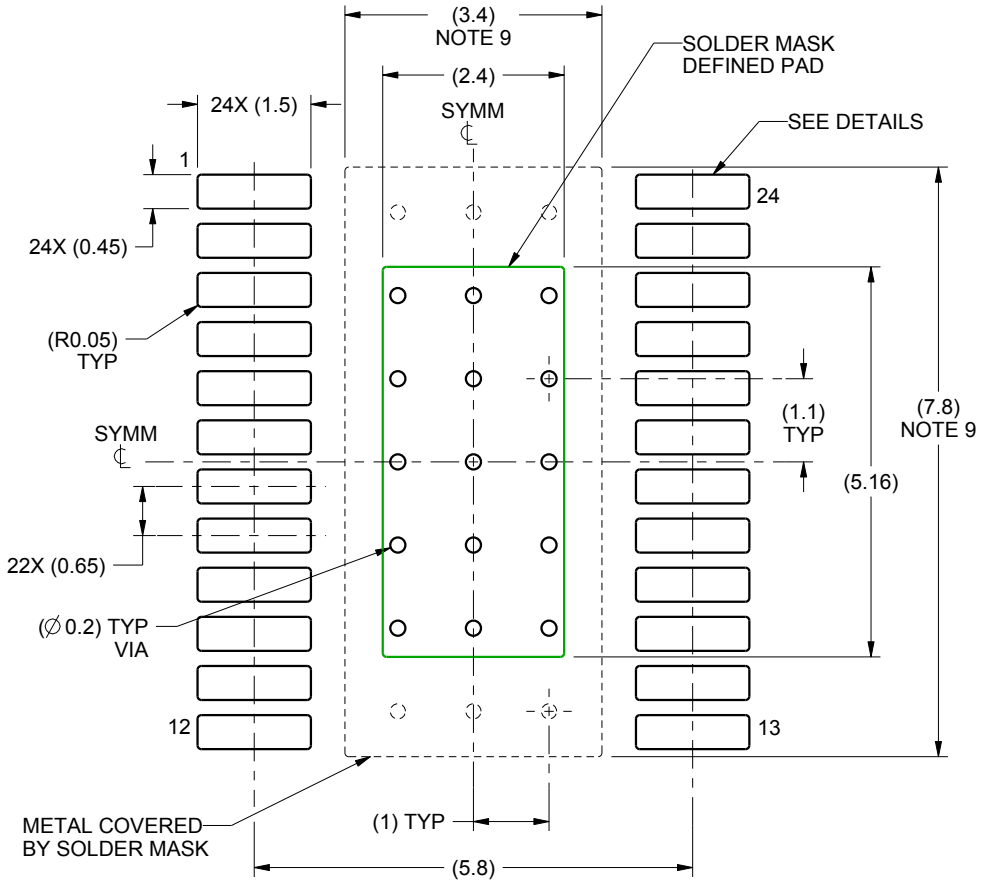
PLASTIC SMALL OUTLINE



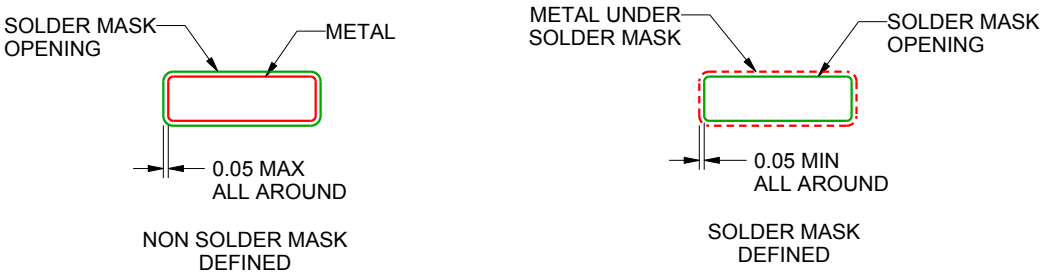
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

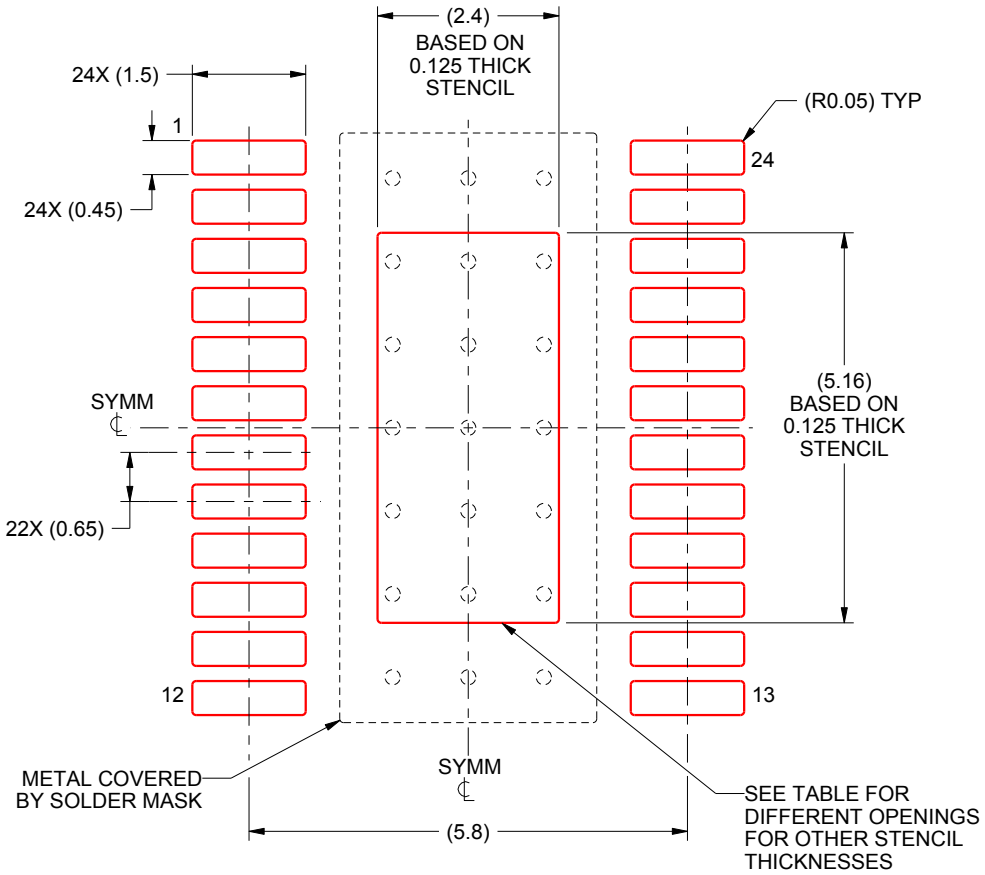


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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