AN1775
APPLICATION NOTE

STR71x Hardware Development Getting Started

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use the STR71x product family and describes the minimum hardware resources required to develop an STR71x application.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

Contents

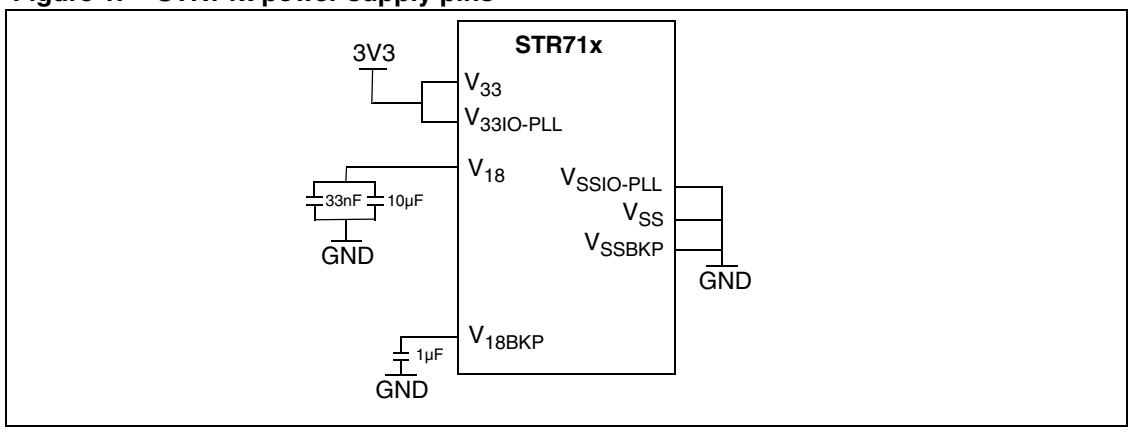
1 Power management

1.1 Overview

The chip is powered by an external 3V3 supply(V_{33}: 2.7 to 3.6 V, AV_{DD}: 3.0 to 3.6 V).

All I/Os are 3V3-capable. An internal Voltage Regulator generates the supply voltage for core logic (~=1.8V). The two V_{18} pins must be connected to external stabilization capacitors. The following figure indicates the recommended configuration for the power supply pins:

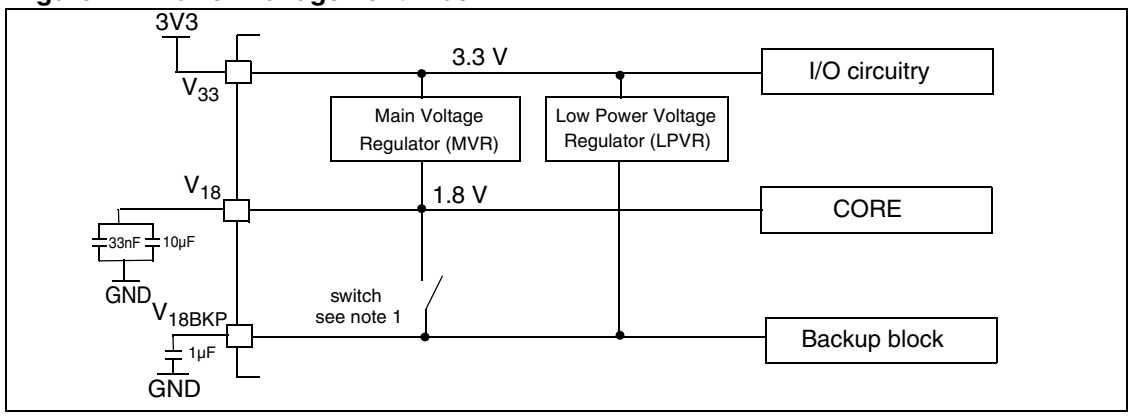
Figure 1. STR71x power supply pins



1.2 Power management block

The following figure describes the power management block implemented on the STR71x devices.

Figure 2. Power Management Block



The STR71x power management block has two regulators:

- The Main Voltage Regulator MVR.
- The Low Power Voltage Regulator LPVR.

Note the following remarks about the two regulators:

- Both regulators can be switched-off by software

- V18 can be used to supply an externally regulated 1.8V, **but** V33 must supply the IOs
- V18BKP pin can be used to externally supply the backup logic, **but** V33 must supply the IOs
- The switch in *Figure 2*, opened only during STANDBY mode, disconnects the V_{18} domain from the V_{18BKP} domain

It is possible to switch-off the MVR and keep LPVR on when the device is in low-power mode (SLOW, WFI, LPWFI, STOP or STANDBY). The LPVR has a different design from the main VR and generates a non-stabilized and non-thermally-compensated voltage of approximately 1.6V.

In STANDBY mode the Low Power VR can be switched off when an external regulator provides a 1.8V supply to the chip through the V_{18BKP} pin for use by RTC and Wake-Up block.

In this case we must to keep the 3.3V on pin V33 even if the two regulators are switch off to keep stable state on the I/Os.

Remark:The PLL is automatically disabled (PLL off) when the MVR is switched off and the maximum allowed operating frequency is 1 MHz. This is due to the limitation imposed by the LPVR which is not able to generate sufficient current to operate in run mode.

The MAIN DEVICE CORE is powered from an external 3V3 power supply pin (V_{33}) through the main regulator.

For more details on the power regulators, refer to the STR71x Reference Manual.

2 Clock management

The STR71x offers a flexible way for selecting core and peripherals clocks, the devices have up to 3 external clock sources:

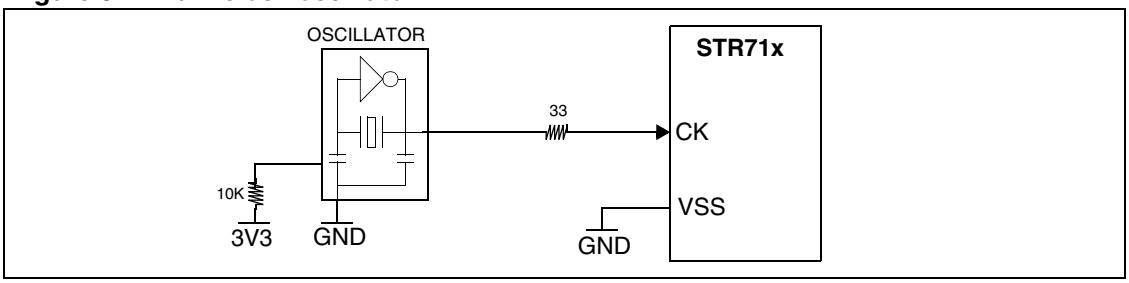
- The PRCCU generates the internal clocks for the CPU and for the on-chip peripherals. The PRCCU may be driven by an external pulse generator, connected to the CK pin.
- The Real time Clock 32kHz oscillator is connected to the internal CK_AF signal (if present on the application), and this clock source may be selected when low power operation is required.
- USB clock source available only with devices with USB feature.

2.1 Clock control unit

The STR71x clock control unit must be driven by an external oscillator, connected to the CK pin, at a frequency of up to 16 MHz. It generates the clocks for the CPU and for the on-chip peripherals. A range of available multiplication and division factors allows for a large number of operating clock frequencies to be driven from the input frequency. However, great care must be taken to respect the recommendations for allowed frequency limits. For more details on allowed operating frequencies for each clock, refer to the Reference Manual.

The following diagram shows the basic implementation of the main external clock.

Figure 3. Main clock oscillator



The following table gives frequency range examples of the Main clock for some input clock values:

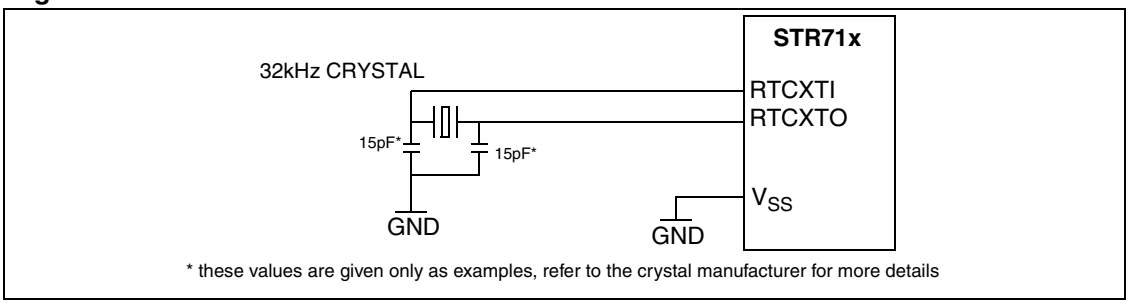
Input Clock	MCLK (Main Clock) Range
4 MHz	[15625 Hz, 50 MHz]
8 MHz	[31250 Hz, 50 MHz]
16 MHz	[62500 Hz, 50MHz]

2.2 Real Time Clock

The Real Time Clock operates at a speed of 32 kHz. This clock must be provided by an external resonator circuitry.

The RTC is used to generate a time base, and can be selected when low power operation is needed. Refer to the Reference Manual for more details.

Figure 4. RTC oscillator



2.3 USB clock

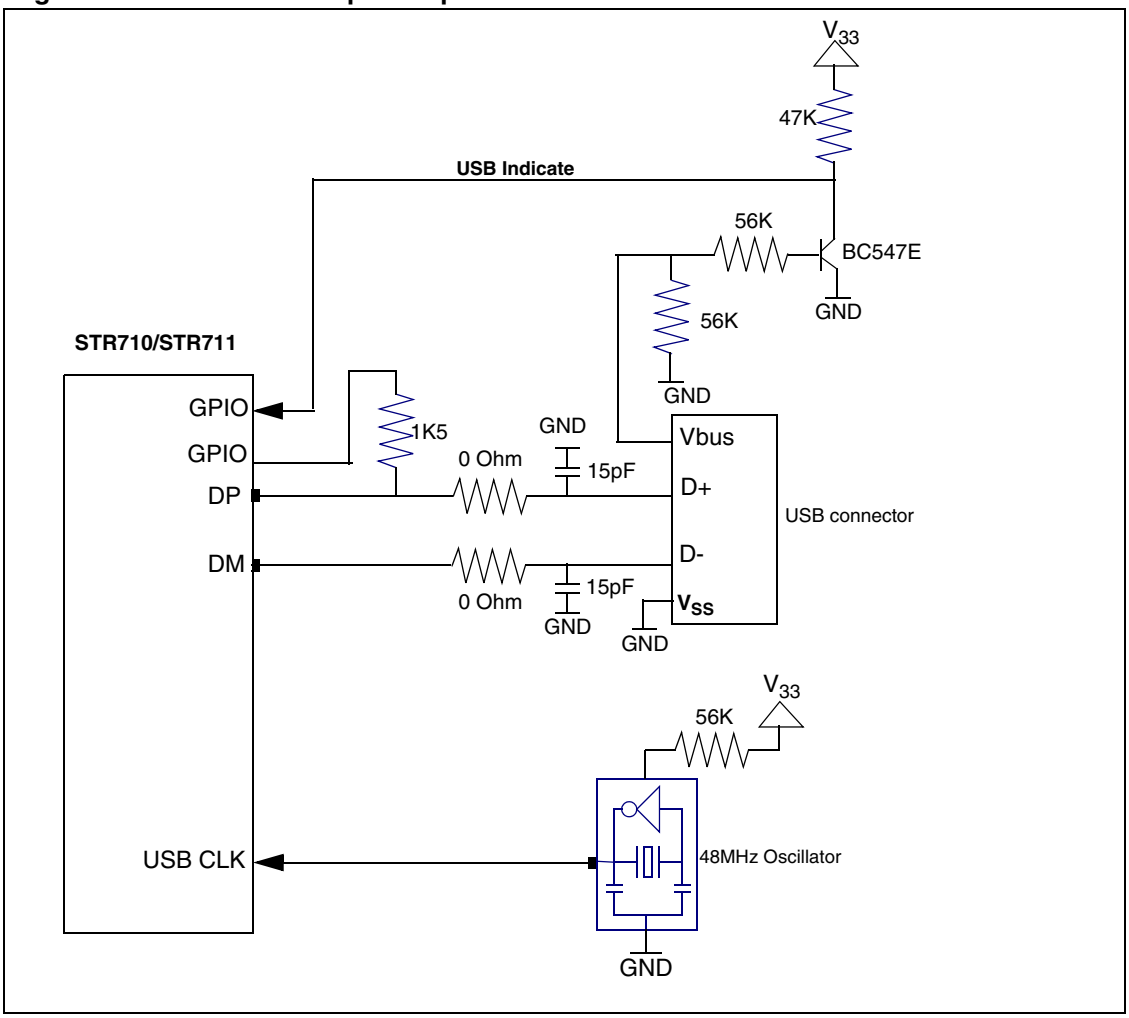
STR710 and STR711 series microcontrollers contain a USB 2.0 Full Speed device module interface that operates at a precise frequency of 48 MHz. This clock is usually provided by an external oscillator connected to the USB clock pin USBCLK. However, to save the board's space and cost, the 48MHz USB clock can also be generated by the internal PLL2 using one single external oscillator for both system and USB module.

This part of the application note describes the hardware and software reference implementation. USB Full Speed signal quality and jitter results can be measured using a single external oscillator to generate not only the System PLL clock and Peripheral's clocks, but also the 48MHz USB clock.

2.3.1 Hardware implementation

The hardware implementation guidelines are described in the figure below.

Figure 5. USB clock and pins implementation



USB full speed interface device supported via type B connector. The USB clock uses a separate 48 MHz oscillator.

Transistor circuit used to indicate the cable status (Cable connected USB/IND pin = 0 logic, Cable deconnected = USB/IND pin = 1 logic).

3 Reset management

Both the Main Voltage Regulator and the Low Power Voltage Regulator contain an LVD.

They keep the device under reset when the corresponding controlled voltage value (V_{18} or V_{18BKP} falls below 1.35V±10%).

The LVDs do not monitor V33 which supplies the I/O and analog parts of the device.

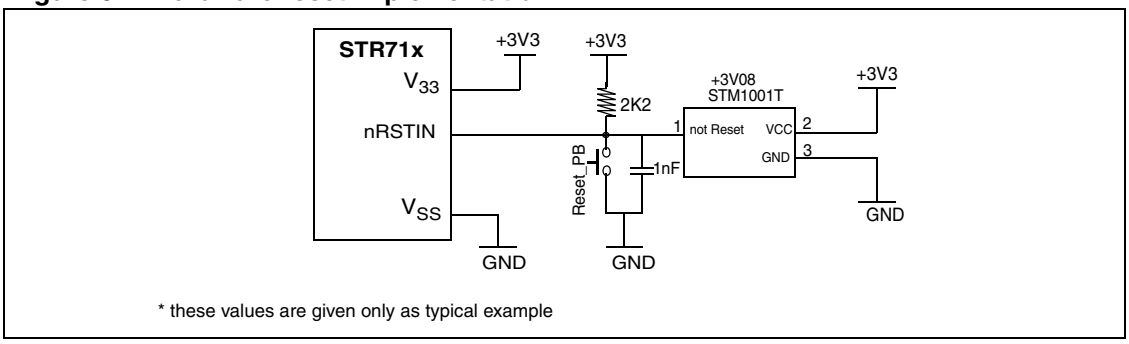
Note: During power-on, a reset must be provided externally.

At power on, the nRSTIN pin must be held low by an external reset circuit until V_{33}.

Figure 6 gives an example of the hardware implementation of the RESET circuit for STR71x devices.

- The STM1001 low-power CMOS microprocessor supervisory circuit is used to assert a reset signal whenever the V_{33} voltage falls below a preset threshold or a manual reset is asserted.

Figure 6. Hardware reset implementation



4 Boot management

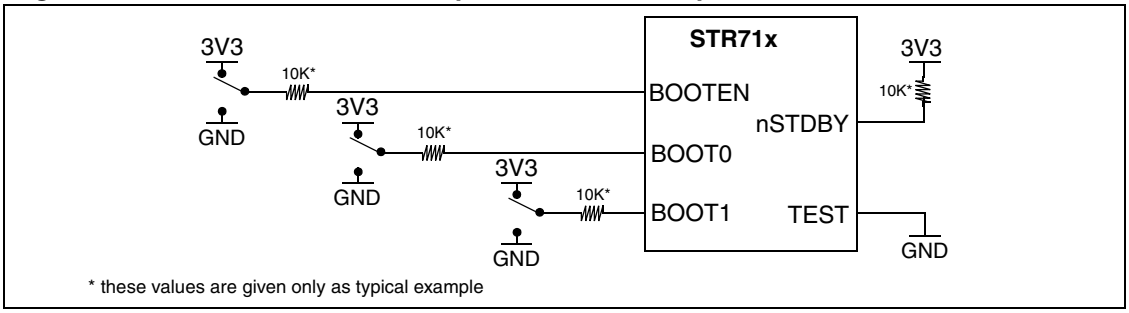
Three different boot modes are available and can be enabled by means of three input pins: BOOTEN, BOOT0 and BOOT1.

The following table describes the different boot mode configurations.

BOOTEN	BOOT0	BOOT1	BOOT Mode
0	x	x	USER: boot from internal FLASH memory
1	0	0	
1	1	0	Reserved
1	0	1	RAM: boot from internal RAM memory
1	1	1	EXTMEM: boot from external memory mapped on the EMI interface at 0000 0000h address.

The following figure gives an implementation example of boot management for STR71x devices. BOOT0 and BOOT1 are alternate function pins used for boot configuration during the RESET phase (floating-input configuration), so they can be used afterwards in the application as standard I/Os. For more details concerning boot configuration, refer to the device reference manual.

Figure 7. Boot mode selection implementation example



Note: 1 As the nSTDBY pin has a floating input configuration, an external pull-up has to be provided to avoid remaining in stand-by mode.

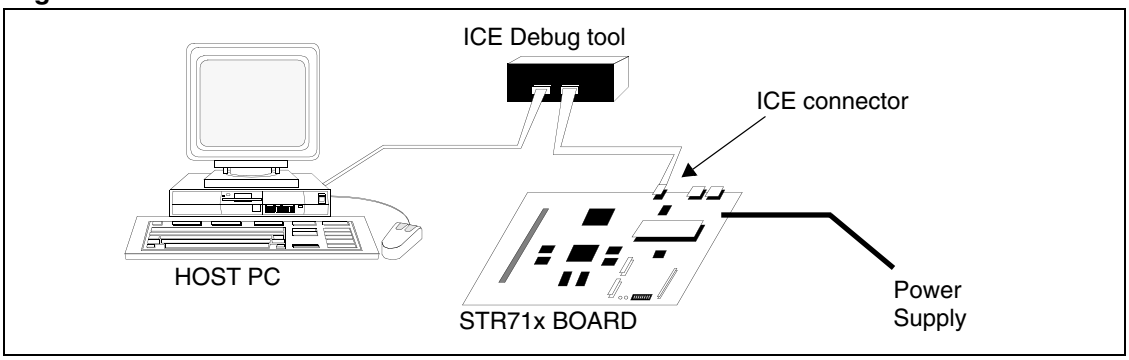
2 The TEST pin of the STR71x must always be forced to ground (ST reserved test pin)

5 Debug management

The Host/Target interface is the hardware equipment that connects the Host to the application board. This interface is made of three components: a hardware debug tool, such as Micro-ICE from ARM, a JTAG connector and a cable connecting the host to the debug tool.

Figure 8 shows the connection of the host to the STR71x board.

Figure 8. Host to board connection



5.1 ICE debug tool

ICE Debug tool is a host interface that connects a PC to an STR71x development board featuring a debug interface as shown in *Figure 8*. The Embedded ICE is an intelligent host interface that provides fast access to host services, access to on-chip emulation and debug facilities. When you are using the ST7R71x board as stand-alone system, the ICE Debug tool can be used to download programs.

The STR71x development kit supports the ARM RealView ICE Micro Edition. The Micro-ICE is plugged in to the host via a USB cable.

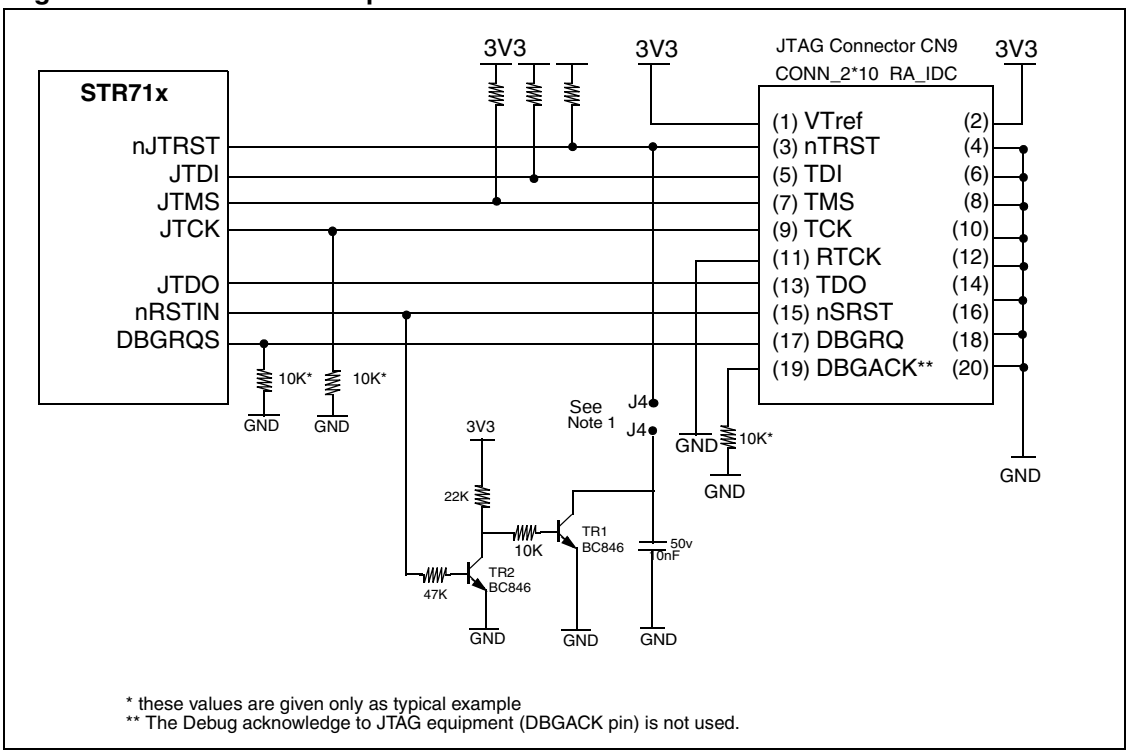
5.2 JTAG / ICE connector

The ICE connector enables JTAG hardware debugging equipment, such as RealView-ICE, to be connected to the ST7R71x board. It is possible to both drive and sense the system-reset line, and to drive JTAG reset to the core from the ICE connector. The *Figure 9* shows the ARM ICE connector pin-out.

The STR71x has a user debug interface. This interface contains a five-pin serial interface conforming to JTAG, IEEE standard 1149.1-1993, “Standard Test Access Port-Scan Boundary Architecture”. JTAG allows the ICE device to be plugged to the board and used to debug the software running on the STR71x.

JTAG emulation allows the core to be started and stopped under control of the connected debugger software. The user can then display and modify registers and memory contents, and set break and watch points.

Figure 9. Ice connector implementation



Note: 1 In order for JTAG and Chip Reset to be synchronized the J4 jumper must be fitted.

2 STR71x has a Debug Request (DBGRQS) pin, on 144-pin packages only. This active high signal can be used to force the core to enter Debug Mode, giving the Emulation system access to internal resources (code, registers, memory, etc). This pin must be kept LOW when emulation is not being used.

The following table describes the JTAG connector pins:

Std Name	STR71x	Description	Function
nTRST	JTRST	Test Reset (from JTAG equipment)	This active LOW open-collector is used to reset the JTAG port and the associated debug circuitry. It is asserted at power-up by each module, and can be driven by the JTAG equipment.
TDI	JTDI	Test data in (from JTAG equipment)	TDI goes down the stack of modules to the motherboard and then back up the stack, labelled TDO, connecting to each component in the scan chain.
TMS	JTMS	Test mode select (from JTAG equipment)	TMS controls transitions in the tap controller state machine. TMS connects to all JTAG components in the scan chain as the signal flows down the module stack.
TCK	JTCK	Test clock (from JTAG equipment)	TCK synchronizes all JTAG transactions. TCK connects to all JTAG components in the scan chain. Series termination resistors are used to reduce reflections and maintain good signal integrity. TCK flows down the stack of modules and connects to each JTAG component. However, if there is a device in the scan chain that synchronizes TCK to some other clock, then all down-stream devices are connected to the RTCK signal on that component.

Std Name	STR71x	Description	Function
RTCK	GND (not used)	Return TCK (to JTAG equipment)	Some devices sample TCK (for example a synthesizable core with only one clock), and this has the effect of delaying the time that a component actually captures data. Using a mechanism called adaptive clocking, the RTCK signal is returned by the core to the JTAG equipment, and the clock is not advanced until the core had captured the data. In adaptive clocking mode, the debugging equipment waits for an edge on RTCK before changing TCK.
TDO	JTDO	Test data out (to JTAG equipment)	TDO is the return path of the data input signal TDI.
nSRST	nRSTIN	System reset (bidirectional)	nSRST is an active LOW open-collector signal that can be driven by the JTAG equipment to reset the target board. Some JTAG equipment senses this line to determine when a board has been reset by the user. When the signal is driven LOW by the reset controller on the core module, the motherboard resets the whole system by driving nSYSRST low.
DBGRQ	DBGRQS (not used w/ 64pin)	Debug request (from JTAG equipment)	DBGRQ is a request for the processor core to enter debug state.
DBGACK	GND (not used)	Debug acknowledge (to JTAG equipment)	DBGACK indicates to the debugger that the processor core has entered debug mode.

For more details on the JTAG port refer to the IEEE standard 1149.1-1993, “Standard Test Access Port-Scan Boundary Architecture” specification.

6 Reference Design

6.1 Main

This reference design is based on the STR710FZ2T6, a highly integrated microcontroller, running at 48 MHz that combines the popular ARM7TDMI™ 32-bit RISC CPU with 256 Kbytes of embedded flash, 64 Kbytes of high speed SRAM, and numerous on-chip peripherals.

6.1.1 Clock

- +3.3 V surface mounted 16 MHz oscillator provides the main clock source: S113, please refer to *Section 2.1 on page 6* for more details.
- RTC real-time clock for wakeup from standby mode with 32 KHz crystal: Y101, please refer to *Section 2.2 on page 6* for more details.

6.1.2 Reset

One push button S112 is used to generate a hardware reset, please refer to *Section 3 on page 9* for more details.

6.1.3 Boot mode

Three switches S108, S109 and S110 are used to select the boot Mode, please refer to *Section 4 on page 10* for more details.

6.1.4 Wake-Up

S111 push button is used to exit from STANDBY mode (power supply voltage removed except Real time Clock).

For more details, please refer to the *STR71x reference manual*.

6.2 Power supplies

Power to the board is supplied using a power supply providing 5 V DC to the board. All other required voltages are provided by the on-board voltage regulator 3V3 LD1085V33 and Zener Diode LM4040 for ADC input voltage.

For more details, refer to *LD1085V33, LM4040 datasheets* and *Section 1 on page 4*.

6.3 USB full speed interface

USB full speed interface device supported via type B connector. The USB clock uses a separate 48 MHz oscillator.

A transistor circuit is used to indicate the cable status (Cable connected USB/IND pin = 0 logic, Cable deconnected = USB/IND pin = 1 logic).

6.4 CAN interface

A general purpose, asynchronous serial I/O data port connected through a 9-pin D-type male connector with micro switches selectable between High or Low bus output S702, and between Standby or Slope control S700.

For more details, refer to *CAN transceiver SN65HVD230D datasheet*.

6.5 RS232 serial interface

A general purpose, asynchronous serial I/O data ports is connected through 9-pin D-type male connectors.

RS232 connects directly to UART0, transmit and receive only (null modem).

RTS is shorted to CTS and DTR is shorted to DSR at the connector.

For more details, refer to *RS232 transceiver ST3232 datasheet*.

6.6 Serial ROM

6.6.1 SPI Flash

1-Mbit SPI serial flash connected to the buffered serial peripheral interface (BSPI). Switch S603 is used to enable or disable write protect (pull down = Write protect, pull up = Write enabled).

For more details, refer to *SPI Flash M25P10-A datasheet*.

6.6.2 I2C EEPROM:

8-kbit EEPROM connected to the I2C0 interface, Switch S600 is used to enable or disable write protect (pull down = Write protect, pull up = Write enabled).

For more details, refer to *I2C Eeprom M24C08 datasheet*.

The values R614 and R616 are dependent on the I2C communication speed.

For more details on theses values, please refer to the *STR71x reference manual*.

6.7 JTAG interface

Refer to the section *Section 5 on page 11*.

6.8 SRAM

Two SRAM 2M byte are connected to External Interface Memoy EMI and mapped from 0x6200 0000 to 0x623F FFFF.

For more details, refer to the *SRAM memory TC55V8200FT-12 datasheet*.

6.9 Flash

One Flash 2M word is connect to External Interface Memoy EMI and mapped from 0x6000 0000 to 0x603F FFFF (boot bank).

For more details, refer toFlash memory M28W320ECB datasheet.

6.10 LCD interface

LCd 2 * 16 is connected to external interface memory EMI.

Address 2 A2 is used as the LCD register address signal.

Region space available from 0x6400 0000 to 0x65FF FFFF

6.11 Conclusions and recommendations

- System clock jitter values decrease when the system clock is delivered by STR71x internal PLL1 (comparing to the jitter values on the external oscillator inputs), because the noise injected in the CLK pin input was filtered by the internal PLL.
- It is possible to use one single external 4MHz oscillator to generate both core, peripheral's clocks and 48MHz USB clock to minimize and save board cost and space.
- With this single external oscillator generating both the system clock using PLL1 and the 48Mhz USB clock using PLL2, the STR710/STR711 has all the characteristics to pass the requirements for USB revision 2.0 full speed device test and get the USB certification.

Particular care must be taken to decrease external oscillator noise while routing its clock on board.

7 Schematics

Figure 10. Reference design top level schematics

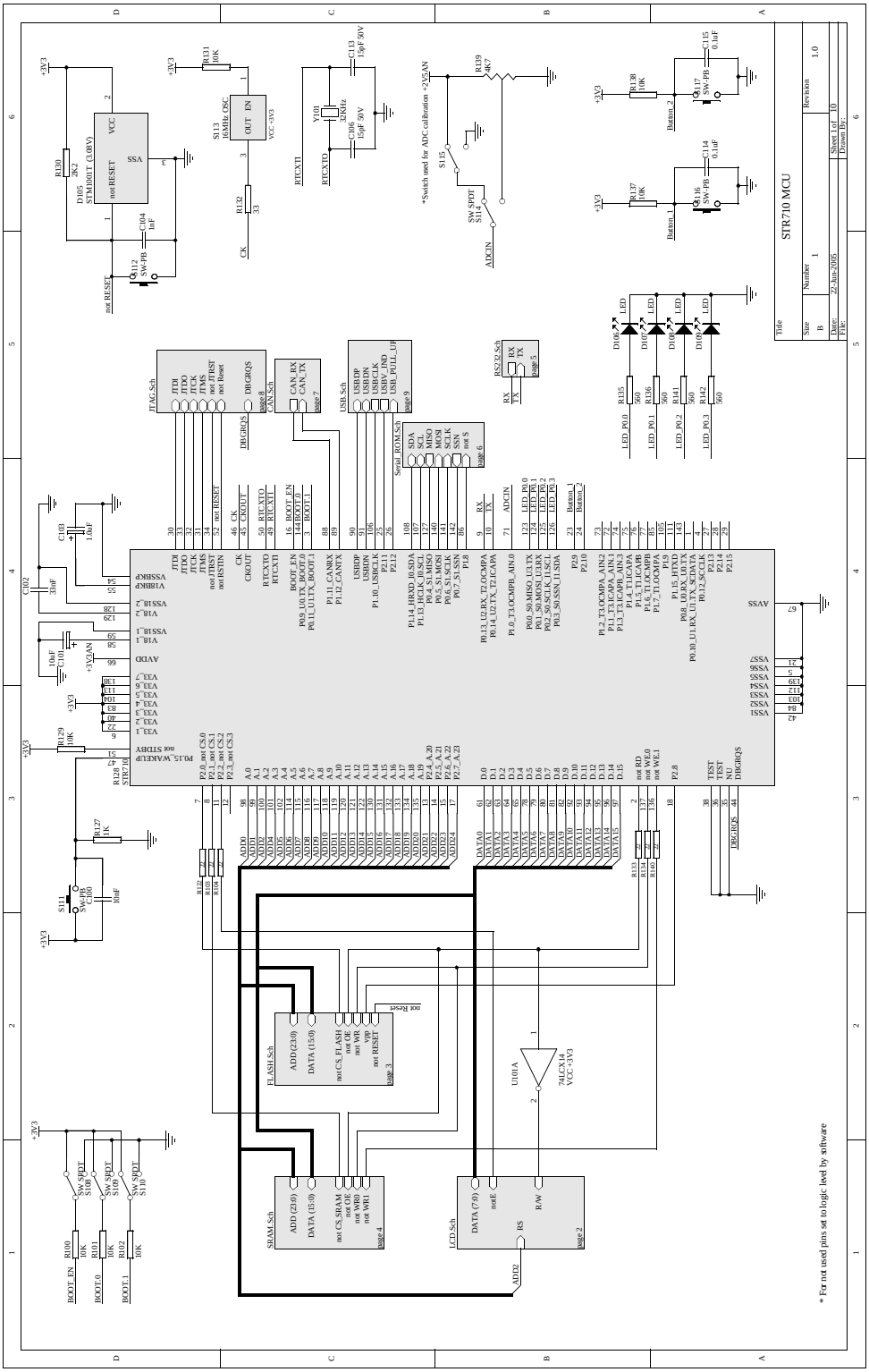


Figure 11. LCD interface

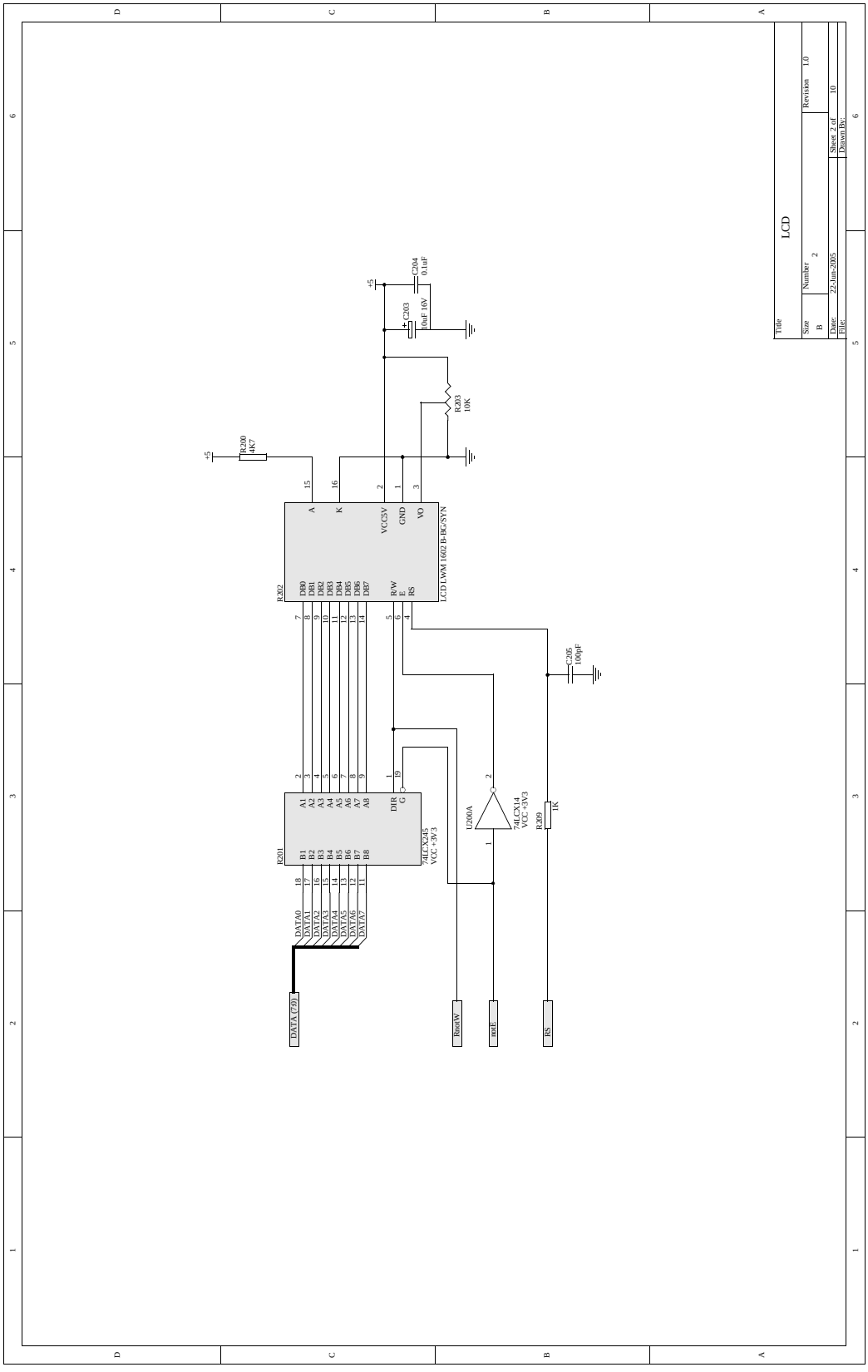


Figure 12. EMI Flash

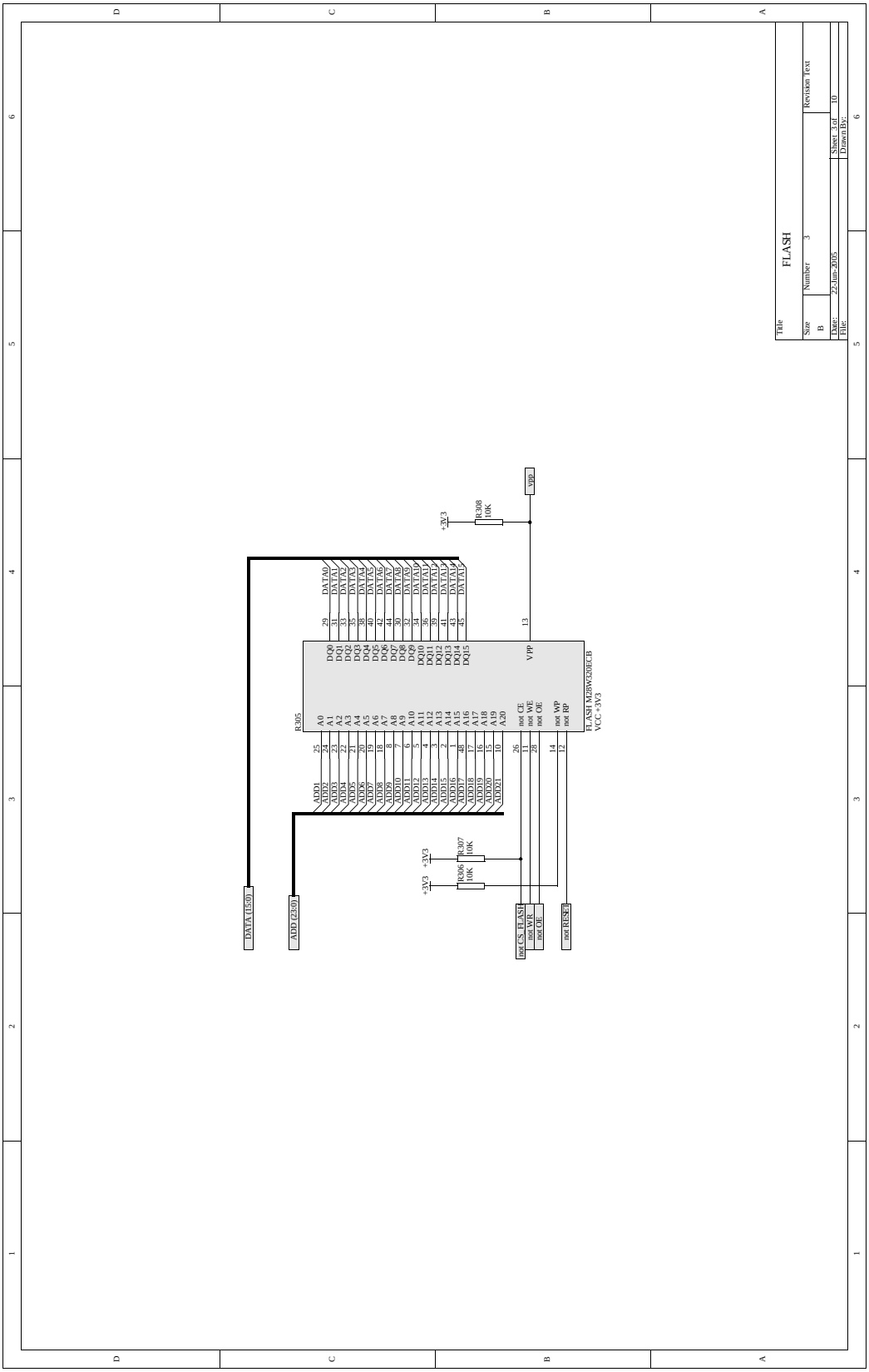


Figure 13. EMI SRAM

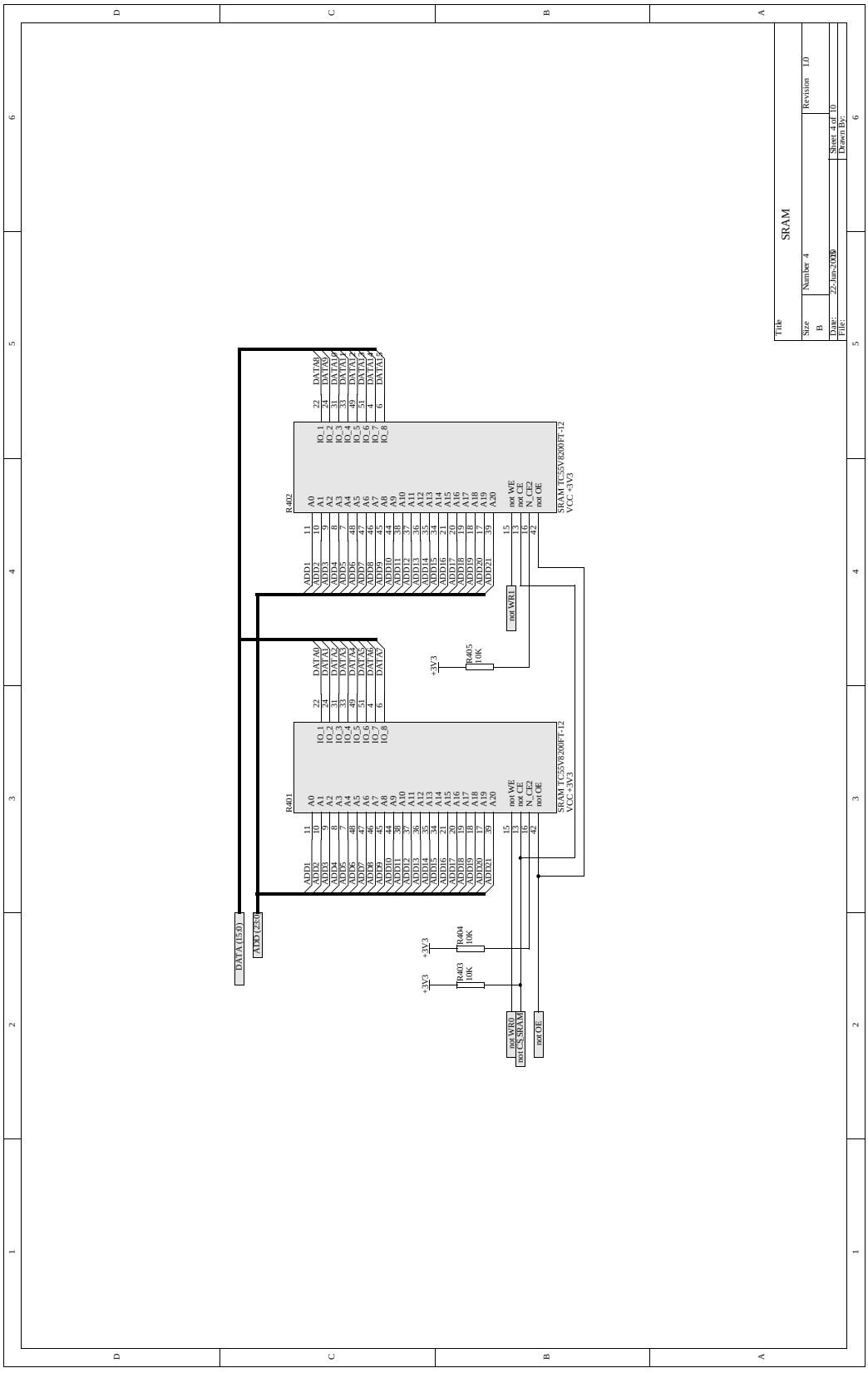


Figure 14. RS232 interface

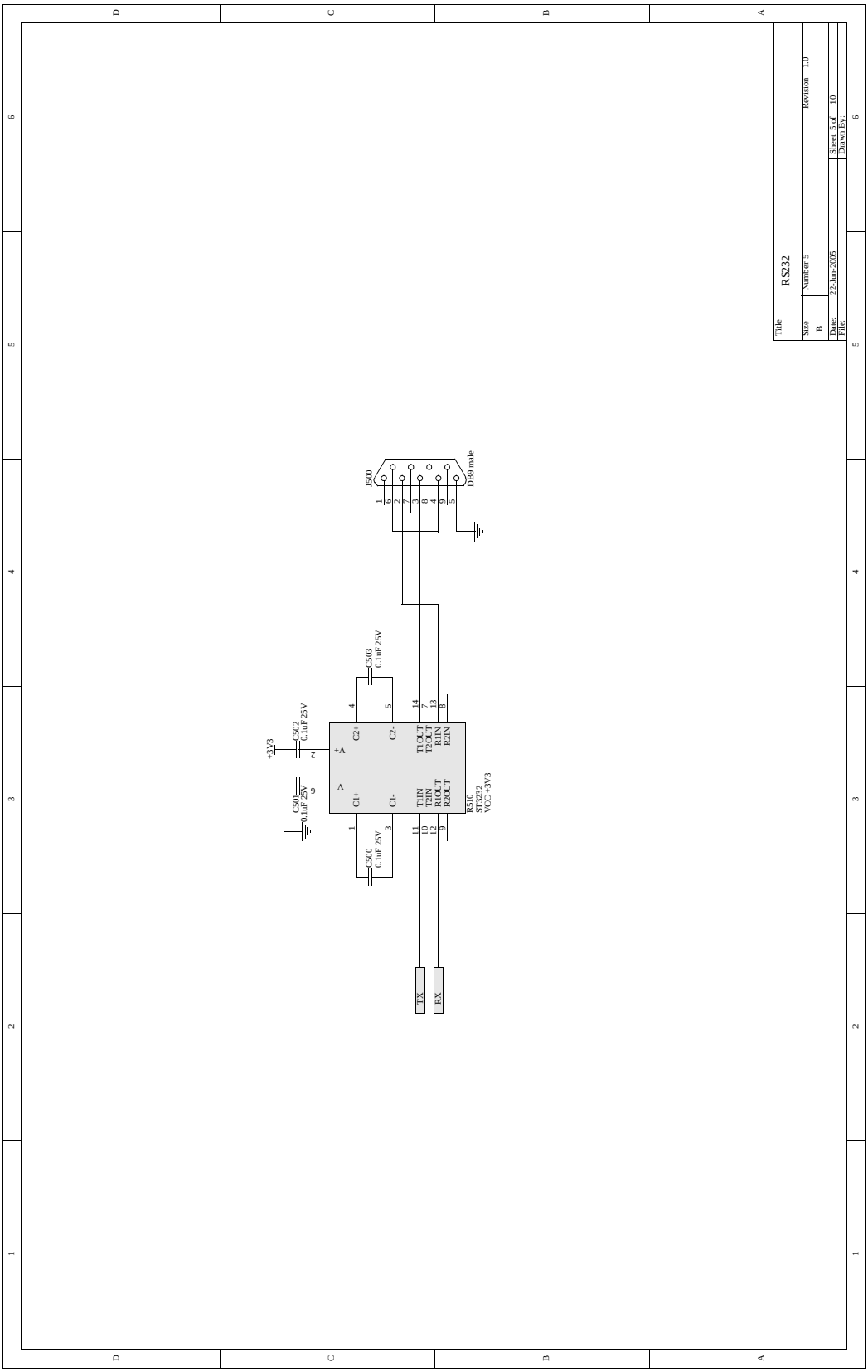


Figure 15. Serial ROM interface

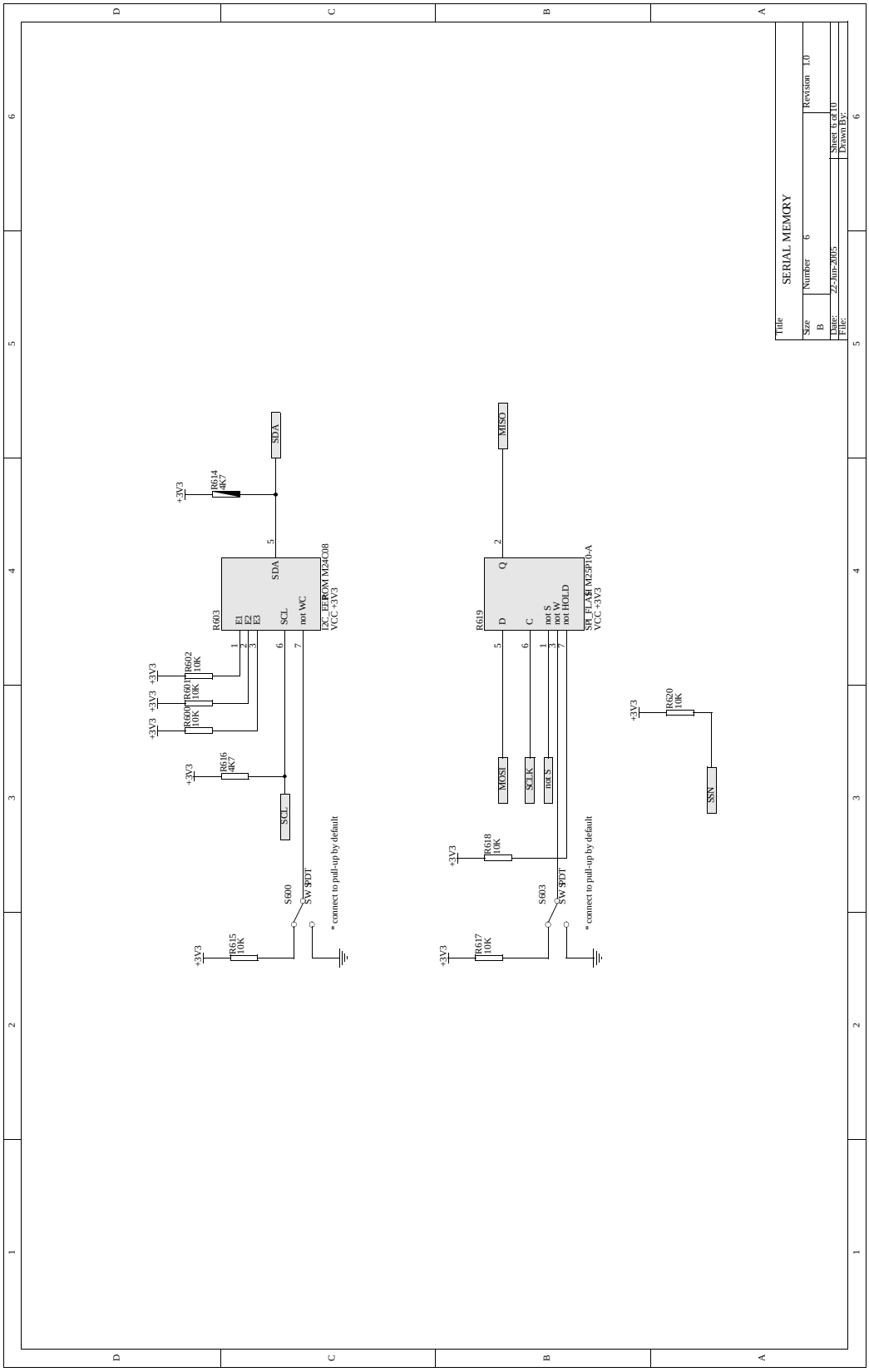


Figure 16. CAN interface

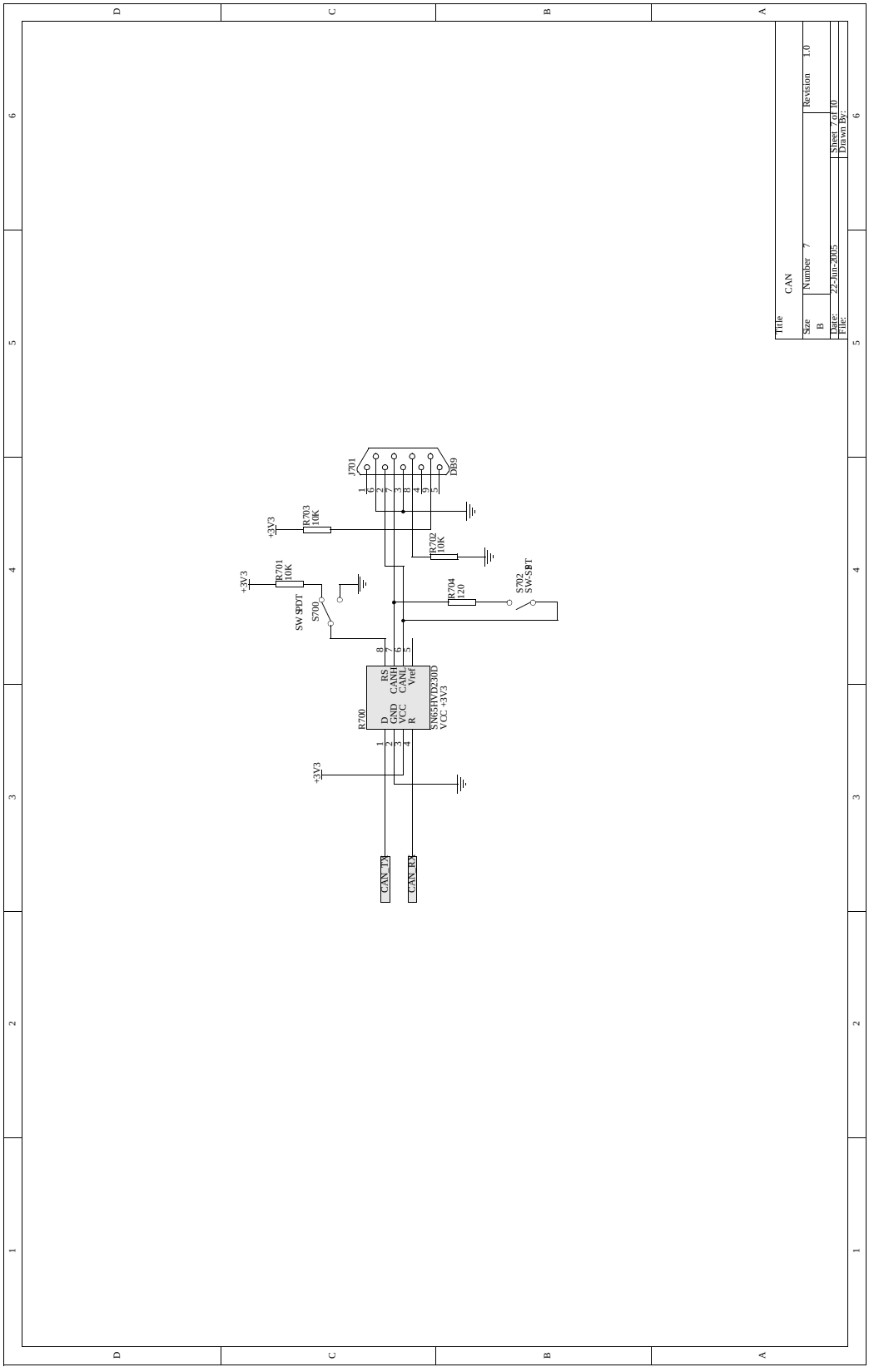


Figure 17. JTAG interface

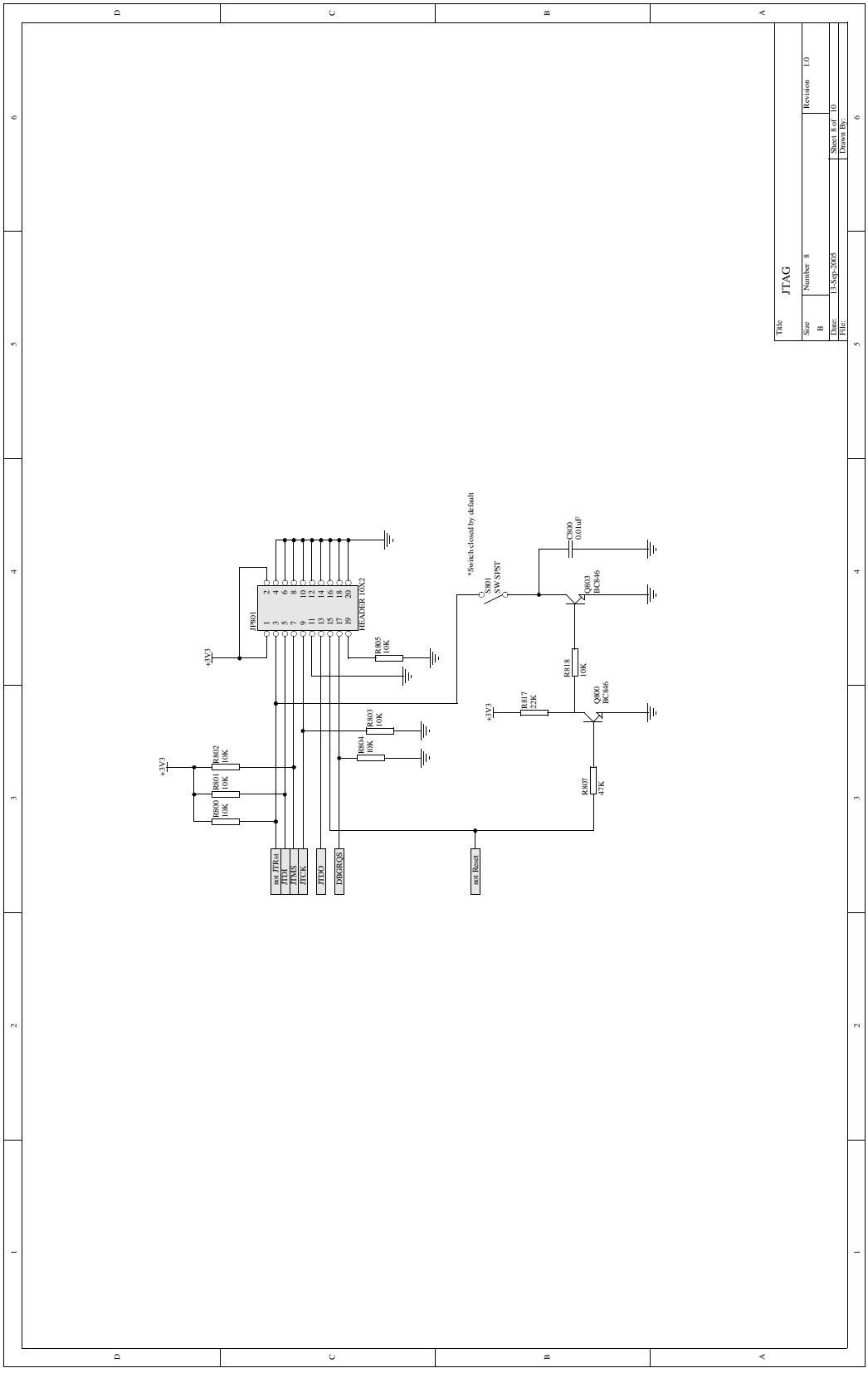


Figure 18. USB interface

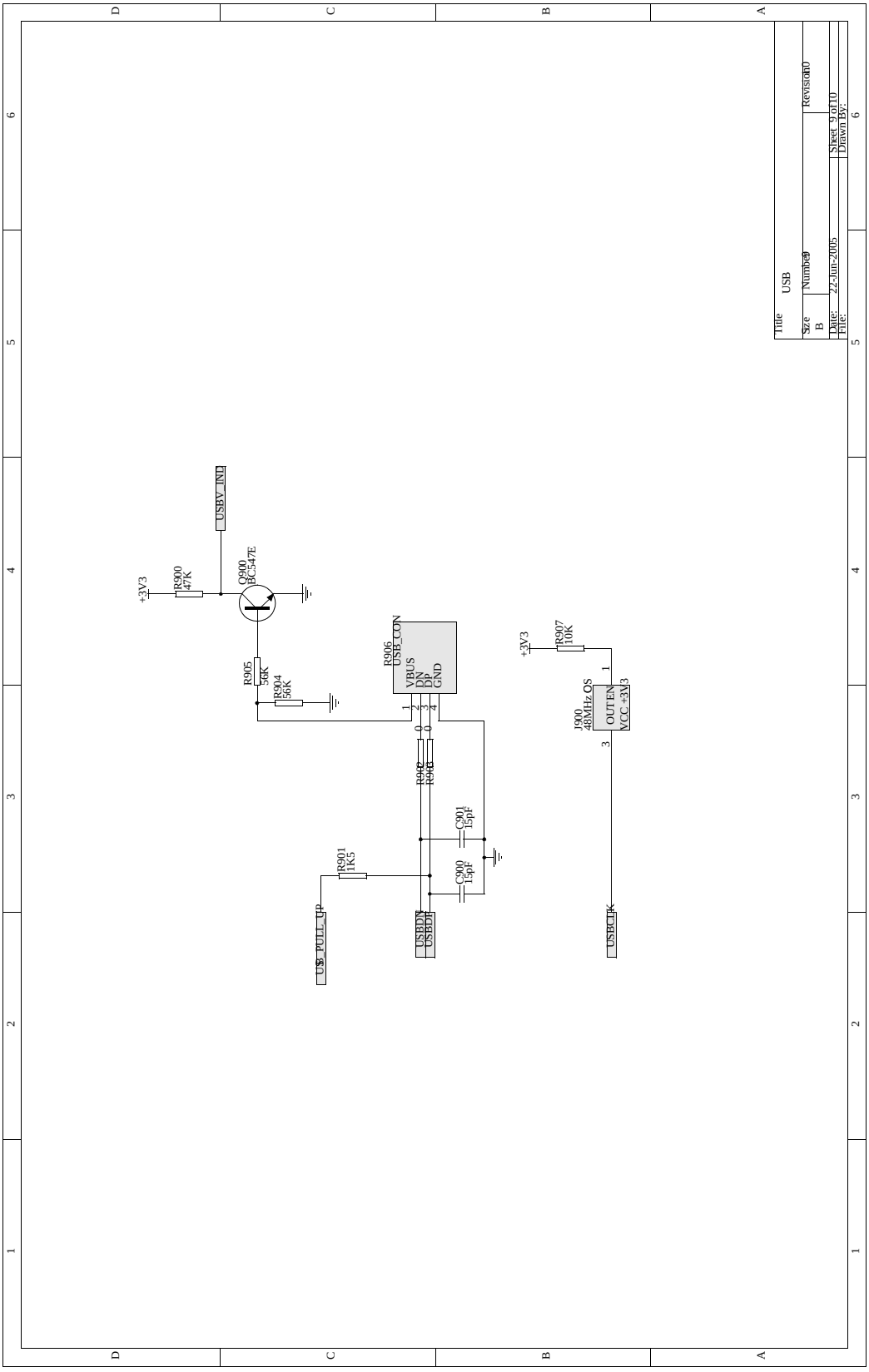
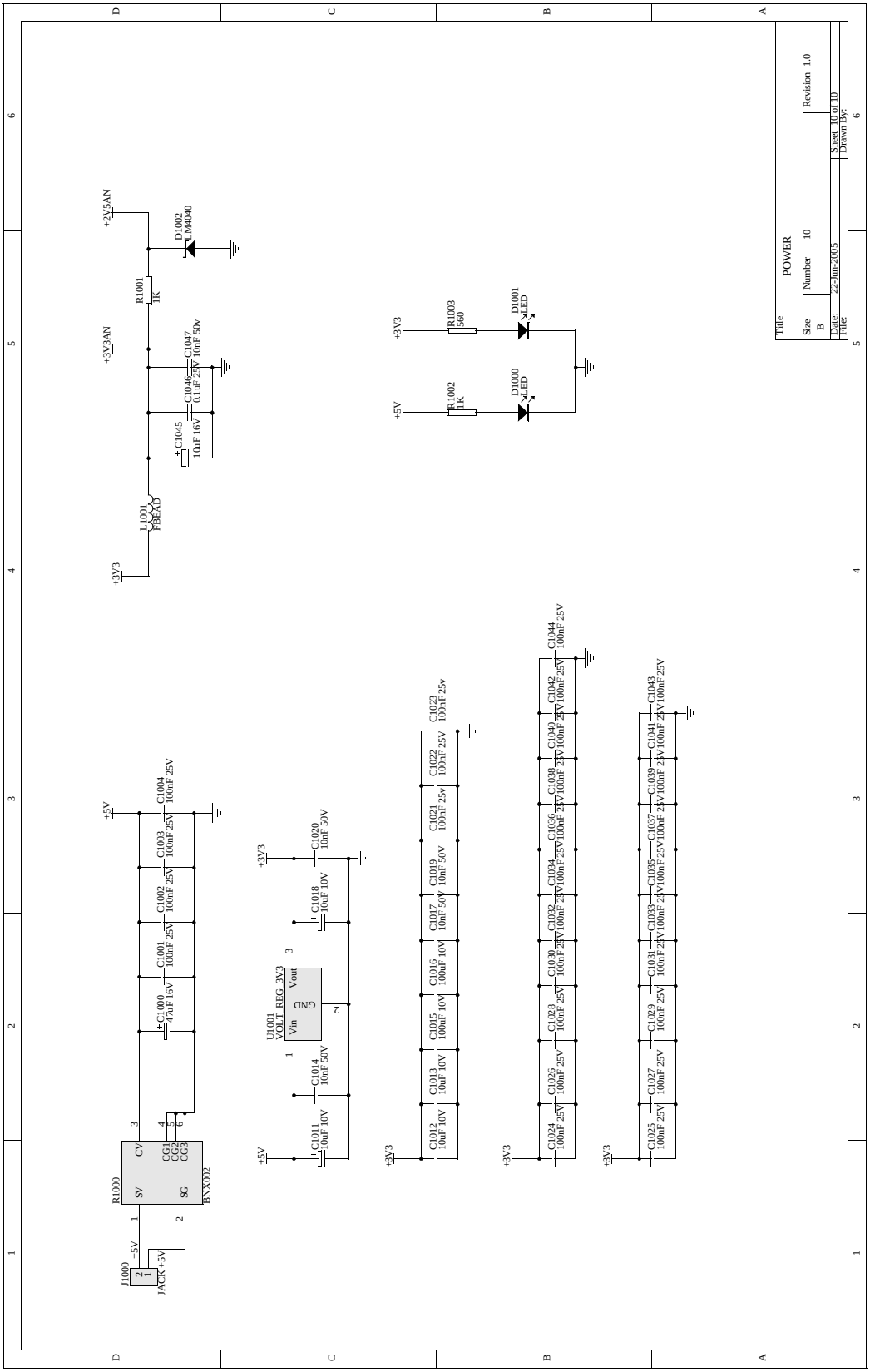


Figure 19. Power schematics



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