LTC2063/LTC2066
2µA/10µA Supply Current, Low I_B, Zero-Drift Operational Amplifiers

DESCRIPTION

Demonstration circuit 2837A is a customizable board showcasing the micropower zero-drift op amp LTC®2063 (-A option) or LTC2066 (-B option) with shutdown in an SC70 6-pin package. The board is laid out for most common op amp applications and left mostly unstuffed to maximize flexibility for a wide range of applications.

The DC2837A includes the SC70 package op amp, jumpers, unity gain configuration resistors, input lowpass filters, reverse supply protection, and supply bypass capacitors on a small printed circuit board with turrets and SMA connectors for input, output, power and shutdown. The board may be used in split rail or single supply as desired.

The user only needs to furnish external ±2.5V split supplies and an input signal to operate the board. An external shutdown signal can be applied as well to demonstrate the very minimal transient current when starting up the part from shutdown.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LTC2063, V_S = 5V						
V_{OS}	Input Offset Voltage	V_S = 5.25V		1	±5	µV
$\Delta V_{OS}/\Delta_T$	Input Offset Voltage Drift	–40°C to 85°C			±0.02	µV/°C
I_B	Input Bias Current			–3	±20	pA
GBW	Gain Bandwidth Product	R_L = 499kΩ		20		kHz
f_C	Internal Chopping Frequency			5		kHz
I_S	Supply Current	No Load In Shutdown ($\overline{SHDN}$ = V^-)		1.4 90	2 170	µA nA
LTC2066, V_S = 5V						
V_{OS}	Input Offset Voltage	V_S = 5.25V		1	±5	µV
$\Delta V_{OS}/\Delta_T$	Input Offset Voltage Drift	–40°C to 85°C			±0.02	µV/°C
I_B	Input Bias Current			±5	±35	pA
GBW	Gain Bandwidth Product	R_L = 499kΩ		100		kHz
f_C	Internal Chopping Frequency			25		kHz
IS	Supply Current	No load In Shutdown ($\overline{SHDN}$ = V^-)		7.5 90	10 170	µA nA

QUICK START PROCEDURE

Demonstration circuit 2837A is easy to set up to evaluate the performance of the LTC2063/LTC2066. The DC2837A board provides multiple empty mostly-0805 component footprints for users to configure the LTC2063/LTC2066 as desired.

The default configuration of the board is in **unity gain/ buffer with split supplies (V^+ and $V^–$)**.

Refer to Figure 1 for a generic schematic, Figure 2 for measurement equipment setup, and Table 1 for a jumper table, and follow the procedure below.

Note: Unless otherwise specified, leave jumpers in default positions, and components unstuffed. Table 1 explains each jumper setting in further detail.

1. Verify that jumper **JP6** for $\overline{SHDN}$ is on position 1, labeled *EN*, so that the part is enabled.
2. Verify that jumper **JP4** is across 2–3 for GND so the board is in split supply mode.
3. Set the power supply's positive output to +2.5V and the negative output to –2.5V.

   Note: The supply limits are **±2.62V** in **split** supply, and **1.7V to 5.25V** in **single**-supply ($V^–$ = GND) configuration.
4. With power off, connect the power supply to the row of turrets at the top of the board: + supply to V^+ turret, –supply to $V^–$ turret, and COM to GND turret.
5. Connect a signal generator either at the +IN and GND turrets or at the +IN SMA input. A 100Hz sine wave with 0V offset and $0.5V_{P-P}$ is a good starting point.

   Note: The input lowpass filter at IN^+ has a cutoff of 480Hz for DC2837A-A (LTC2063) and 2.4kHz for DC2837A-B (LTC2066).
6. Connect an Oscilloscope 10× probe to the OUT turret. Clip scope probe GND to a GND turret. Set the scaling to 100mV/2ms per division.
7. Power-up the system. A 100Hz $0.5V_{P-P}$ sine wave centered at 0V should appear on the oscilloscope.
8. Increase the signal amplitude and observe the signal for clipping as signals reach the supply rails. Slew and settling behavior can be evaluated by switching the signal generator to square wave.
9. To evaluate shutdown performance, move the jumper at **JP6** to position 3, labeled *DIS*, tying $\overline{SHDN}$ to $V^–$. To re-enable the part, move the **JP6** jumper back to *EN* (position 1).
10. **OPTIONAL:** To evaluate shutdown performance with a shutdown control signal, **remove any jumper connectors on JP6 completely**. Connect a signal generator to the $\overline{SHDN}$ turret and GND. Set the signal generator to a $5V_{P-P}$, 0V offset, 1Hz square wave. Keep the input sine wave on. Adjust oscilloscope time scale to 100ms/div at least. Observe the part's output shutting down and returning, and the supply current dropping when shut down and rising again when turned back on.

Table 1. Jumper Table

JUMPER	POSITION 1 OR STUFFED*	POSITION 3 OR UNSTUFFED*	NOTES
JP1	V^+	$V^–$	Add DC Offset, or Connects Filter Component Z1 to –IN
JP2*	Ties –IN to V^+ or $V^–$ via Z1	Disconnects –IN from V^+ or $V^–$ via Z1	Z1 Unstuffed by Default
JP3	V^+	$V^–$	Add DC Offset to +IN; R9, R10 Allow for Scaling/Dividing
JP4	$V^–$ Tied to GND (Single-Supply)	Separate $V^–$ and GND (Split Rail)	3rd Position GND for Jumper Storage when Using Split Rails
JP5	Add Z2 in Parallel with R5 Feedback	Short Out R6 in Series with Output	Default Open Path (Z2 Unstuffed)
JP6	V^+, Enable	$V^–$, Disable	Remove Jumper Completely if Using External $\overline{SHDN}$ Control

* Two-Terminal Jumper ONLY (JP2)

QUICK START PROCEDURE

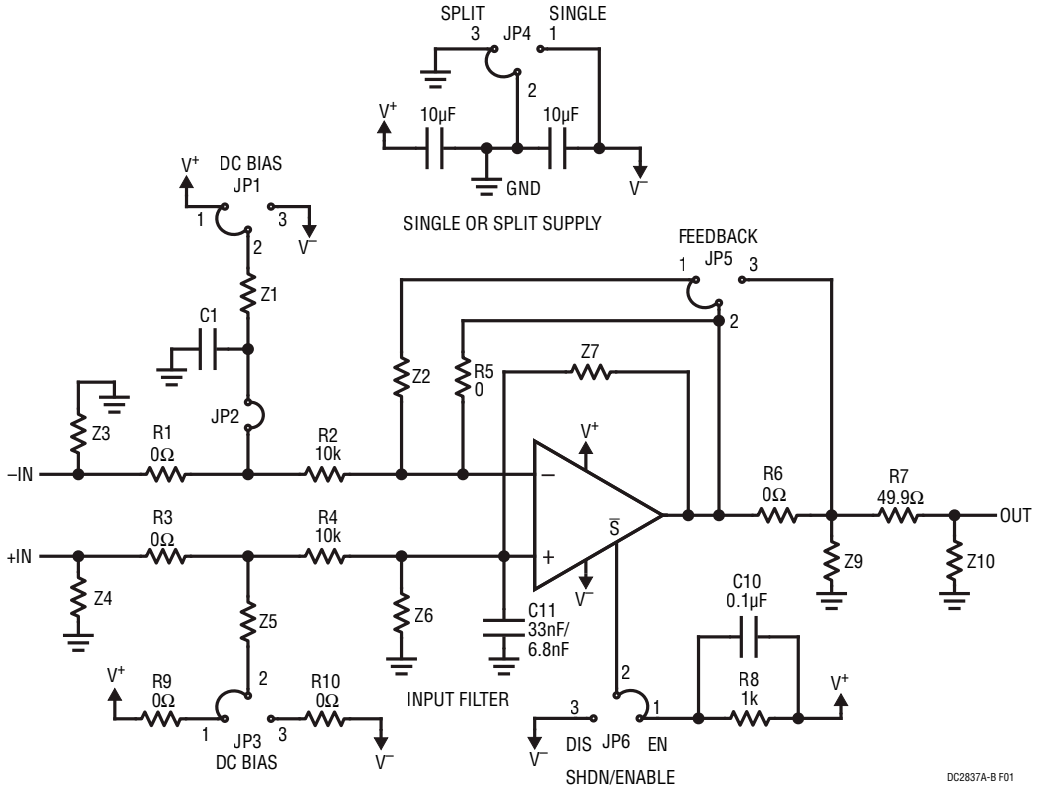

Figure 1. Simplified Generic Schematic

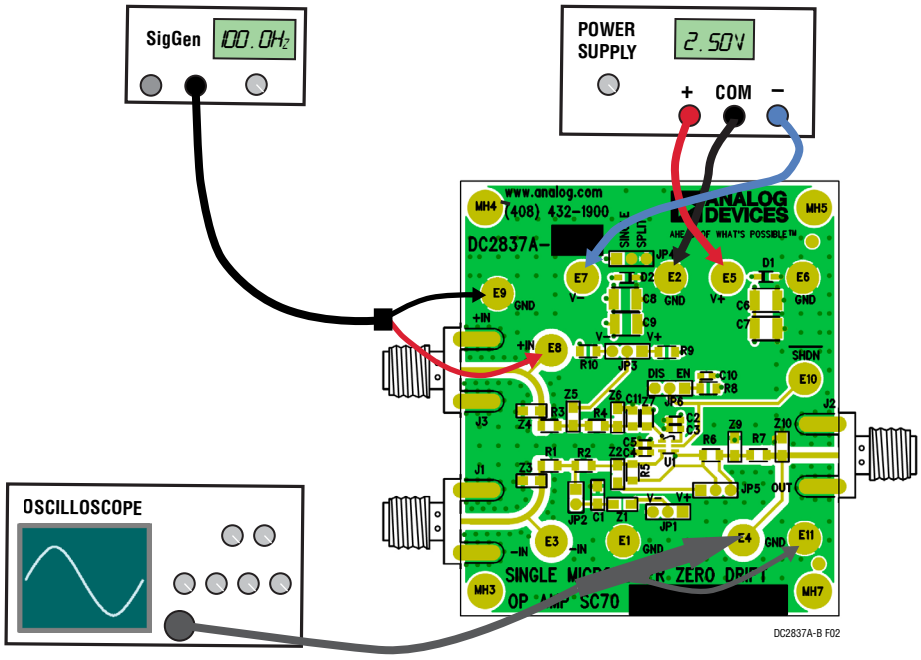

Figure 2. Proper Measurement Equipment Setup

OPERATING PRINCIPLES

The DC2837A board provides multiple empty mostly-0805 component footprints for users to configure the LTC2063/LTC2066 as desired. Common configurations and functions are illustrated below.

In the following schematics, components not mentioned should be left unstuffed, and jumpers not mentioned are not relevant.

SINGLE SUPPLY VS SPLIT RAILS

By default, the board is set up is for split supplies (V^+, $V^–$).

To switch to a single supply, V^+ and GND:

1. Remove any negative supplies from the $V^–$ turret. This is important to prevent shorting the power supply out.
2. Disconnect and change offset voltage of input signal source(s), then reconnect.
3. Move jumper **JP4** to connect $V^–$ and GND. All connections formerly tied to $V^–$ are now at GND.

The supplies are reverse-protected by Schottky diodes and bypassed with 10µF. Additional 1210 capacitors may be added in parallel as needed.

INPUT FILTER

As shown in Figure 3, the 10k R4 and C11 create an input lowpass filter at +IN. C11's value is 33nF for a 480Hz cutoff for LTC2063, 6.8nF for a 2.4kHz cutoff for LTC2066. These pass bands should be sufficient for most input signals.

If an input filter at –IN is desired, the resistors at R1 and R2 may be swapped (R1 = 10k, R2 = 0Ω) and the capacitor C1 populated with either 33nF (for LTC2063) or 6.8nF (LTC2066). Jumper **JP2** must be installed for C1 to be connected.

In general, to minimize the effect of chopper clock feedthrough, signal bandwidths should be limited to at least a decade below the internal chopping frequency, which is 5kHz for LTC2063 and 25kHz for LTC2066.

DEFAULT: UNITY GAIN WITH INPUT FILTER

The default configuration of the board is for unity gain with split supplies, as shown in Figure 3. R4 is 10k for input protection, and R7 is 49.9Ω for 50Ω instrument termination. R5 = 0Ω sets gain at unity. **JP6** ties $\overline{SHDN}$ to V^+ to enable the op amp.

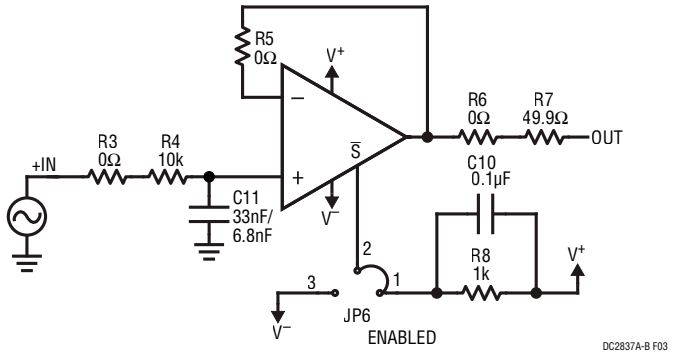

Figure 3. Unity Gain with +IN Lowpass Filter

INVERTING GAIN

$$A_V = -\frac{R_{FB}}{R_G}$$

To set the board up for inverting gain with split supplies (see Figure 4):

1. Populate R5 with the desired R_{FB}
2. Populate R2 with the desired R_G
3. Tie +IN turret to GND (or populate Z4 with 0Ω)
4. Connect the input signal to the –IN turret

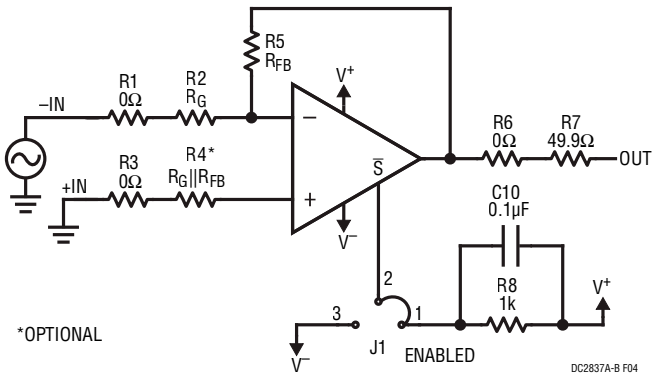

Figure 4. Inverting Gain

OPERATING PRINCIPLES

R4 may be optionally populated with a resistor equivalent to $R_G||R_{FB}$ for increased precision over temperature. R4 will cancel out I_B and potential parasitic thermocouples at the inputs.

NON-INVERTING GAIN

$$A_V = 1 + \frac{R_{FB}}{R_G}$$

To set the board up for non-inverting gain with split supplies (see Figure 5):

1. Populate R5 with the desired R_{FB}
2. Populate R2 with the desired R_G
3. Tie –IN turret to GND (or populate Z3 with 0Ω)
4. Connect the input signal to the +IN turret

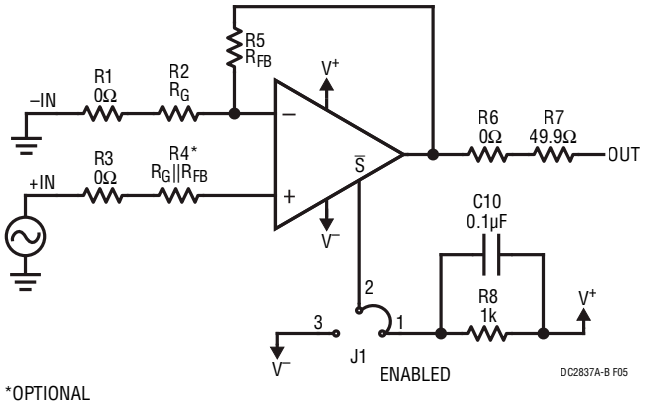

Figure 5. Non-Inverting Gain

R4 may be optionally populated with a resistor equivalent to $R_G||R_{FB}$ for increased precision over temperature. R4 will cancel out I_B and potential parasitic thermocouples at the inputs.

ADDING DC BIASES

To add a DC bias using a resistor divider, populate Z1 and R9/R10 with the same value resistor to set the same DC offset at both inputs. To keep total power consumption in the microwatts, choose R_G and R_{FB} values in the 100's of kilohm to single-digit megohm range.

The circuit in Figure 6 level shifts an input signal's common mode voltage from 0V to mid-rail ($V^+/2$), with inverting gain of $–R_{FB}/R_G$. The DC bias added to –IN is set by divider Z1 and R1, and the DC bias added to +IN is set by divider R9 and R3.

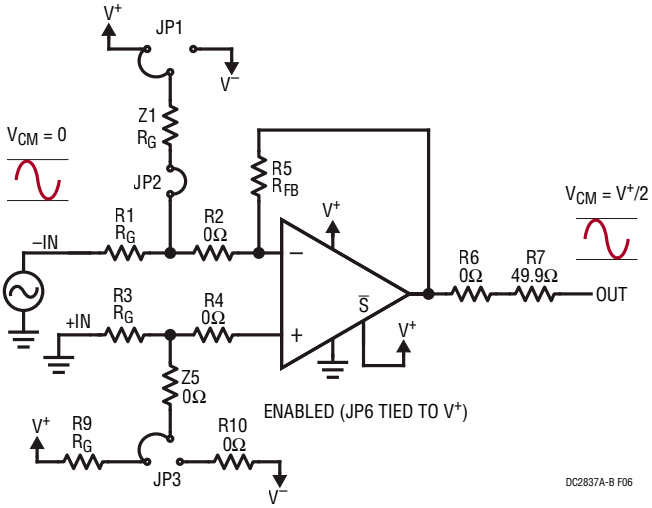

Figure 6. Inverting Gain with DC Bias

To build the Figure 6 level shift circuit with DC2837A:

1. Remove default R1 – R5 and R9
2. Stuff R1, R3, R9, and Z1 with desired R_G
3. Stuff R2, R4, Z5 with 0Ω
4. Stuff R5 with desired R_{FB}
5. Tie +IN turret to GND (or populate Z4 with 0Ω)
6. Jumper settings: JP1 to 1 (V^+), JP3 to 1 (R9), JP2 installed
7. Connect the –IN turret to input signal

OPERATING PRINCIPLES

Negative offsets may also be applied by shifting **JP1** and **JP3** to tie to V^-, and populating R10 instead of R9 with the desired R_G.

SHUTDOWN ENABLE/DISABLE

Jumper **JP6** is provided to enable or disable $\overline{SHDN}$ easily. To filter noise before it reaches the $\overline{SHDN}$ pin, 1k R8 and 0.1µF C10 are provided in series.

To enable the part, tie **JP6** to 1, *EN* or leave it floating. To disable it, tie **JP6** to 3, *DIS*.

To use an external shutdown control signal, remove the jumper at **JP6 completely**, and apply the external signal via the $\overline{SHDN}$ and GND turrets. Remember to apply an offset voltage if the part is being used in single-supply configuration.

If no signal is applied with the jumper at **JP6** completely unstuffed, the part will float to enable by default.

CLOCK FEEDTHROUGH AND INPUT IMPEDANCE

Since the LTC2063/LTC2066 is a zero-drift amplifier, very large R_{FB} or R_G values connected at the inputs can potentially lead to clock feedthrough appearing in the output, especially if the gain setting of the amplifier is not high enough that GBW roll-off will naturally attenuate signals at the clock frequency.

Placing a capacitor in parallel with a large R_{FB} can help filter out this undesired clock signal. On this board, if R_{FB} is R5, a filter capacitor can be stuffed in Z2 if **JP5** is set to connect Z2 and R5 in parallel (default). The filter created by R5 and a capacitor in Z2 must roll-off at least a decade below 5kHz for DC2838A-A (LTC2063) or 25kHz for DC2837A-B (LTC2066) to be effective.

DESIGN EXAMPLE

Figure 7 shows a general textbook second-order active lowpass filter, which may be either a Bessel or Butterworth filter depending on the choice of component values. The equations for this filter are:

$$A_V = \frac{Z1}{R1}$$

$$f_{-3dB} \bullet k = \frac{1}{2\pi\sqrt{C1 \bullet C2 \bullet Z1 \bullet R2}}$$

$$Q = \frac{\sqrt{\frac{C1 \bullet Z1}{C2 \bullet R2}}}{A_V + \frac{Z1}{R2} + 1}$$

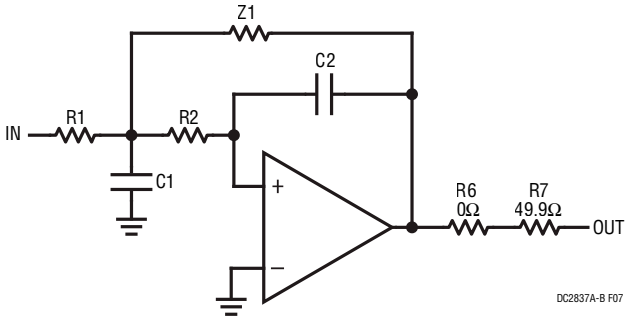

Figure 7. Generic Second-Order Lowpass Filter

OPERATING PRINCIPLES

The following design example will show how to build a **unity-gain, 100Hz f_{-3dB} second-order filter** using DC2837A-A or DC2837A. The target specifications for both a Bessel and a Butterworth filter with this architecture are provided in Table 2.

Table 2. Target Second-Order Butterworth and Bessel Filter Parameters

	BUTTERWORTH	BESSEL
k	1	1.274
Q	0.707	0.577

Populate the board with the component values in Table 3, according to the following instructions and Figure 8.

Table 3. Sample A_V = 1, f_0 = 100Hz Filter Component Values

	BUTTERWORTH	BESSEL
R1	681k	806k
R2	169k	88.7k
Z1	681k	806k
C1	10nF	10nF
C2	2.2nF	2.2nF

1. Stuff Z6 with 0Ω to tie +IN to GND
2. Remove C11 and R5
3. Stuff C1, leave **JP2** connected
4. Replace R1 and R2 with desired values
5. Replace R5 with desired **capacitor C2** value
6. Stuff Z1 with desired value (gain set resistor).
7. Completely remove both jumper connectors from JP1 and **JP5** (leave open)
8. Connect center pin 2 of **JP1** to pin 2 of **JP5**

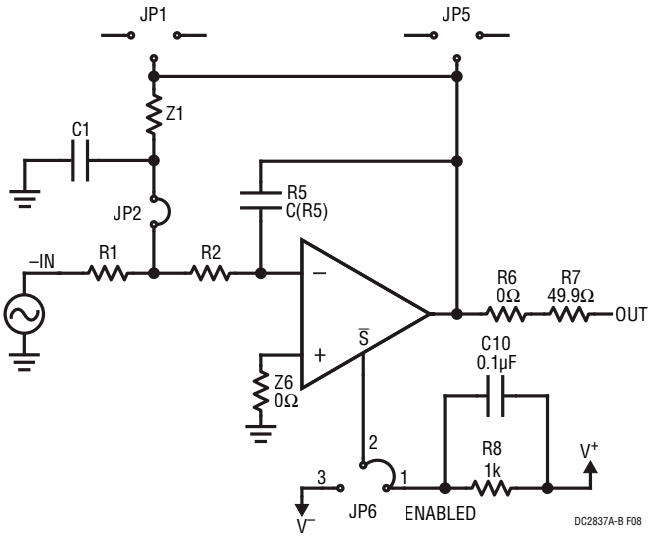

Figure 8. Building A Second-Order Active Lowpass Filter with DC2837A

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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