3.0-A ULTRA-LDO WITH PROGRAMMABLE SOFT-START

Check for Samples: TPS74401-EP

FEATURES

- **Soft-Start (SS) Pin Provides a Linear Startup with Ramp Time Set by External Capacitor**
- **1% Accuracy Over Line, Load, and Temperature**
- **Supports Input Voltages as Low as 0.9 V with External Bias Supply**
- **Adjustable Output (0.8 V to 3.6 V)**
- **Ultra-Low Dropout: 115 mV at 3.0 A (typ)**
- **Stable with Any or No Output Capacitor**
- **Excellent Transient Response**
- **Available in 5 mm × 5 mm × 1 mm QFN Package**
- **Active High Enable**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Ranges**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

APPLICATIONS

- **FPGA Applications**
- **DSP Core and I/O Voltages**
- **Post-Regulation Applications**
- **Applications with Special Start-Up Time or Sequencing Requirements**
- **Hot-Swap and Inrush Controls**

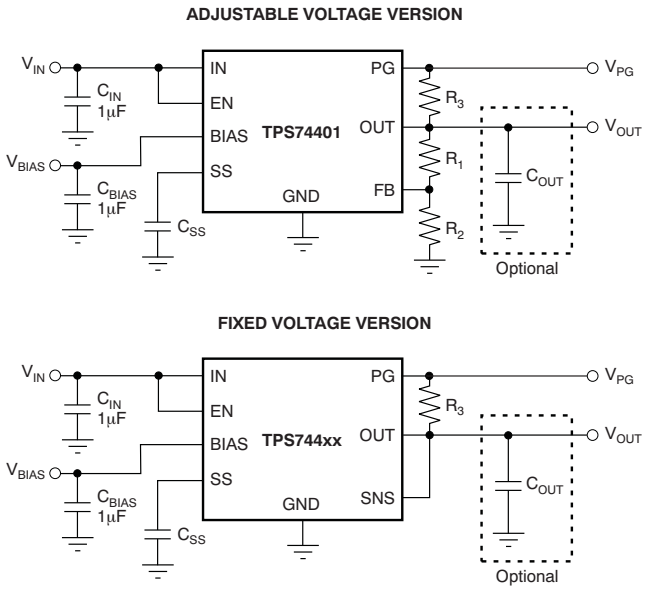


Figure 1. Typical Application Circuit

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The TPS74401 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that will meet the sequencing requirements of FPGAs, DSPs, and other applications with specific start-up requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. Each LDO is stable with low-cost ceramic output capacitors and the device is fully specified from –55°C to 125°C.

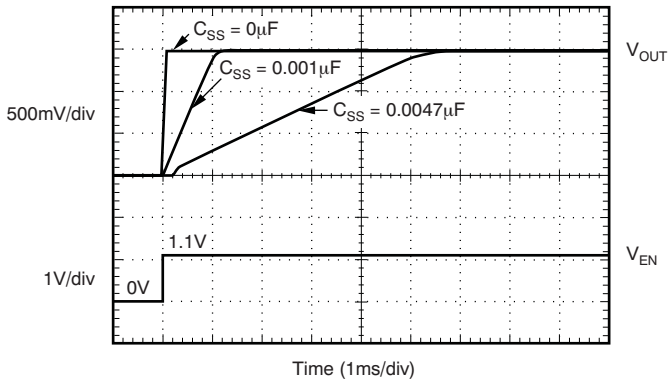


Figure 2. Turn-On Response

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	QFN (RGW)	Reel of 3000	TPS74401MRGWREP	TPS74401EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –55°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

			UNIT
V_{IN}, V_{BIAS}	Input voltage range	–0.3 to +6	V
V_{EN}	Enable voltage range	–0.3 to +6	V
V_{PG}	Power-good voltage range	–0.3 to +6	V
I_{PG}	PG sink current	0 to +1.5	mA
V_{SS}	SS pin voltage range	–0.3 to +6	V
V_{FB}	Feedback pin voltage range	–0.3 to +6	V
V_{OUT}	Output voltage range	–0.3 to V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited	
	Output short circuit duration	Indefinite	
T_J	Operating junction temperature range	–55 to +125	°C
T_{STG}	Storage junction temperature range	–65 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS74401-EP	UNITS
		RGW (20 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	36.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34.3	
θ_{JB}	Junction-to-board thermal resistance	10.8	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	11.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

ELECTRICAL CHARACTERISTICS

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{IN} = C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –55°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.375		5.25	V
V_{REF}	Internal reference (Adj.)		0.792		0.808	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A, V_{BIAS} = 5 V	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.25 V, 50 mA ≤ I_{OUT} ≤ 3.0 A	–1	±0.2	+1	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.0005	0.05	%/V
V_{OUT}/I_{OUT}	Load regulation	0mA ≤ I_{OUT} ≤ 50 mA		0.013		%/mA
		50 mA ≤ I_{OUT} ≤ 3.0 A		0.03		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 3.0 A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62 V		120	195	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 3.0 A, V_{IN} = V_{BIAS}			1.62	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$	3.7		6.0	A
I_{BIAS}	Bias pin current	I_{OUT} = 0 mA to 3.0 A		2	4	mA
I_{SHDN}	Shutdown supply current (V_{IN})	V_{EN} ≤ 0.4 V		0.4	1	µA
I_{FB}	Feedback pin current(3)	I_{OUT} = 50 mA to 3.0 A	–250	95	250	nA
PSRR(4)	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		73		dB
		800 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		42		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		62		dB
		800 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 0.001 µF		16 × V_{OUT}		μV_{RMS}
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 100 mA to 3.0 A at 1 A/µs, C_{OUT} = 0 µF		4		%V_{OUT}
t_{STR}	Minimum startup time	I_{OUT} = 1.5 A, C_{SS} = open		100		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V	0.5	0.73	1	µA
$V_{EN,\ HI}$	Enable input high level		1.1		5.5	V
$V_{EN,\ LO}$	Enable input low level		0		0.4	V
$V_{EN,\ HYS}$	Enable pin hysteresis			50		mV
$V_{EN,\ DG}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG,\ LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	µA
T_J	Operating junction temperature		–55		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+155		°C
		Reset, temperature decreasing		+140		

(1) Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
(3) I_{FB} current flow is out of the device.
(4) See Figure 10 to Figure 13 for PSRR at different conditions.

BLOCK DIAGRAM

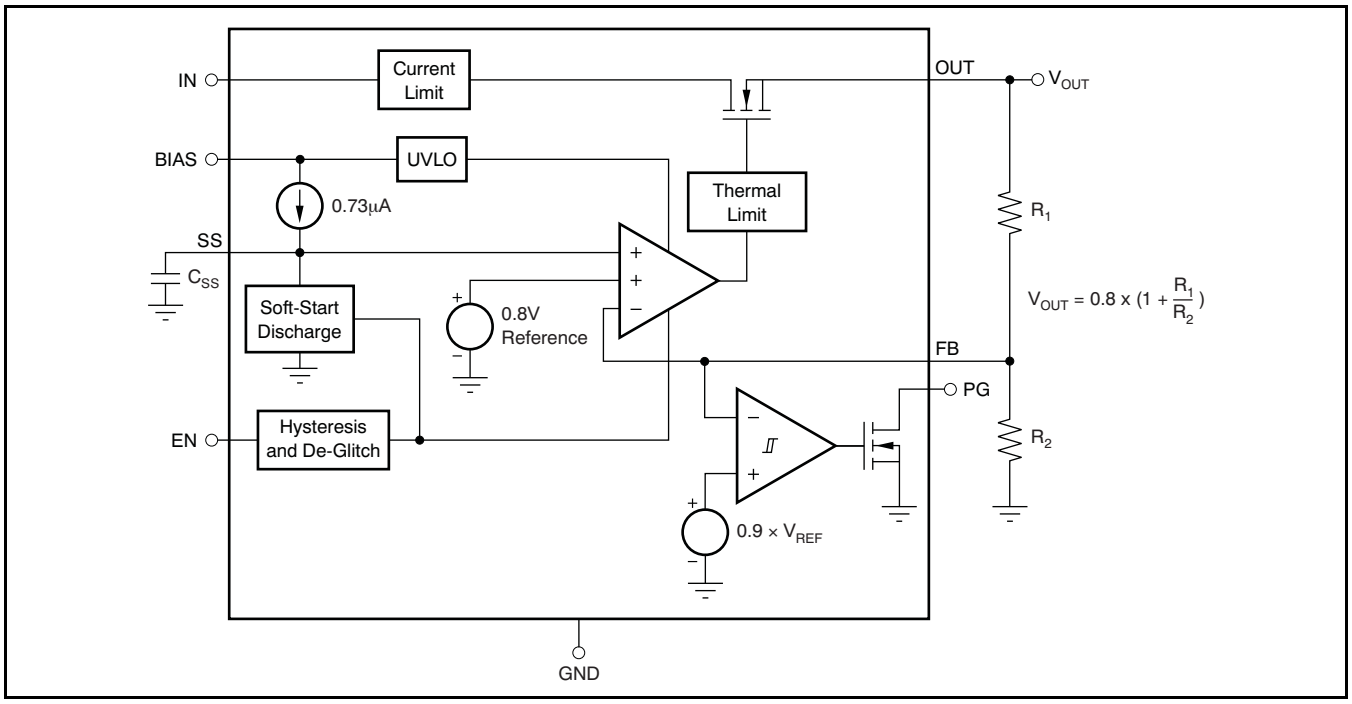


Table 2. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

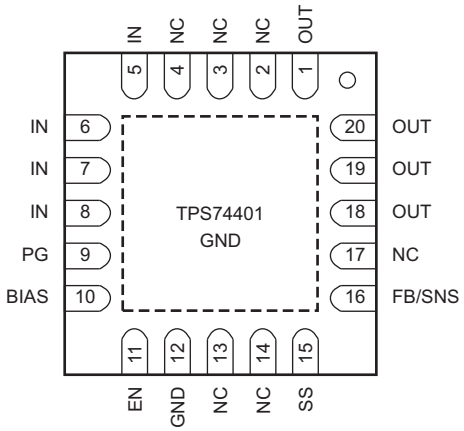
(1) $V_{OUT} = 0.8 \times (1 + R_1/R_2)$

Table 3. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
470 pF	0.5 ms
1000 pF	1 ms
4700 pF	5 ms
0.01 μF	10 ms
0.015 μF	16 ms

(1) $t_{SS}(s) = 0.8 \times C_{SS}(F)/7.3 \times 10^{-7}$

RGW PACKAGE
(TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
IN	5–8	Unregulated input to the device.
EN	11	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
SS	15	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100μs.
BIAS	10	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	9	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10kΩ to 1MΩ should be connected from this pin to a supply up to 5.5V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
FB	16	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	1, 18–20	Regulated output voltage. No capacitor is required on this pin for stability.
NC	2–4, 13, 14, 17	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	12	Ground
PAD/TAB		Should be soldered to the ground plane for increased thermal performance.

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

LOAD REGULATION

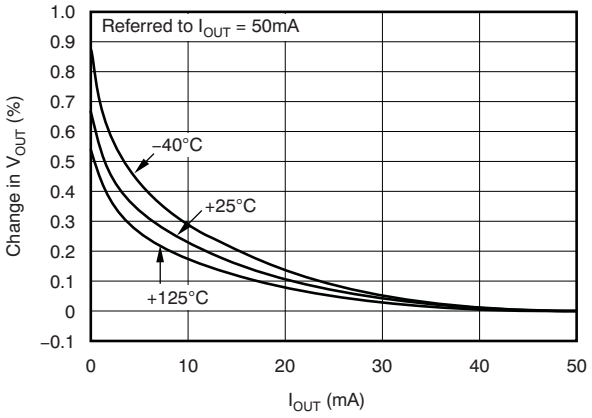


Figure 3.

LOAD REGULATION

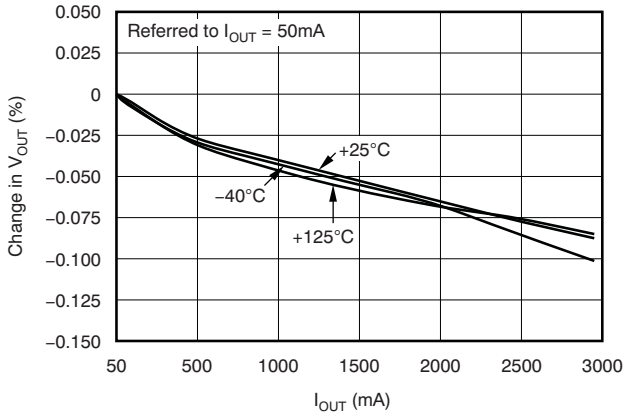


Figure 4.

LINE REGULATION

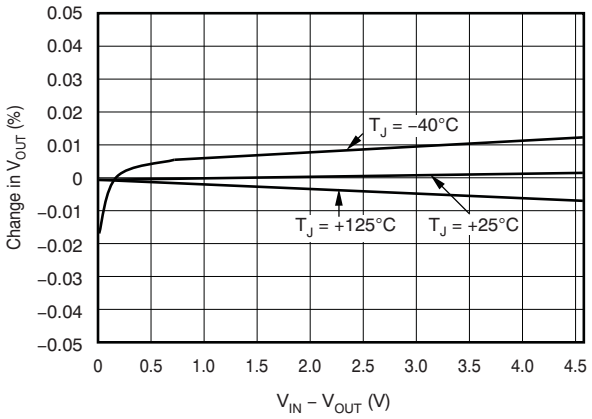


Figure 5.

V_{IN} DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE (T_J)

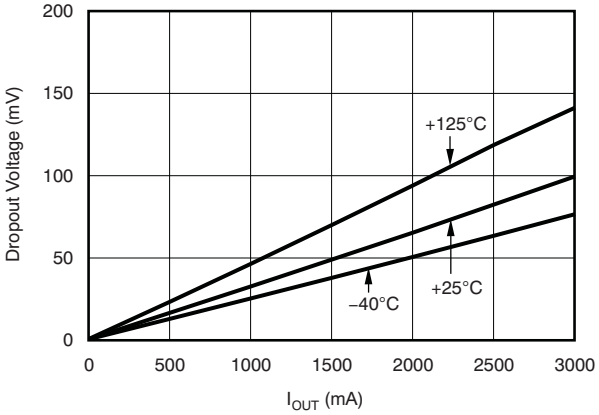


Figure 6.

V_{IN} DROPOUT VOLTAGE vs V_{BIAS} − V_{OUT} AND TEMPERATURE (T_J)

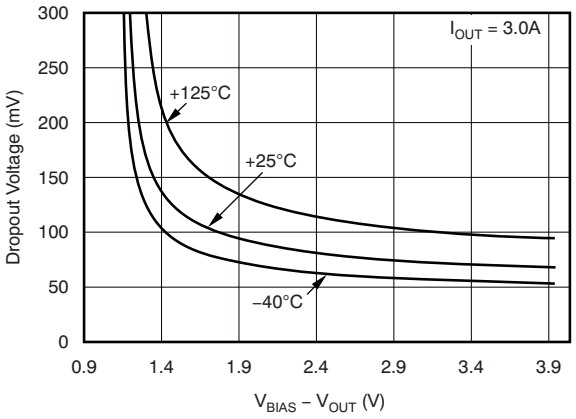


Figure 7.

V_{IN} DROPOUT VOLTAGE vs V_{BIAS} − V_{OUT} AND TEMPERATURE (T_J)

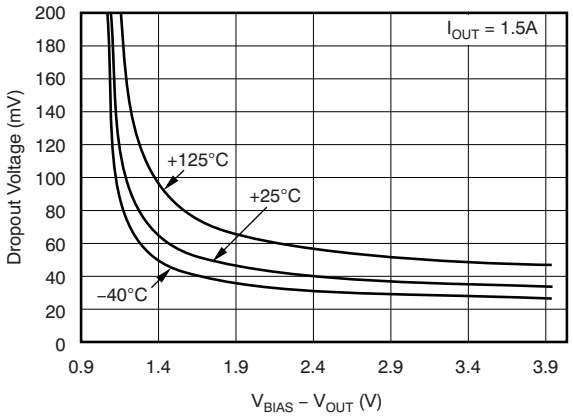


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

V_{BIAS} DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE (T_J)

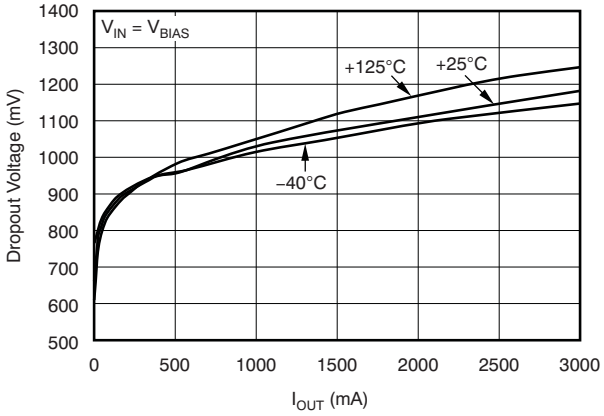


Figure 9.

V_{BIAS} PSRR vs FREQUENCY

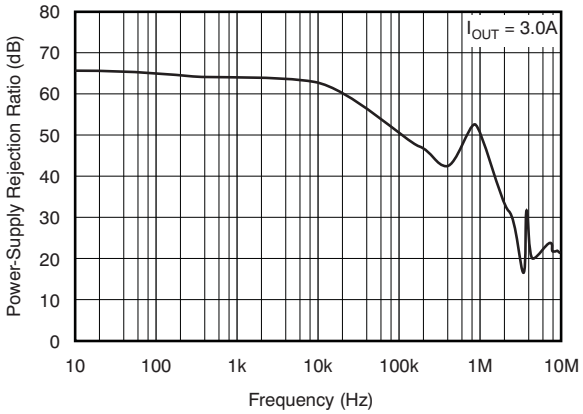


Figure 10.

V_{IN} PSRR vs FREQUENCY

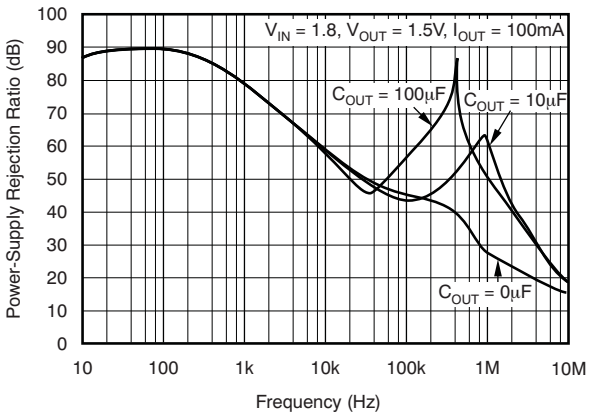


Figure 11.

V_{IN} PSRR vs FREQUENCY

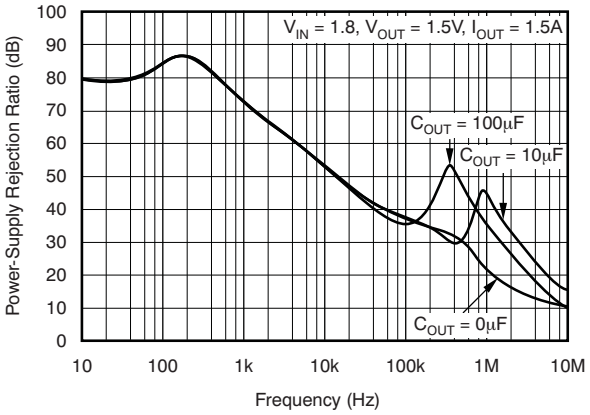


Figure 12.

V_{IN} PSRR vs FREQUENCY

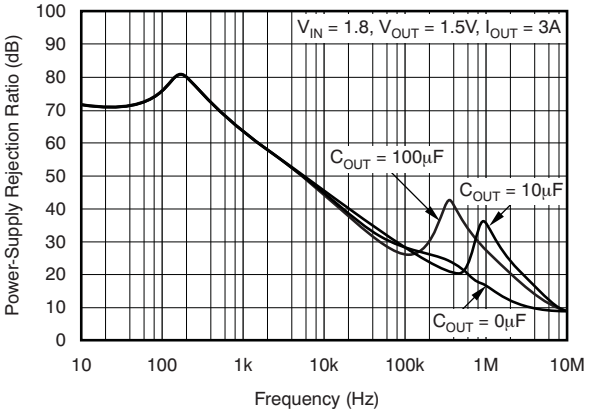


Figure 13.

V_{IN} PSRR vs V_{IN} – V_{OUT}

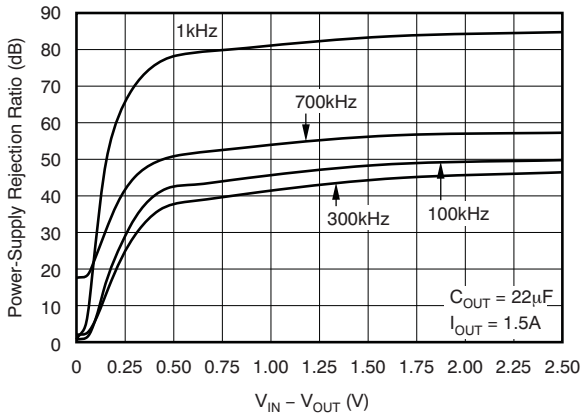


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

NOISE SPECTRAL DENSITY

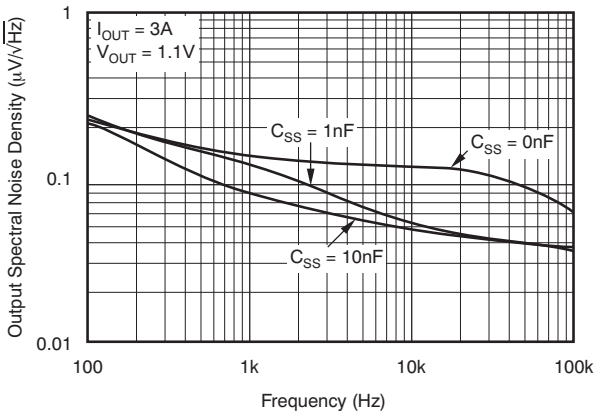


Figure 15.

NOISE SPECTRAL DENSITY

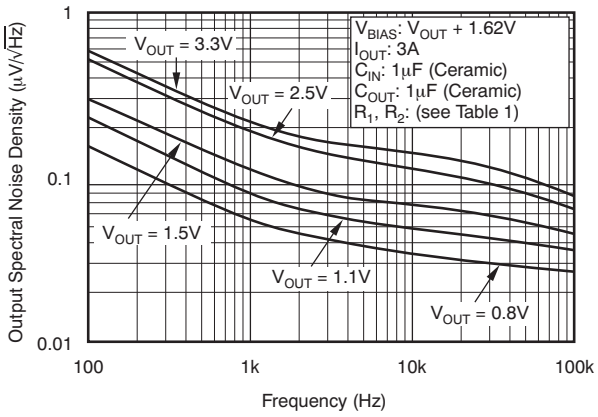


Figure 16.

I_{BIAS} vs I_{OUT} AND TEMPERATURE

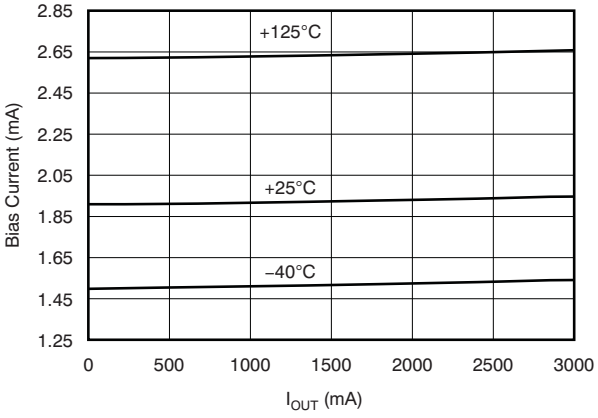


Figure 17.

I_{BIAS} vs V_{BIAS} AND V_{OUT}

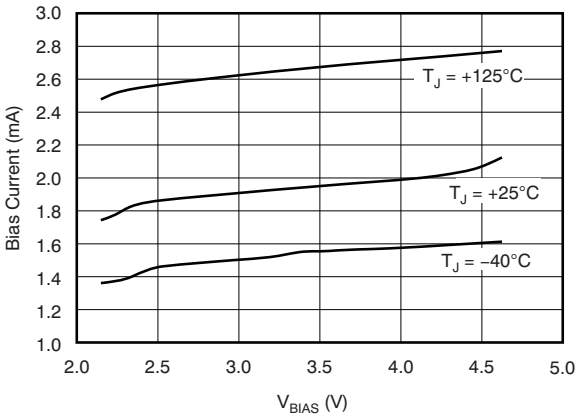


Figure 18.

I_{BIAS} SHUTDOWN vs TEMPERATURE

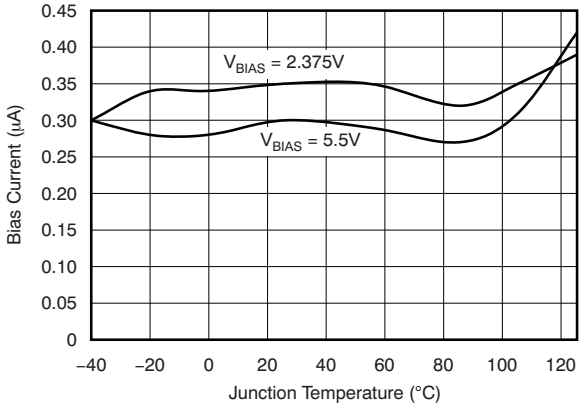


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

SOFT-START CHARGING CURRENT (I_{SS}) vs TEMPERATURE

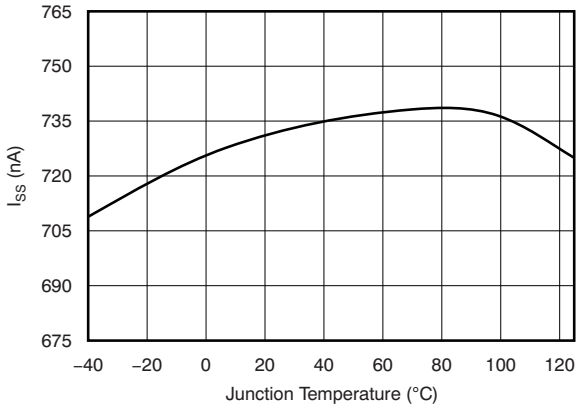


Figure 20.

LOW-LEVEL PG VOLTAGE vs PG CURRENT

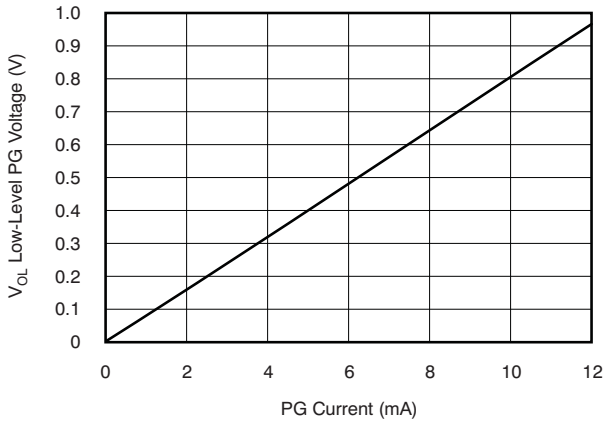


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

LOAD TRANSIENT RESPONSE

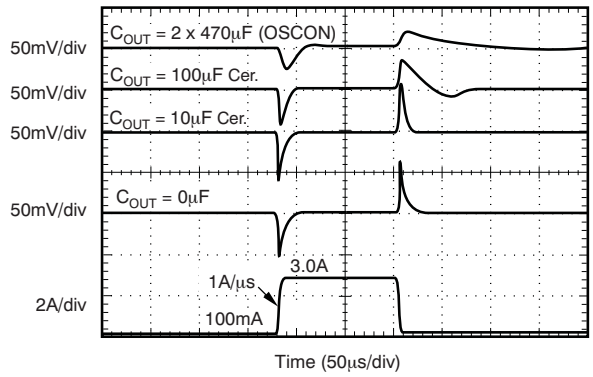


Figure 22.

V_{BIAS} LINE TRANSIENT (3A)

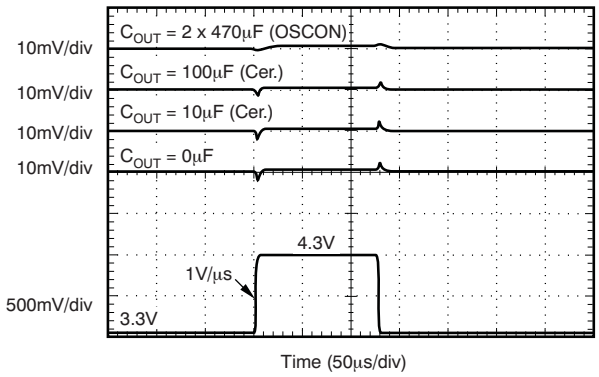


Figure 23.

V_{IN} LINE TRANSIENT (3A)

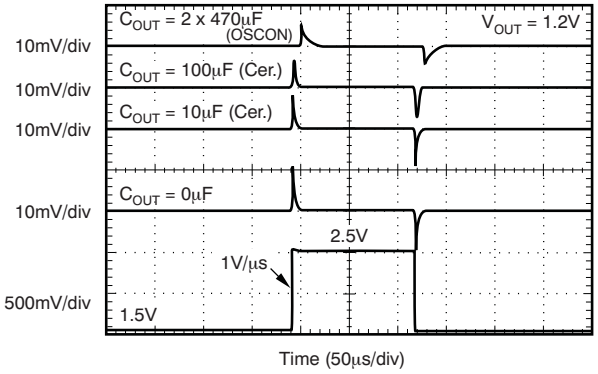


Figure 24.

TURN-ON RESPONSE

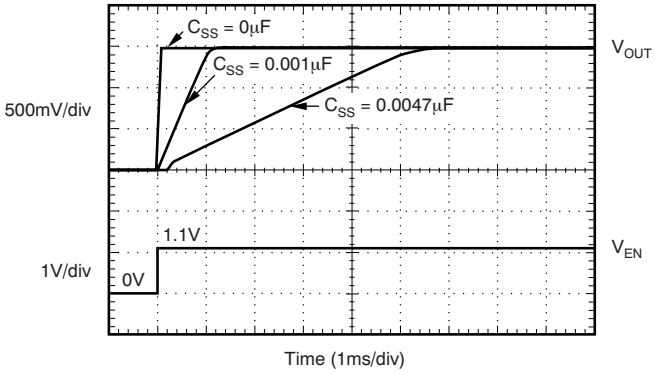


Figure 25.

POWER-UP/POWER-DOWN

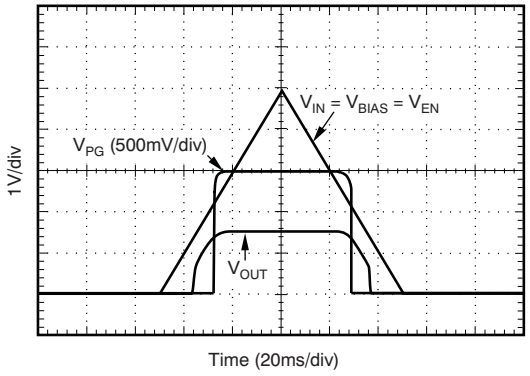


Figure 26.

OUTPUT SHORT-CIRCUIT RECOVERY

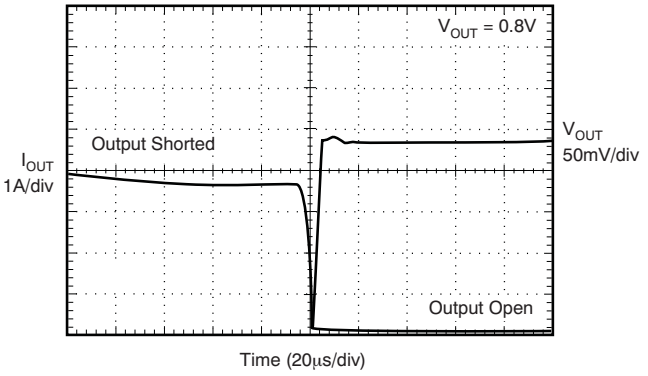


Figure 27.

APPLICATION INFORMATION

The TPS74401 belongs to a family of new generation ultra-low dropout regulators that feature soft-start and tracking capabilities. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74401 to be stable with any or even no output capacitor. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74401 features a programmable, voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

Figure 28 illustrates a typical application circuit for the TPS74401 adjustable output device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 28. Refer to Table 2 for sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 should be ≤ 4.99 kΩ.

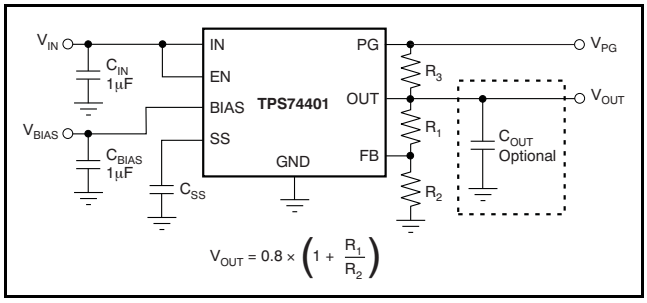


Figure 28. Typical Application Circuit for the TPS74401 (Adjustable)

INPUT, OUTPUT, AND BIAS CAPACITOR REQUIREMENTS

The device does not require any output capacitor for stability. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

TRANSIENT RESPONSE

The TPS74401 was designed to have transient response within 5% for most applications without any output capacitor. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time. Refer to Figure 22 in the Typical Characteristics section. Since the TPS74401 is stable without an output capacitor, many applications may allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

DROPOUT VOLTAGE

The TPS74401 offers industry-leading dropout performance, making it well-suited for high-current low V_{IN}/low V_{OUT} applications. The extremely low dropout of the TPS74401 allows the device to be used in place of a DC/DC converter and still achieve good efficiencies. This efficiency allows users to rethink the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74401. The first specification (see Figure 29) is referred to as *V_{IN} Dropout* and is for users that wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3-V rail with 5% tolerance and with V_{OUT} = 1.5V. If V_{BIAS} is higher than 3.3 V × 0.95 or V_{OUT} is less than 1.5 V, V_{IN} dropout is less than specified.

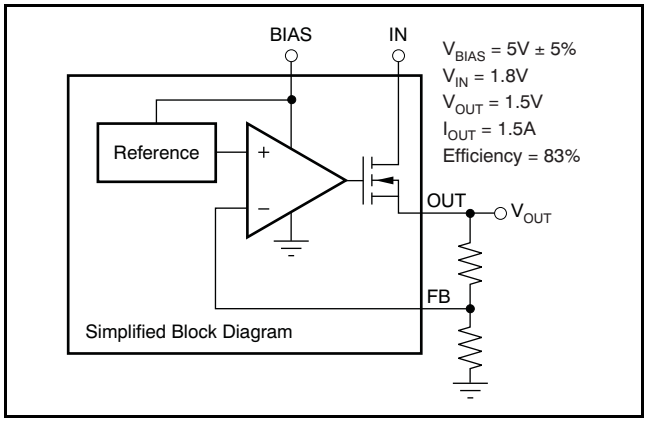


Figure 29. Typical Application of the TPS74401 Using an Auxiliary Bias Rail

The second specification (see Figure 30) is referred to as *V_{BIAS} Dropout* and is for users that wish to tie IN and BIAS together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.62 V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

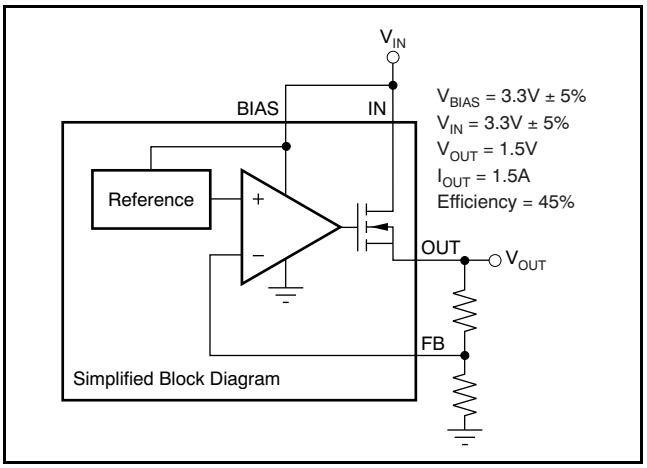


Figure 30. Typical Application of the TPS74401 Without an Auxiliary Bias

PROGRAMMABLE SOFT-START

The TPS74401 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74401 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), the soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (2)$$

$V_{OUT(NOM)}$ is the nominal set output voltage as set by the user, C_{OUT} is the output capacitance, and $I_{CL(MIN)}$ is the minimum current limit for the device. In applications where monotonic startup is required, the soft-start time given by Equation 1 should be set to be greater than Equation 2.

The maximum recommended soft-start capacitor is 0.015 μF. Larger soft-start capacitors can be used and will not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when re-enabled. Soft-start capacitors larger than 0.015 μF could be a problem in applications where the user needs to rapidly pulse the enable pin and still requires the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Refer to Table 3 for suggested soft-start capacitor values.

SEQUENCING REQUIREMENTS

The device can have V_{IN}, V_{BIAS}, and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} and V_{BIAS} are present is preferred, and can be accomplished using a digital output from a processor or supply supervisor. An analog signal from an external RC circuit, as shown in Figure 31, can also be used as long as the delay time is long enough for V_{IN} and V_{BIAS} to be present.

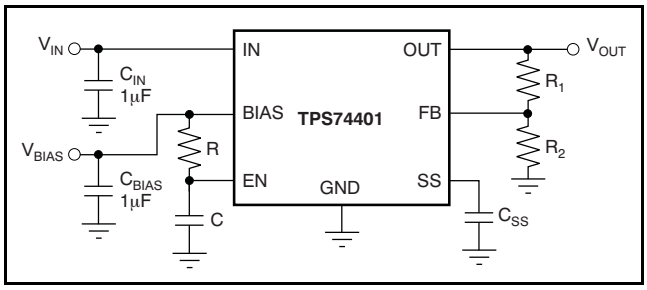


Figure 31. Soft-Start Delay Using an RC Circuit on Enable

If a signal is not available to enable the device after IN and BIAS, simply connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output will track the slower supply minus the dropout voltage until it reaches the set output voltage. If EN is connected to BIAS, the device will soft-start as programmed provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired then V_{OUT} will track V_{IN}.

NOTE: When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 μA of current from OUT. Although this condition will not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

OUTPUT NOISE

The TPS74401 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-μF soft-start capacitor, the output noise is reduced by half and is typically 19 μV_{RMS} for a 1.2-V output (100 Hz to 100 kHz). Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-μF soft-start capacitor is given in Equation 3.

$$V_N(\mu V_{RMS}) = 16\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

The low output noise of the TPS74401 makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

ENABLE/SHUTDOWN

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4 V turns the regulator off, while V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow-ramping analog signals. This configuration allows the TPS74401 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, a fast rise-time signal should be used to enable the TPS74401.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

POWER-GOOD (QFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pull-up resistor. This pin requires at least 1.1 V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the

pull-up resistor for PG should be in the range of 10 kΩ to 1 MΩ. The pull-up resistor for PG should be in the range of 10 kΩ to 1 MΩ. PG is only provided on the QFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

INTERNAL CURRENT LIMIT

The TPS74401 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 3.5 A and maintain regulation. The current limit responds in about 10 μs to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Figure 27 in the Typical Characteristics section for short-circuit recovery performance.

The internal current limit protection circuitry of the TPS74401 is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS74401 above the rated current degrades device reliability.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +30°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74401 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS74401 into thermal shutdown degrades device reliability.

LAYOUT RECOMMENDATIONS AND POWER DISSIPATION

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 28 should be connected as close as possible to the load. If BIAS is connected to IN, it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

The primary conduction path for heat is through the exposed pad or tab to the printed circuit board (PCB). The pad or tab can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125^{\circ}C - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$ and system air flow, the minimum amount of PCB copper area needed for appropriate heatsinking can be calculated using Figure 32 through Figure 34.

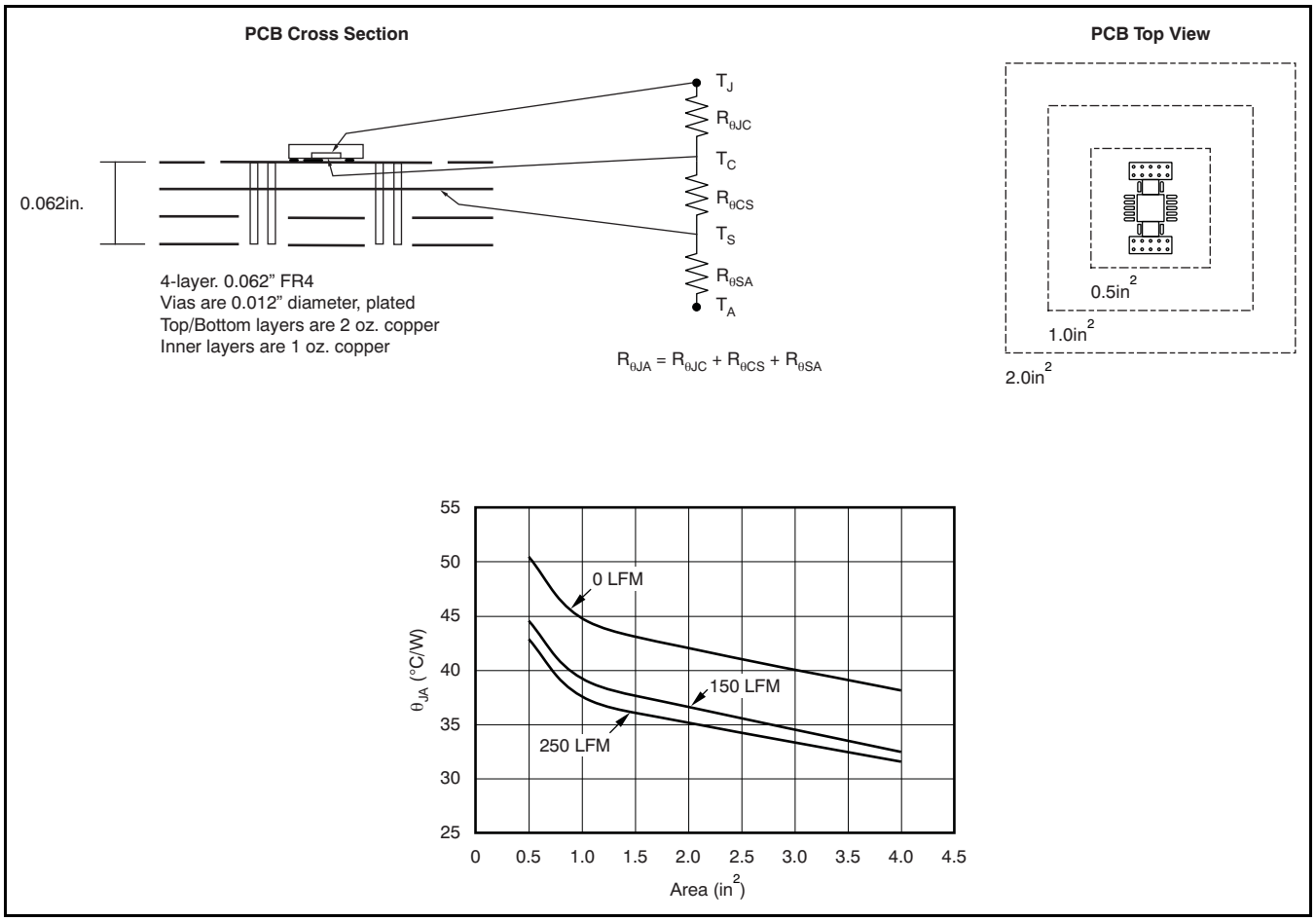


Figure 32. PCB Layout and Corresponding $R_{\theta JA}$ Data, Buried Thermal Plane, No Vias Under Thermal Pad

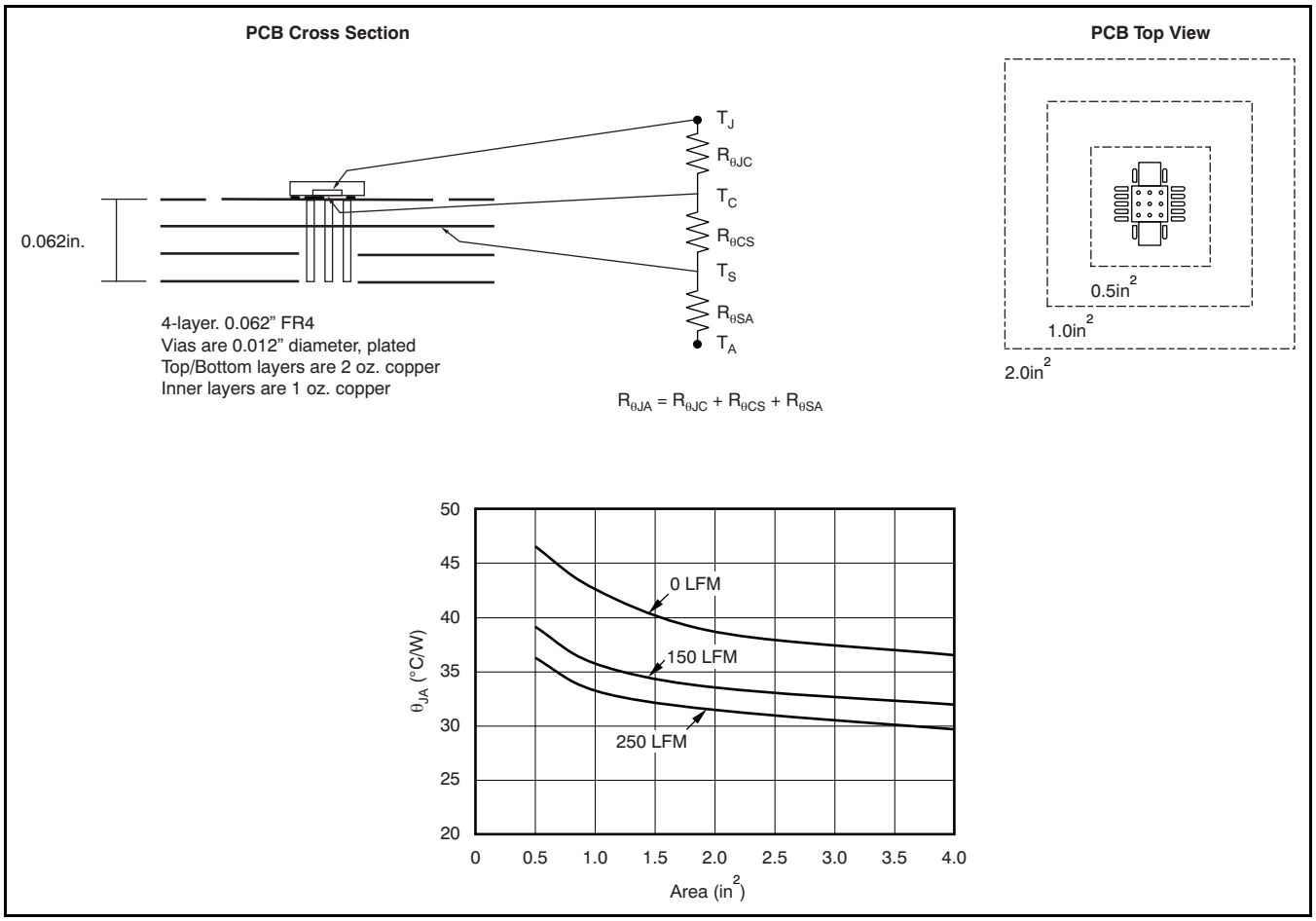


Figure 33. PCB Layout and Corresponding $R_{\theta JA}$ Data, Buried Thermal Plane, Vias Under Thermal Pad

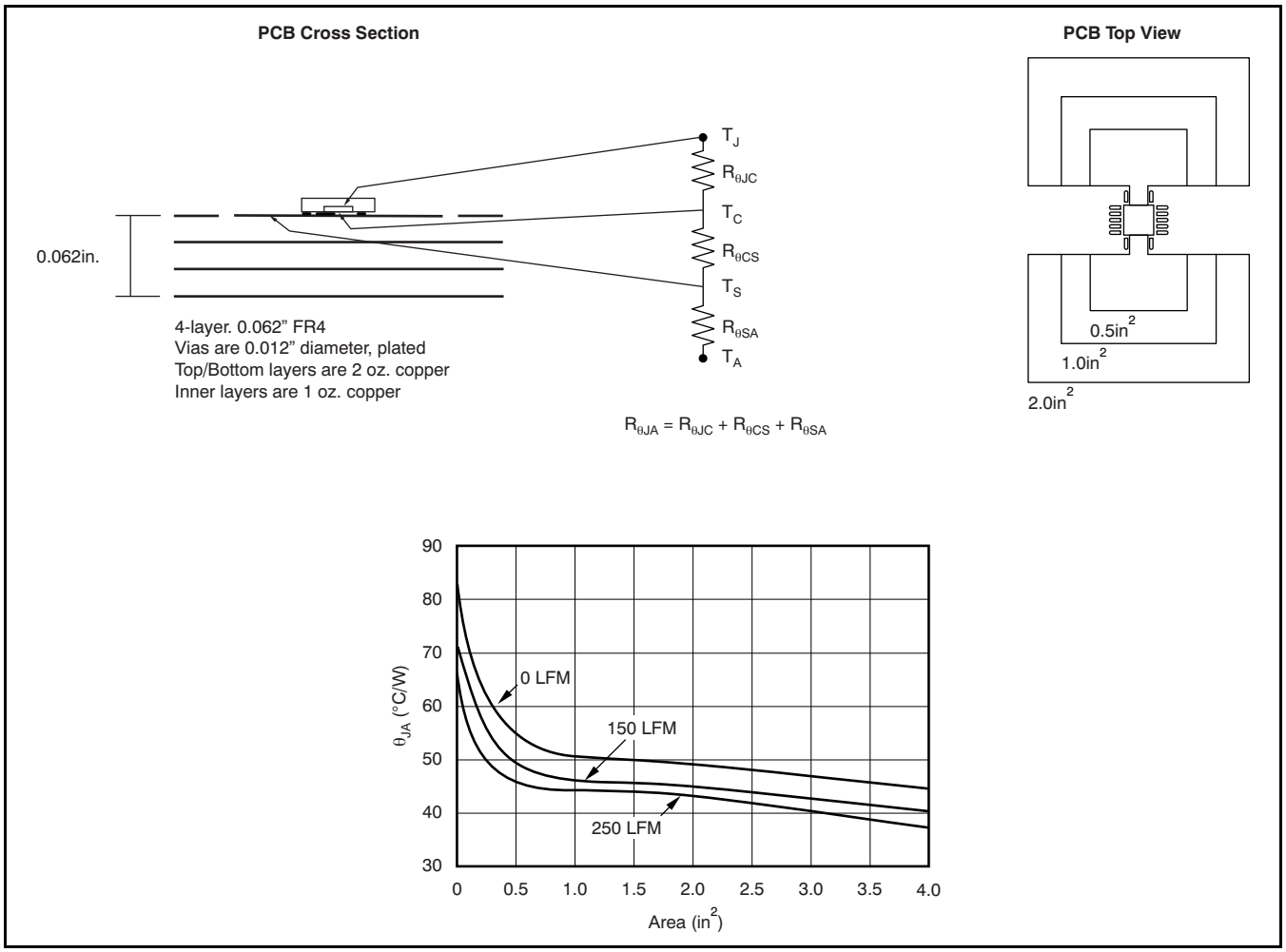


Figure 34. PCB Layout and Corresponding $R_{\theta JA}$ Data, Top Layer Thermal Plane

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74401MRGWREP	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TPS 74401EP	Samples
V62/10611-01XE	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TPS 74401EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS74401-EP :

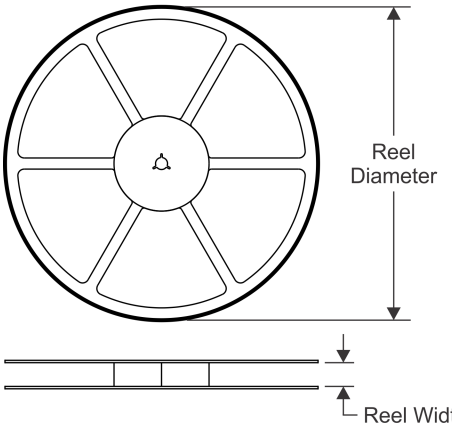
- Catalog: TPS74401

NOTE: Qualified Version Definitions:

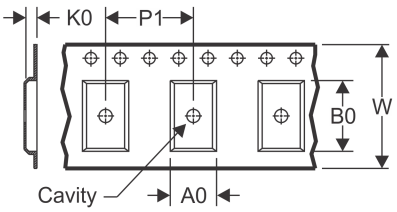
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

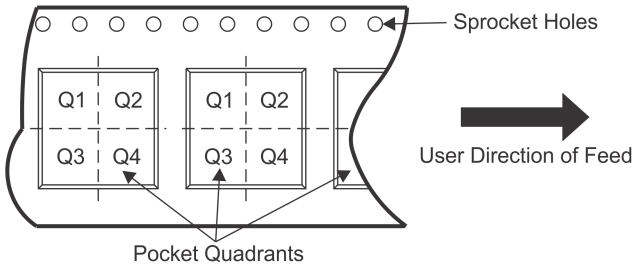


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

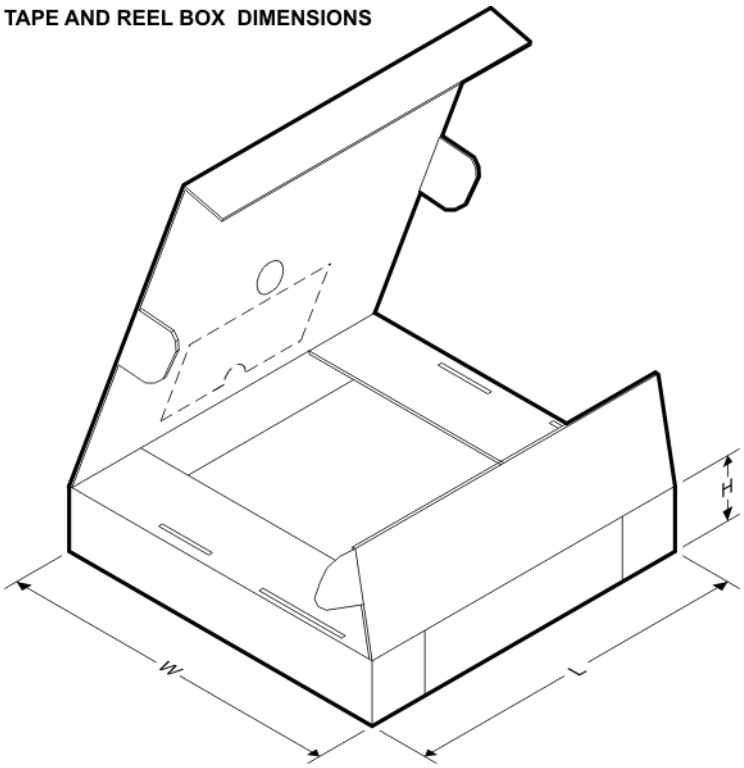
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74401MRGWREP	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

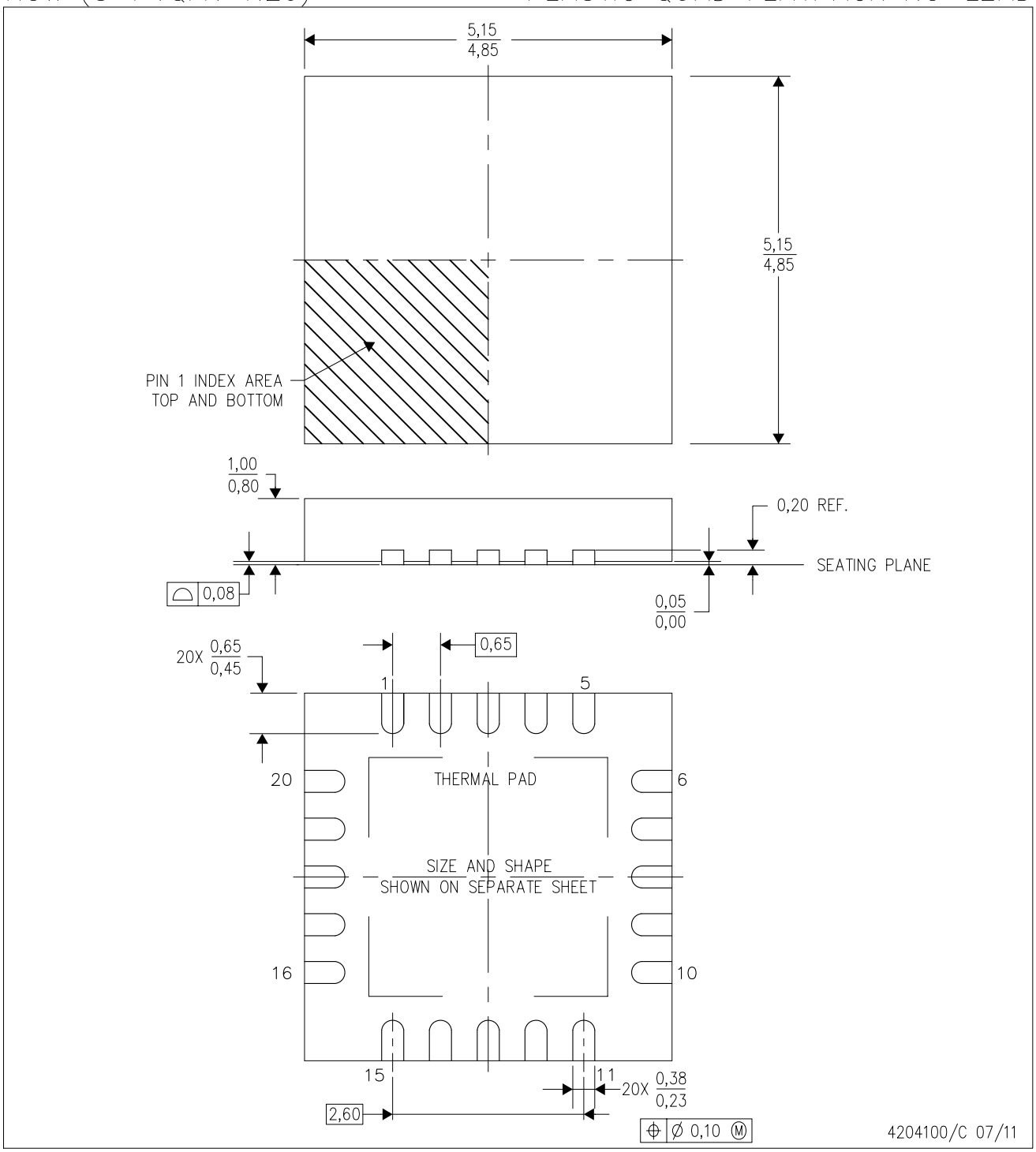
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74401MRGWREP	VQFN	RGW	20	3000	853.0	449.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

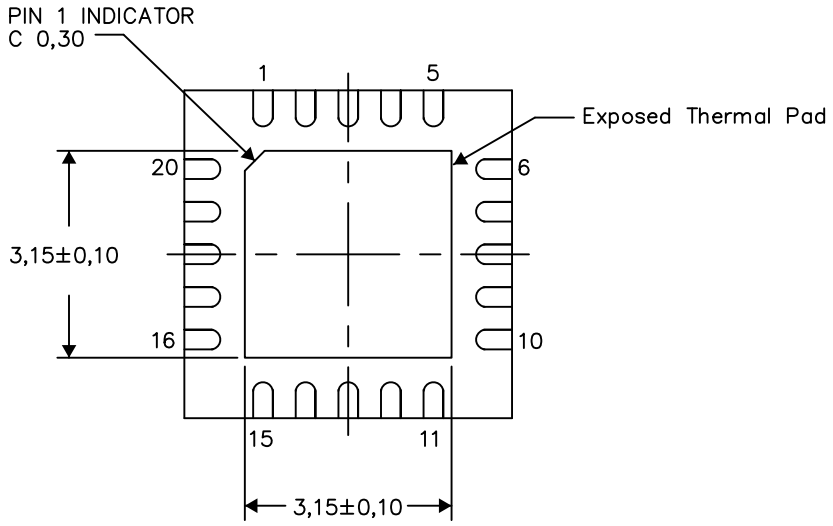
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



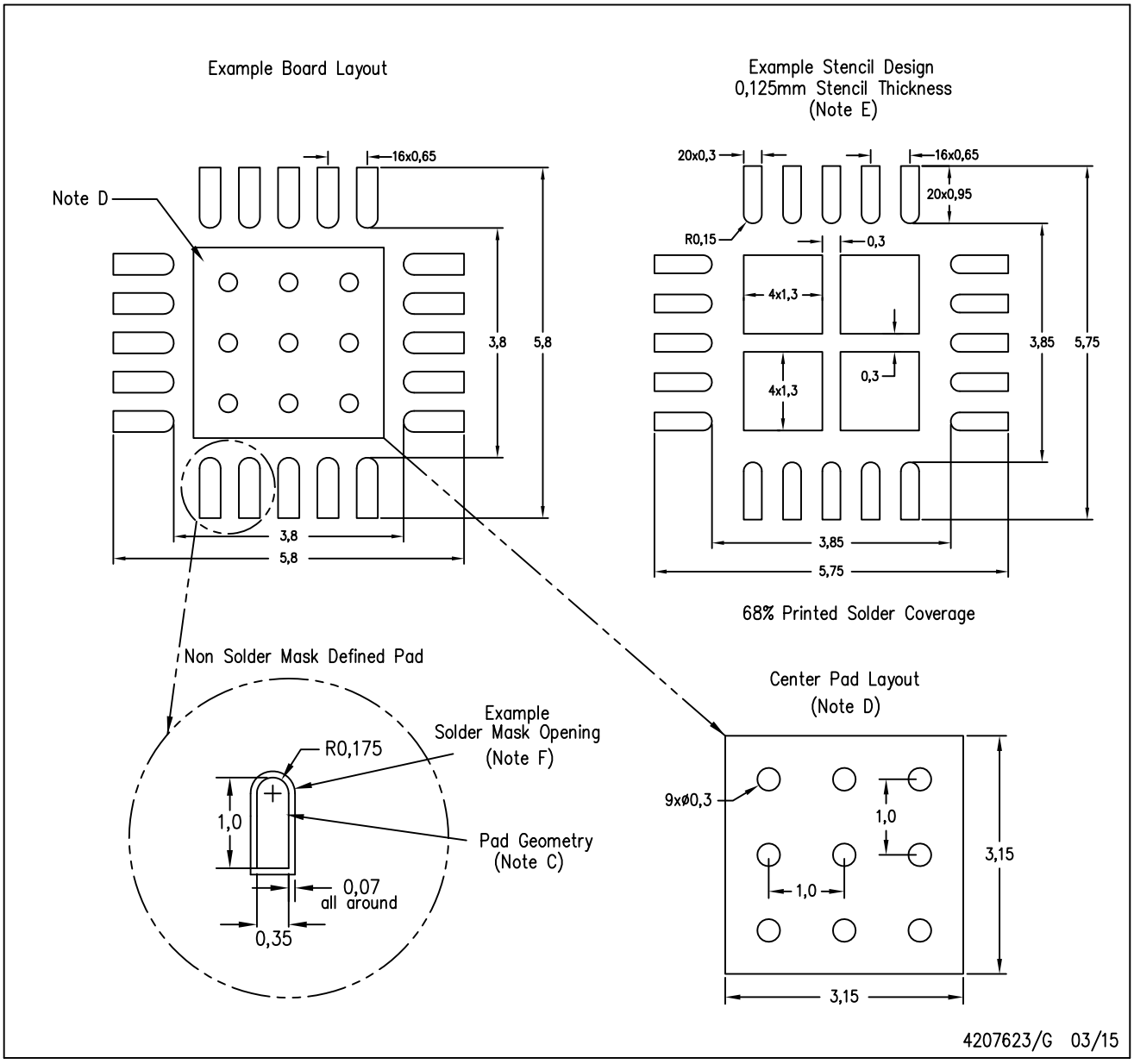
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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