



QFN



HTQFP

# 10-W STEREO CLASS-D AUDIO POWER AMPLIFIER

Check for Samples: [TPA3101D2](#)

## FEATURES

- 10-W/ch into an 8-Ω Load From a 13-V Supply
- 9.2-W/ch into an 8-Ω Load From a 12-V Supply
- Operates from 10 V to 26 V
- 87% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Four Selectable, Fixed Gain Settings
- Differential Inputs
- Thermal and Short-Circuit Protection With Auto Recovery Feature
- Clock Output for Synchronization With Multiple Class-D Devices
- Surface Mount 7 mm × 7 mm, 48-pin QFN Package
- Surface Mount 7 mm × 7 mm, 48-pin HTQFP Package

## APPLICATIONS

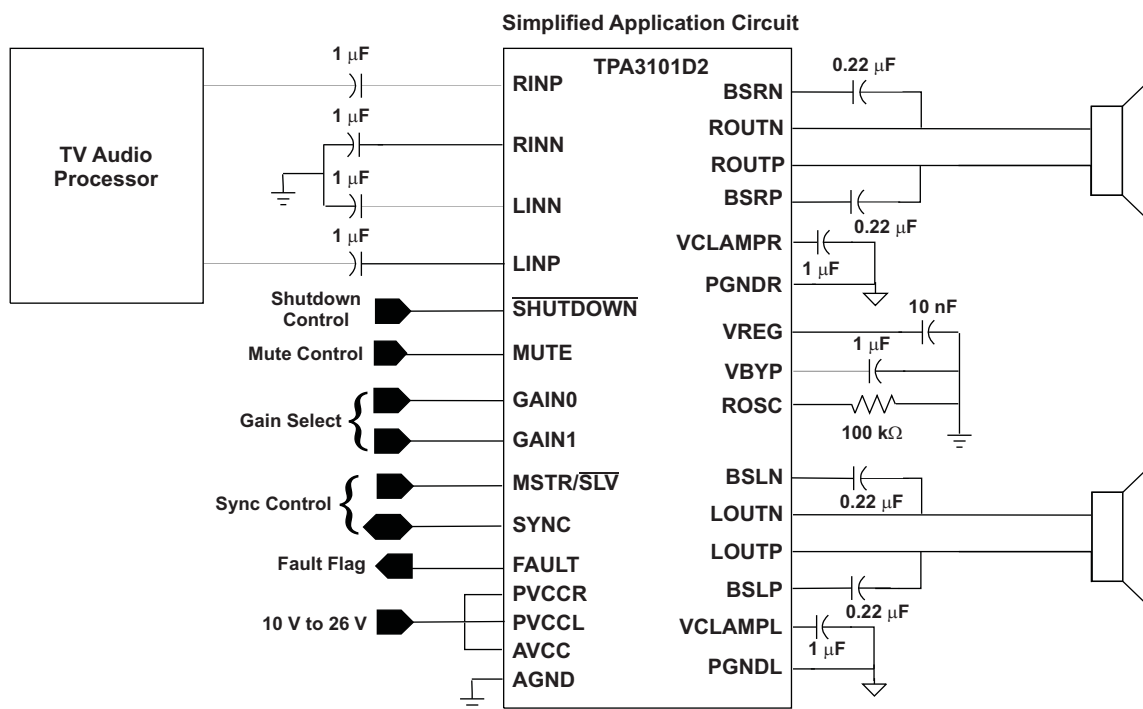
- Televisions

## DESCRIPTION

The TPA3101D2 is a 10-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. The TPA3101D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3101D2, 87%, eliminates the need for an external heat sink when playing music.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, 36 dB.

The outputs are fully protected against shorts to GND,  $V_{CC}$ , and output-to-output shorts with an auto recovery feature and monitor output.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                    |                                                     |                                                                            | UNIT                              |
|------------------------------------|-----------------------------------------------------|----------------------------------------------------------------------------|-----------------------------------|
| V <sub>CC</sub>                    | Supply voltage                                      | AVCC, PVCC                                                                 | –0.3 V to 30 V                    |
| V <sub>I</sub>                     | Input voltage                                       | SHUTDOWN, MUTE                                                             | –0.3 V to V <sub>CC</sub> + 0.3 V |
|                                    |                                                     | GAIN0, GAIN1, RINN, RINP, LINN, LINP, MSTR/ $\overline{\text{SLV}}$ , SYNC | –0.3 V to VREG + 0.5 V            |
| Continuous total power dissipation |                                                     |                                                                            | See Thermal Information Table     |
| T <sub>A</sub>                     | Operating free-air temperature range                |                                                                            | –40°C to 85°C                     |
| T <sub>J</sub>                     | Operating junction temperature range <sup>(2)</sup> |                                                                            | –40°C to 150°C                    |
| T <sub>stg</sub>                   | Storage temperature range                           |                                                                            | –65°C to 150°C                    |
| R <sub>(Load)</sub>                | Load Resistance                                     |                                                                            | 3.2 Ω Minimum                     |
|                                    | Electrostatic discharge                             | Human body model <sup>(3)</sup> (all pins)                                 | ±2 kV                             |
|                                    |                                                     | Machine model <sup>(4)</sup> (all pins)                                    | ±200 V                            |
|                                    |                                                     | Charged-device model <sup>(5)</sup> (all pins)                             | ±500 V                            |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The TPA3101D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs [SCBA017D](#) and [SLUA271](#) for more information about using the QFN thermal pad. See TI Technical Briefs [SLMA002](#) for more information about using the HTQFP thermal pad.
- (3) In accordance with JEDEC Standard 22, Test Method A114-B.
- (4) In accordance with JEDEC Standard 22, Test Method A115-A.
- (5) In accordance with JEDEC Standard 22, Test Method C101-A.

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> (2) |                                              | PHP       | RGZ       | UNITS |
|-----------------------------------|----------------------------------------------|-----------|-----------|-------|
|                                   |                                              | 48 (PINS) | 48 (PINS) |       |
| $\theta_{JA}$                     | Junction-to-ambient thermal resistance       | 28.5      | 26.4      | °C/W  |
| $\theta_{JCTop}$                  | Junction-to-case (top) thermal resistance    | 19        | 19        |       |
| $\theta_{JB}$                     | Junction-to-board thermal resistance         | 10.5      | 14.4      |       |
| $\psi_{JT}$                       | Junction-to-top characterization parameter   | 0.3       | 0.2       |       |
| $\psi_{JB}$                       | Junction-to-board characterization parameter | 6.4       | 6.3       |       |
| $\theta_{JCbott}$                 | Junction-to-case (bottom) thermal resistance | 0.7       | 1.7       |       |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                          | TEST CONDITIONS                                                    | MIN | MAX | UNIT |
|-----------------|--------------------------|--------------------------------------------------------------------|-----|-----|------|
| V <sub>CC</sub> | Supply voltage           | PVCC, AVCC                                                         | 10  | 26  | V    |
| V <sub>IH</sub> | High-level input voltage | SHUTDOWN, MUTE, GAIN0, GAIN1, MSTR/ $\overline{\text{SLV}}$ , SYNC | 2   |     | V    |
| V <sub>IL</sub> | Low-level input voltage  | SHUTDOWN, MUTE, GAIN0, GAIN1, MSTR/ $\overline{\text{SLV}}$ , SYNC |     | 0.8 | V    |

## RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                            | TEST CONDITIONS                                                                 | MIN        | MAX | UNIT               |
|--------------------------------------|---------------------------------------------------------------------------------|------------|-----|--------------------|
| $I_{IH}$ High-level input current    | SHUTDOWN, $V_I = V_{CC}$ , $V_{CC} = 24\text{ V}$                               |            | 125 | $\mu\text{A}$      |
|                                      | MUTE, $V_I = V_{CC}$ , $V_{CC} = 24\text{ V}$                                   |            | 75  |                    |
|                                      | GAIN0, GAIN1, MSTR/SLV, SYNC, $V_I = V_{REG}$ , $V_{CC} = 24\text{ V}$          |            | 2   |                    |
| $I_{IL}$ Low-level input current     | SHUTDOWN, $V_I = 0$ , $V_{CC} = 24\text{ V}$                                    |            | 2   | $\mu\text{A}$      |
|                                      | SYNC, MUTE, GAIN0, GAIN1, MSTR/SLV, $V_I = 0\text{ V}$ , $V_{CC} = 24\text{ V}$ |            | 1   |                    |
| $V_{OH}$ High-level output voltage   | FAULT, $I_{OH} = 1\text{ mA}$                                                   | VREG - 0.6 |     | V                  |
| $V_{OL}$ Low-level output voltage    | FAULT, $I_{OL} = -1\text{ mA}$                                                  | AGND + 0.4 |     | V                  |
| $f_{OSC}$ Oscillator frequency       | $R_{OSC}$ Resistor = 100 k $\Omega$ , MSTR/SLV = 2 V                            | 200        | 300 | kHz                |
| $T_A$ Operating free-air temperature |                                                                                 | -40        | 85  | $^{\circ}\text{C}$ |

## DC CHARACTERISTICS

 $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = 24\text{ V}$ ,  $R_L = 8\text{ }\Omega$  (unless otherwise noted)

| PARAMETER             |                                                         | TEST CONDITIONS                                                         |               | MIN  | TYP  | MAX  | UNIT |
|-----------------------|---------------------------------------------------------|-------------------------------------------------------------------------|---------------|------|------|------|------|
| V <sub>OS</sub>       | Class-D output offset voltage (measured differentially) | V <sub>I</sub> = 0 V, Gain = 36 dB                                      |               |      | 5    | 50   | mV   |
|                       | Bypass reference for input amplifier                    | VBYP, no load                                                           |               | 1.1  | 1.25 | 1.45 | V    |
|                       | 4-V internal supply voltage                             | VREG, no load, V <sub>CC</sub> = 10 V to 26 V                           |               | 3.75 | 4    | 4.25 | V    |
| PSRR                  | DC Power supply rejection ratio                         | V <sub>CC</sub> = 12 V to 24 V, inputs ac coupled to AGND, Gain = 36 dB |               |      | -70  |      | dB   |
| I <sub>CC</sub>       | Quiescent supply current                                | SHUTDOWN = 2 V, MUTE = 0 V, no load, filter or snubber                  |               |      | 22   | 26.5 | mA   |
| I <sub>CC(SD)</sub>   | Quiescent supply current in shutdown mode               | SHUTDOWN = 0.8 V, no load, filter or snubber                            |               |      | 300  | 400  | μA   |
| I <sub>CC(MUTE)</sub> | Quiescent supply current in mute mode                   | MUTE = 2 V, no load, filter or snubber                                  |               |      | 8    | 10   | mA   |
| r <sub>DS(on)</sub>   | Drain-source on-state resistance                        | V <sub>CC</sub> = 12 V, I <sub>O</sub> = 500 mA, T <sub>J</sub> = 25°C  | High Side     | 370  |      | mΩ   |      |
|                       |                                                         |                                                                         | Low side      | 370  |      |      |      |
|                       |                                                         |                                                                         | Total         | 780  | 950  |      |      |
| G                     | Gain                                                    | GAIN1 = 0.8 V                                                           | GAIN0 = 0.8 V | 19   | 20   | 21   | dB   |
|                       |                                                         |                                                                         | GAIN0 = 2 V   | 25   | 26   | 27   |      |
|                       |                                                         | GAIN1 = 2 V                                                             | GAIN0 = 0.8 V | 31   | 32   | 33   | dB   |
|                       |                                                         |                                                                         | GAIN0 = 2 V   | 35   | 36   | 37   |      |
|                       | Gain matching                                           | Between channels                                                        |               |      | 2%   |      |      |
| t <sub>ON</sub>       | Turn-on time                                            | C <sub>(VBYP)</sub> = 1 μF, SHUTDOWN = 2 V                              |               |      | 25   |      | ms   |
| t <sub>OFF</sub>      | Turn-off time                                           | C <sub>(VBYP)</sub> = 1 μF, SHUTDOWN = 0.8 V                            |               |      | 0.1  |      | ms   |

## DC CHARACTERISTICS

 $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $R_L = 8\text{ }\Omega$  (unless otherwise noted)

| PARAMETER                                                          | TEST CONDITIONS                                                         | MIN  | TYP  | MAX  | UNIT          |
|--------------------------------------------------------------------|-------------------------------------------------------------------------|------|------|------|---------------|
| $ V_{OS} $ Class-D output offset voltage (measured differentially) | $V_I = 0\text{ V}$ , Gain = 36 dB                                       |      | 5    | 50   | mV            |
| Bypass reference for input amplifier                               | VBYP, no load                                                           | 1.1  | 1.25 | 1.45 | V             |
| 4-V internal supply voltage                                        | VREG, no load                                                           | 3.75 | 4    | 4.25 | V             |
| PSRR DC Power supply rejection ratio                               | $V_{CC} = 12\text{ V}$ to 24 V, Inputs ac coupled to AGND, Gain = 36 dB |      | -70  |      | dB            |
| $I_{CC}$ Quiescent supply current                                  | SHUTDOWN = 2 V, MUTE = 0 V, no load, filter or snubber                  |      | 18   | 22.5 | mA            |
| $I_{CC(SD)}$ Quiescent supply current in shutdown mode             | SHUTDOWN = 0.8 V, no load, filter or snubber                            |      | 180  | 300  | $\mu\text{A}$ |
| $I_{CC(MUTE)}$ Quiescent supply current in mute mode               | MUTE = 2 V, no load, filter or snubber                                  |      | 7    | 9    | mA            |

**DC CHARACTERISTICS (continued)** $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $R_L = 8\ \Omega$  (unless otherwise noted)

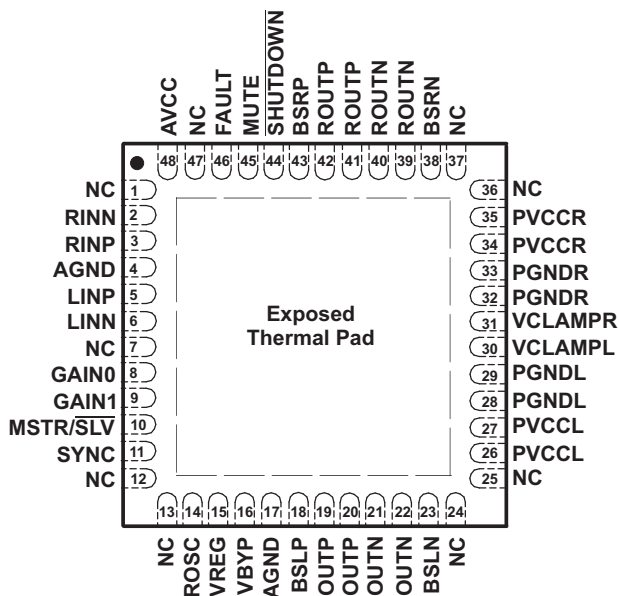
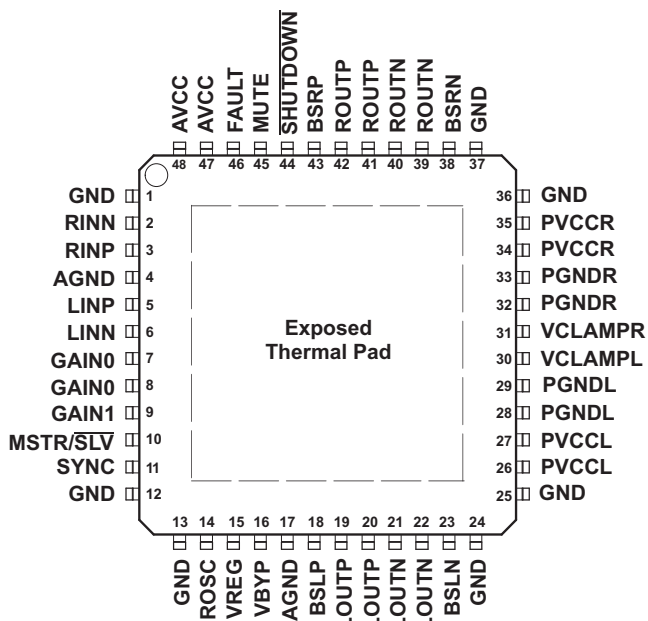
| PARAMETER    |                                  | TEST CONDITIONS                                                              |               | MIN | TYP | MAX | UNIT       |
|--------------|----------------------------------|------------------------------------------------------------------------------|---------------|-----|-----|-----|------------|
| $r_{DS(on)}$ | Drain-source on-state resistance | $V_{CC} = 12\text{ V}$ , $I_O = 500\text{ mA}$ ,<br>$T_J = 25^\circ\text{C}$ | High Side     |     | 370 |     | m $\Omega$ |
|              |                                  |                                                                              | Low side      |     | 370 |     |            |
|              |                                  |                                                                              | Total         |     | 780 | 950 |            |
| G            | Gain                             | GAIN1 = 0.8 V                                                                | GAIN0 = 0.8 V | 19  | 20  | 21  | dB         |
|              |                                  |                                                                              | GAIN0 = 2 V   | 25  | 26  | 27  |            |
|              |                                  | GAIN1 = 2 V                                                                  | GAIN0 = 0.8 V | 31  | 32  | 33  | dB         |
|              |                                  |                                                                              | GAIN0 = 2 V   | 35  | 36  | 37  |            |
| $t_{ON}$     | Turn-on time                     | $C_{(VBYP)} = 1\ \mu\text{F}$ , $\overline{\text{SHUTDOWN}} = 2\text{ V}$    |               |     | 25  |     | ms         |
| $t_{OFF}$    | Turn-off time                    | $C_{(VBYP)} = 1\ \mu\text{F}$ , $\overline{\text{SHUTDOWN}} = 0.8\text{ V}$  |               |     | 0.1 |     | ms         |

**AC CHARACTERISTICS** $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 24\text{ V}$ ,  $R_L = 8\ \Omega$  (unless otherwise noted)

| PARAMETER |                                   | TEST CONDITIONS                                                                          | MIN | TYP   | MAX | UNIT             |
|-----------|-----------------------------------|------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| $K_{SVR}$ | Supply ripple rejection           | 200 mV <sub>PP</sub> ripple from 20 Hz–1 kHz,<br>Gain = 20 dB, Inputs ac-coupled to AGND |     | –70   |     | dB               |
| $P_O$     | Continuous output power           | THD+N = 0.09%, $f = 1\text{ kHz}$ (thermally limited)                                    |     | 10    |     | W                |
| THD+N     | Total harmonic distortion + noise | $f = 1\text{ kHz}$ , $P_O = 5\text{ W}$ (half-power)                                     |     | 0.09% |     |                  |
| $V_n$     | Output integrated noise           | 20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB                                         |     | 100   |     | $\mu\text{V}$    |
|           |                                   |                                                                                          |     | –80   |     | dBV              |
|           | Crosstalk                         | $V_O = 1\text{ V}_{rms}$ , Gain = 20 dB, $f = 1\text{ kHz}$                              |     | –92   |     | dB               |
| SNR       | Signal-to-noise ratio             | Maximum output at THD+N < 1%, $f = 1\text{ kHz}$ ,<br>Gain = 20 dB, A-weighted           |     | 102   |     | dB               |
|           | Thermal trip point                |                                                                                          |     | 150   |     | $^\circ\text{C}$ |
|           | Thermal hysteresis                |                                                                                          |     | 30    |     | $^\circ\text{C}$ |

**AC CHARACTERISTICS** $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $R_L = 8\ \Omega$  (unless otherwise noted)

| PARAMETER |                                   | TEST CONDITIONS                                                                          | MIN | TYP   | MAX | UNIT             |
|-----------|-----------------------------------|------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| $K_{SVR}$ | Supply ripple rejection           | 200 mV <sub>PP</sub> ripple from 20 Hz–1 kHz,<br>Gain = 20 dB, Inputs ac-coupled to AGND |     | –70   |     | dB               |
| $P_O$     | Continuous output power           | THD+N = 7%, $f = 1\text{ kHz}$                                                           |     | 8.7   |     | W                |
|           |                                   | THD+N = 10%, $f = 1\text{ kHz}$                                                          |     | 9.2   |     |                  |
|           |                                   | THD+N = 10%, $f = 1\text{ kHz}$ , $V_{CC} = 13\text{ V}$                                 |     | 10    |     |                  |
|           |                                   | THD+N = 0.26%, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ (thermally limited)                |     | 10    |     |                  |
| THD+N     | Total harmonic distortion + noise | $R_L = 8\ \Omega$ , $f = 1\text{ kHz}$ , $P_O = 4.5\text{ W}$ (half-power)               |     | 0.08% |     |                  |
|           |                                   | $R_L = 4\ \Omega$ , $f = 1\text{ kHz}$ , $P_O = 5\text{ W}$ (half-power)                 |     | 0.11% |     |                  |
| $V_n$     | Output integrated noise           | 20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB                                         |     | 100   |     | $\mu\text{V}$    |
|           |                                   |                                                                                          |     | –80   |     | dBV              |
|           | Crosstalk                         | $P_O = 1\text{ W}$ , Gain = 20 dB, $f = 1\text{ kHz}$                                    |     | –94   |     | dB               |
| SNR       | Signal-to-noise ratio             | Maximum output at THD+N < 1%, $f = 1\text{ kHz}$ ,<br>Gain = 20 dB, A-weighted           |     | 98    |     | dB               |
|           | Thermal trip point                |                                                                                          |     | 150   |     | $^\circ\text{C}$ |
|           | Thermal hysteresis                |                                                                                          |     | 30    |     | $^\circ\text{C}$ |

**48 PIN, QFN PACKAGE  
(TOP VIEW)**

**48 PIN, HTQFP PACKAGE  
(TOP VIEW)**


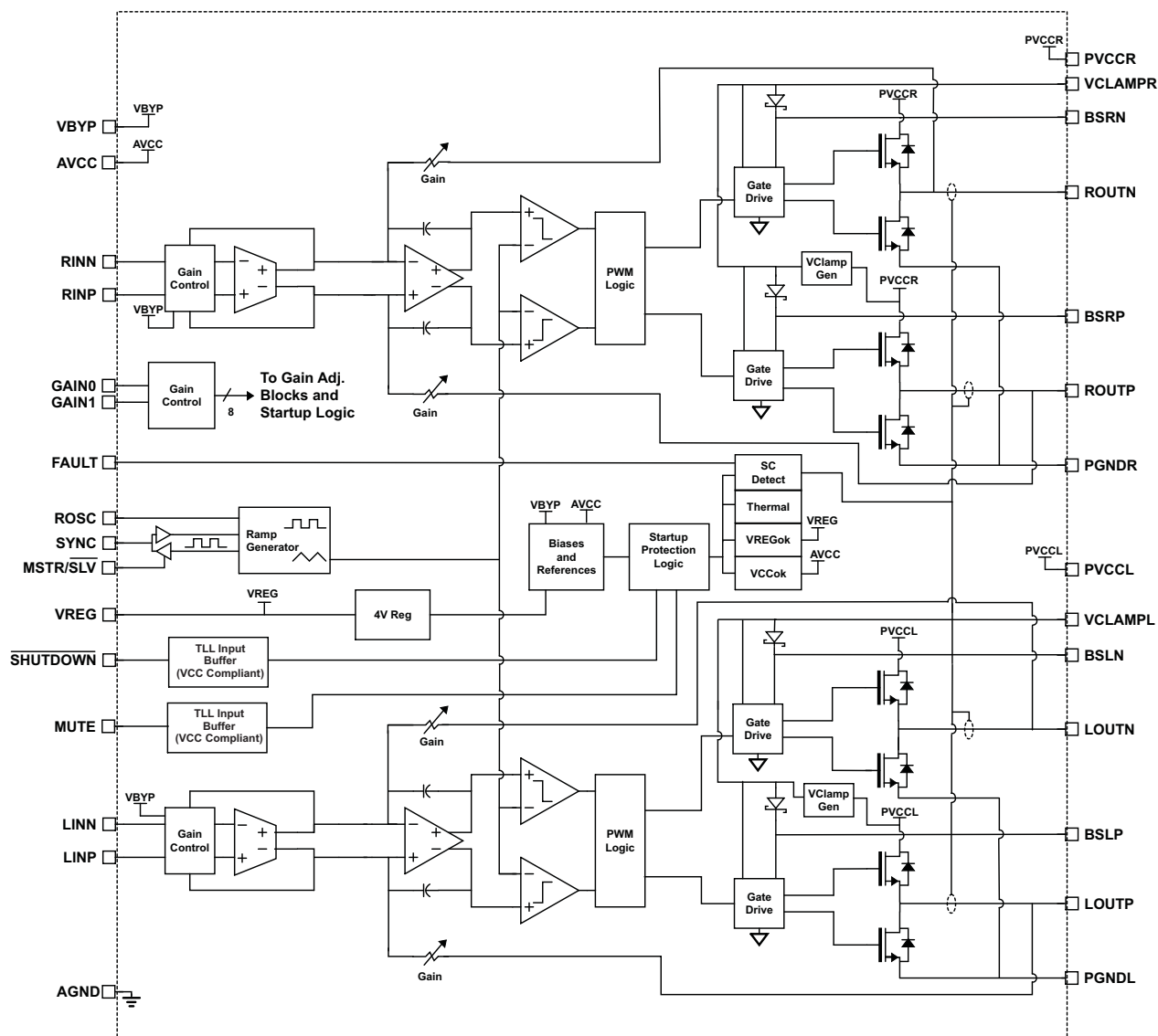
### TERMINAL FUNCTIONS

| TERMINAL |         |                           | I/O | DESCRIPTION                                                                                                                                             |
|----------|---------|---------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | QFN NO. | HTQFP NO.                 |     |                                                                                                                                                         |
| SHUTDOWN | 44      | 44                        | I   | Shutdown signal for IC (LOW = disabled, HIGH = operational). TTL logic levels with compliance to AVCC.                                                  |
| RINN     | 2       | 2                         | I   | Negative audio input for right channel. Biased at VREG/2.                                                                                               |
| RINP     | 3       | 3                         | I   | Positive audio input for right channel. Biased at VREG/2.                                                                                               |
| LINN     | 6       | 6                         | I   | Negative audio input for left channel. Biased at VREG/2.                                                                                                |
| LINP     | 5       | 5                         | I   | Positive audio input for left channel. Biased at VREG/2.                                                                                                |
| GAIN0    | 8       | 7, 8                      | I   | Gain select least significant bit. TTL logic levels with compliance to VREG.                                                                            |
| GAIN1    | 9       | 9                         | I   | Gain select most significant bit. TTL logic levels with compliance to VREG.                                                                             |
| GND      |         | 1, 12, 13, 24, 25, 36, 37 |     | Connect to the thermal pad.                                                                                                                             |
| MUTE     | 45      | 45                        | I   | Mute signal for quick disable/enable of outputs (HIGH = outputs high-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.               |
| FAULT    | 46      | 46                        | O   | TTL compatible output. HIGH = short-circuit fault. LOW = no fault. Only reports short-circuit faults. Thermal faults are not reported on this terminal. |
| BSLP     | 18      | 18                        | I/O | Bootstrap I/O for left channel, positive high-side FET.                                                                                                 |
| PVCCCL   | 26, 27  | 26, 27                    |     | Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.                                                                      |
| LOUPT    | 19, 20  | 19, 20                    | O   | Class-D 1/2-H-bridge positive output for left channel.                                                                                                  |
| PGNDL    | 28, 29  | 28, 29                    |     | Power ground for left channel H-bridge.                                                                                                                 |
| LOUTN    | 21, 22  | 21, 22                    | O   | Class-D 1/2-H-bridge negative output for left channel.                                                                                                  |
| BSLN     | 23      | 23                        | I/O | Bootstrap I/O for left channel, negative high-side FET.                                                                                                 |
| VCLAMPL  | 30      | 30                        |     | Internally generated voltage supply for left channel bootstrap capacitor.                                                                               |
| VCLAMPR  | 31      | 31                        |     | Internally generated voltage supply for right channel bootstrap capacitor.                                                                              |
| BSRN     | 38      | 38                        | I/O | Bootstrap I/O for right channel, negative high-side FET.                                                                                                |
| ROUTN    | 39, 40  | 39, 40                    | O   | Class-D 1/2-H-bridge negative output for right channel.                                                                                                 |
| PGNDR    | 32, 33  | 32, 33                    |     | Power ground for right channel H-bridge.                                                                                                                |

**TERMINAL FUNCTIONS (continued)**

| TERMINAL         |                                  |           | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                              |
|------------------|----------------------------------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME             | QFN NO.                          | HTQFP NO. |     |                                                                                                                                                                                                                                                                                                                                          |
| ROUTP            | 41, 42                           | 41, 42    | O   | Class-D 1/2-H-bridge positive output for right channel.                                                                                                                                                                                                                                                                                  |
| PVCCR            | 34, 35                           | 34, 35    |     | Power supply for right channel H-bridge, not connected to PVCCCL or AVCC.                                                                                                                                                                                                                                                                |
| BSRP             | 43                               | 43        | I/O | Bootstrap I/O for right channel, positive high-side FET.                                                                                                                                                                                                                                                                                 |
| AGND             | 4, 17                            | 4, 17     |     | Analog ground for digital/analog cells in core.                                                                                                                                                                                                                                                                                          |
| ROSC             | 14                               | 14        | I/O | I/O for current setting resistor of ramp generator.                                                                                                                                                                                                                                                                                      |
| MSTR/ <u>SLV</u> | 10                               | 10        | I   | Master/Slave select for determining direction of SYNC terminal. HIGH=Master mode, SYNC terminal is an output; LOW = slave mode, SYNC terminal accepts a clock input. TTL logic levels with compliance to VREG.                                                                                                                           |
| SYNC             | 11                               | 11        | I/O | Clock input/output for synchronizing multiple class-D devices. Direction determined by MSTR/SLV terminal. Input signal not to exceed VREG.                                                                                                                                                                                               |
| VBYP             | 16                               | 16        | O   | Reference for preamplifier. Nominally equal to 1.25 V. Also controls start-up time via external capacitor sizing.                                                                                                                                                                                                                        |
| VREG             | 15                               | 15        | O   | 4-V regulated output for use by internal cells, GAINx, MUTE, and MSTR/SLV pins only. Not specified for driving other external circuitry.                                                                                                                                                                                                 |
| AVCC             | 48                               | 47, 48    |     | High-voltage analog power supply. Not internally connected to PVCCR or PVCCCL.                                                                                                                                                                                                                                                           |
| NC               | 1, 7, 12, 13, 24, 25, 36, 37, 47 |           |     | Not internally connected.                                                                                                                                                                                                                                                                                                                |
| Thermal Pad      | -                                | -         | -   | Connect to AGND and PGND – should be star point for both grounds. Internal resistive connection to AGND and PGND. Thermal vias on the PCB should connect this pad to a large copper area on an internal or bottom layer for the best thermal performance. <i>The Thermal Pad must be soldered to the PCB for mechanical reliability.</i> |

## FUNCTIONAL BLOCK DIAGRAM

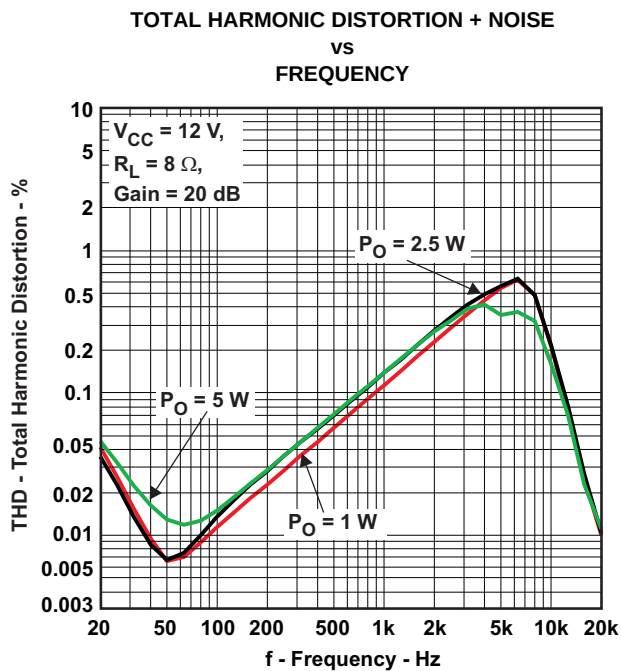


## TYPICAL CHARACTERISTICS

Table 1. TABLE OF GRAPHS<sup>(1)</sup>

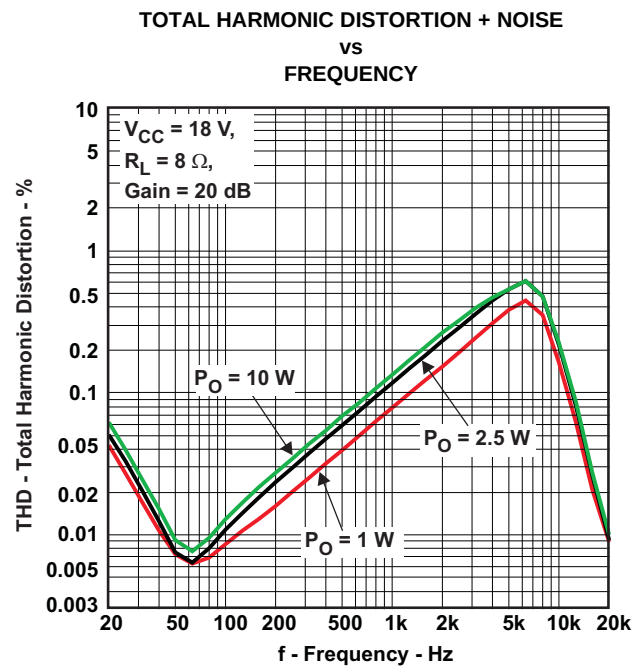
|                  |                                   |                       | FIGURE     |
|------------------|-----------------------------------|-----------------------|------------|
| THD+N            | Total harmonic distortion + noise | vs Frequency          | 1, 2, 3, 4 |
| THD+N            | Total harmonic distortion + noise | vs Output power       | 5, 6, 7, 8 |
|                  | Closed-loop response              | vs Frequency          | 9, 10      |
|                  | Output power                      | vs Supply voltage     | 11, 12     |
|                  | Efficiency                        | vs Output power       | 13, 14     |
| V <sub>CC</sub>  | Supply current                    | vs Total output power | 15, 16     |
|                  | Crosstalk                         | vs Frequency          | 17, 18     |
| k <sub>SVR</sub> | Supply ripple rejection ratio     | vs Frequency          | 19, 20     |

(1) All graphs were measured using the TPA3101D2 EVM.



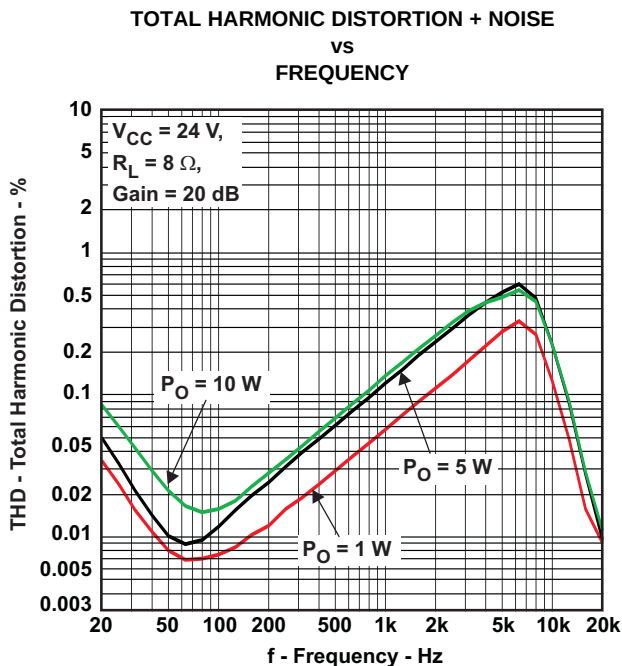
A. Power above 10 W may require increased heatsinking.

Figure 1.



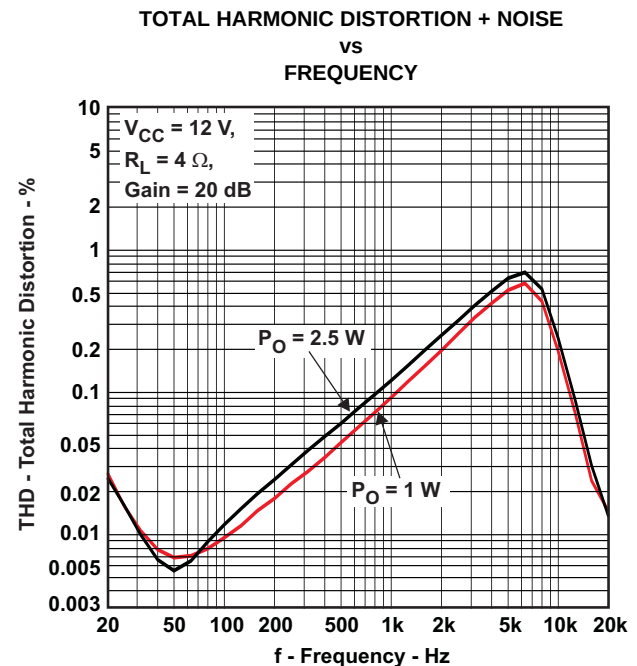
A. Power above 10 W may require increased heatsinking.

Figure 2.



A. Power above 10 W may require increased heatsinking.

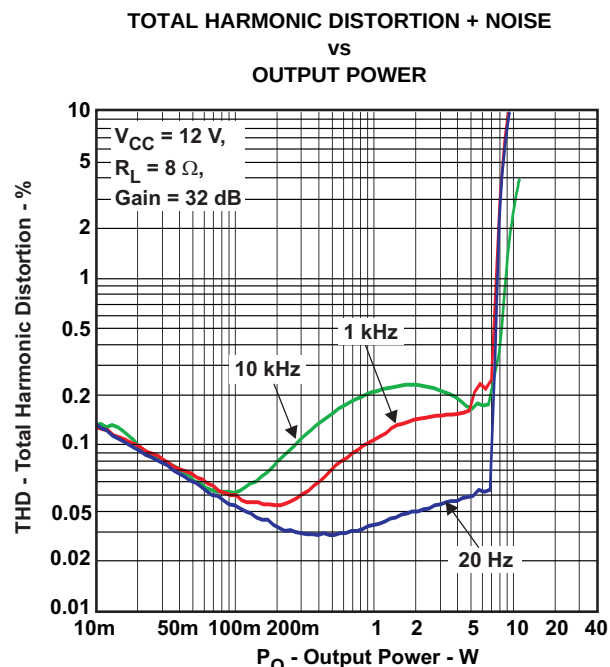
Figure 3.



A. Power above 10 W may require increased heatsinking.

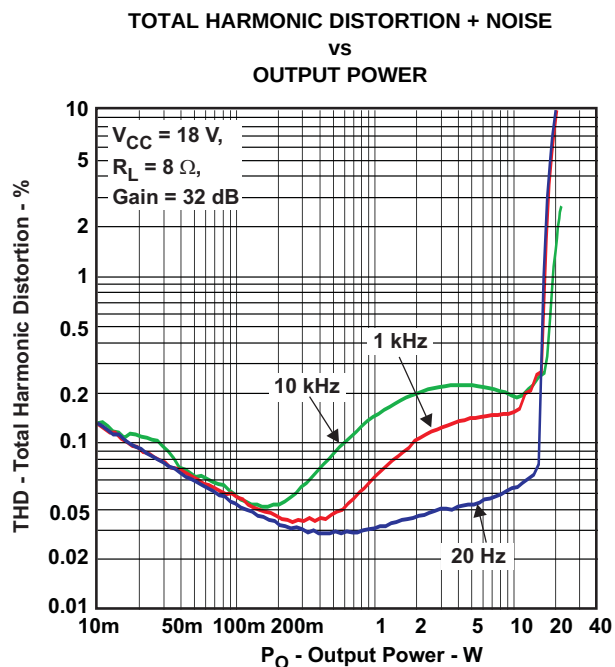
Figure 4.





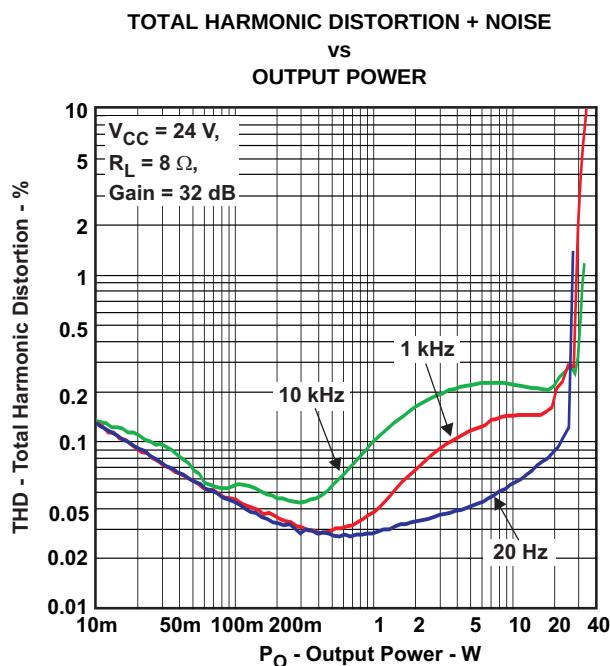
A. Power above 10 W may require increased heatsinking.

Figure 5.



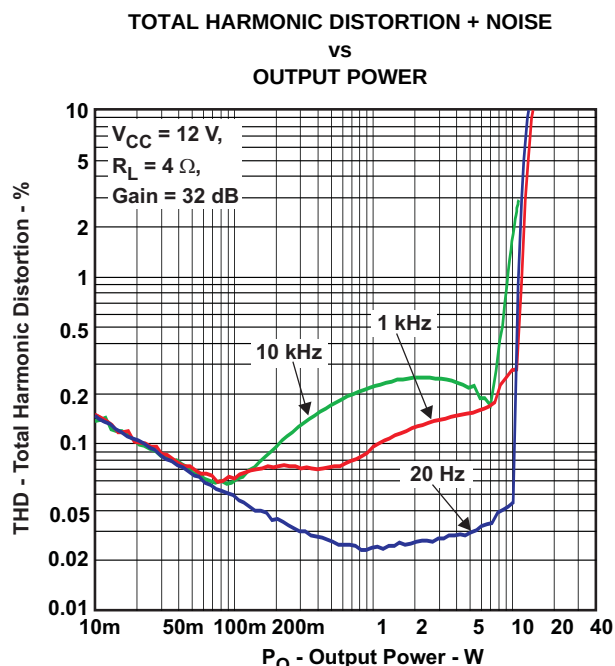
A. Power above 10 W may require increased heatsinking.

Figure 6.



A. Power above 10 W may require increased heatsinking.

Figure 7.



A. Power above 10 W may require increased heatsinking.

Figure 8.

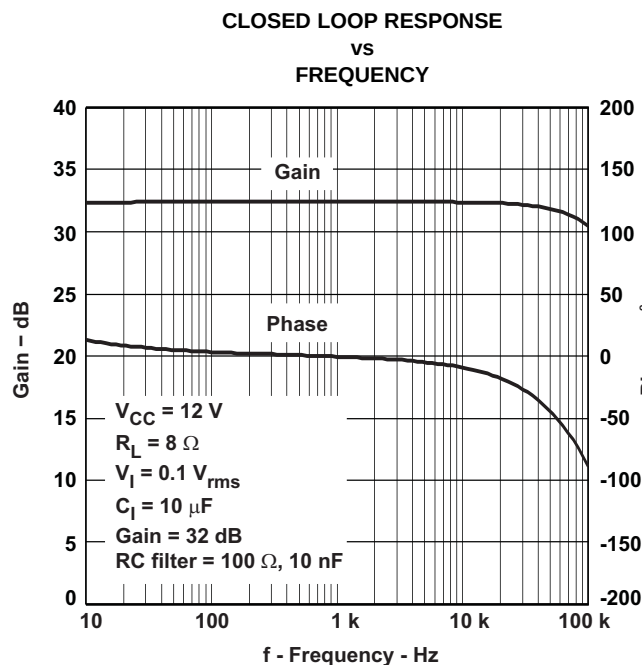


Figure 9.

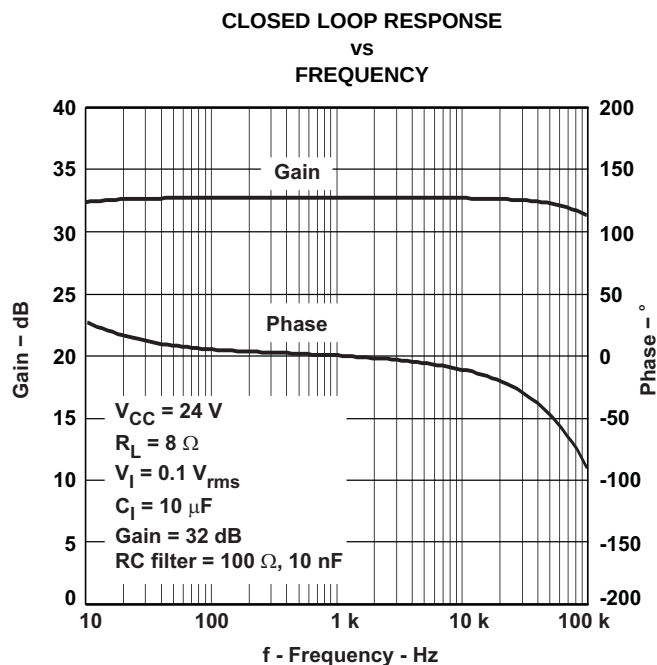


Figure 10.

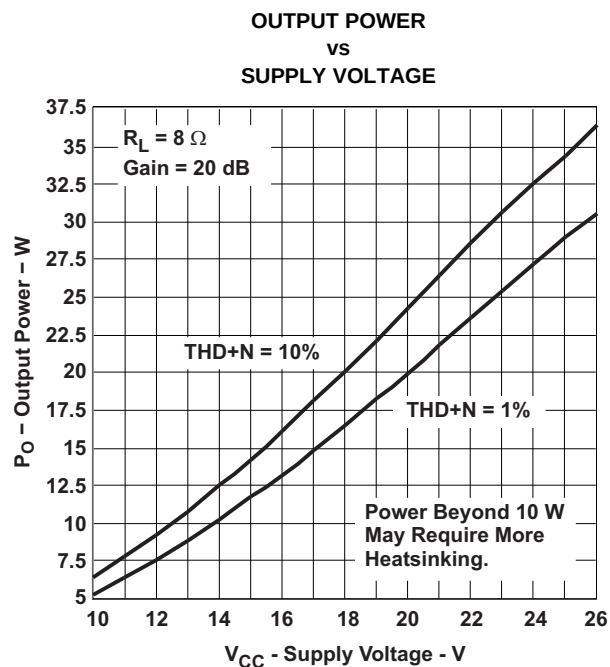


Figure 11.

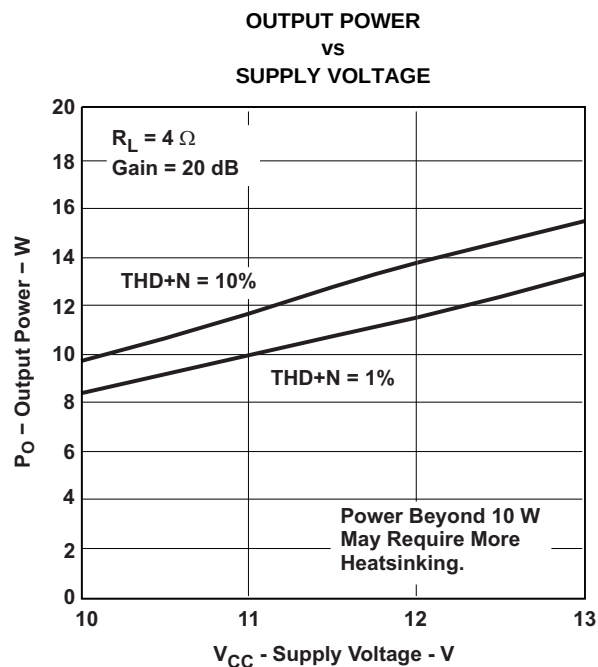


Figure 12.

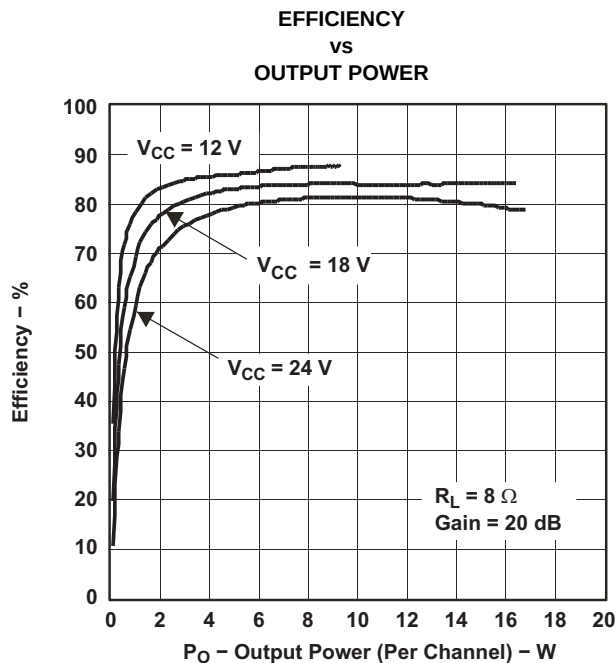


Figure 13.

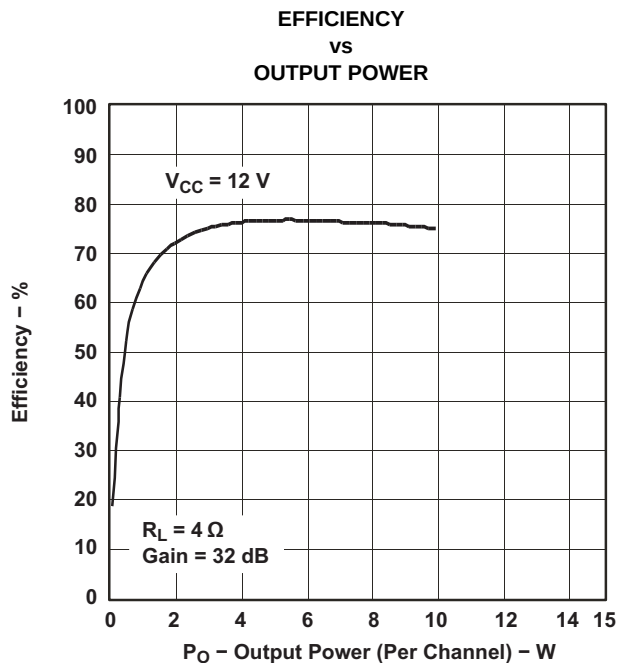


Figure 14.

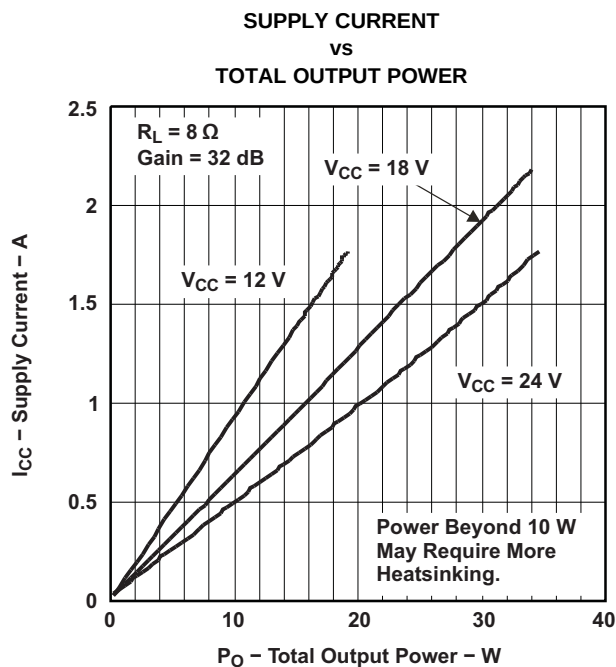


Figure 15.

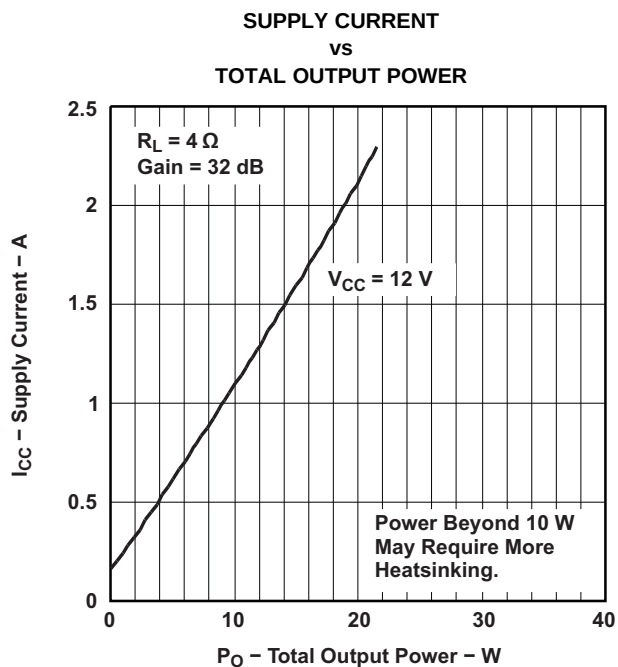


Figure 16.

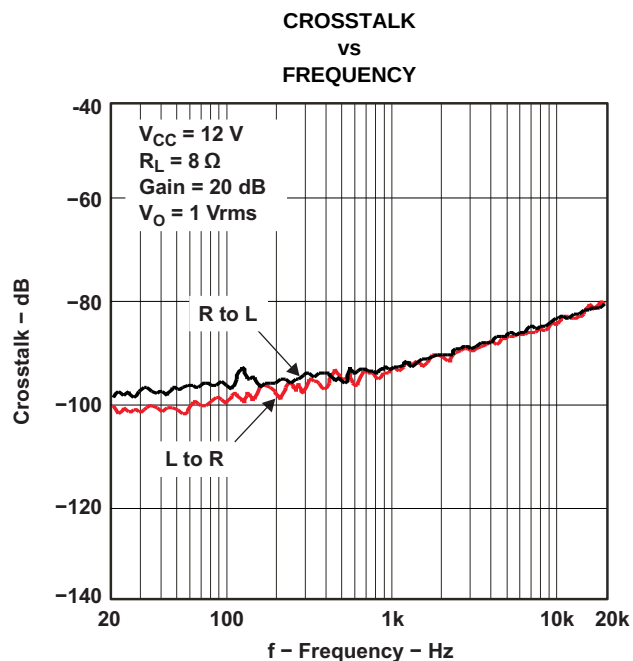


Figure 17.

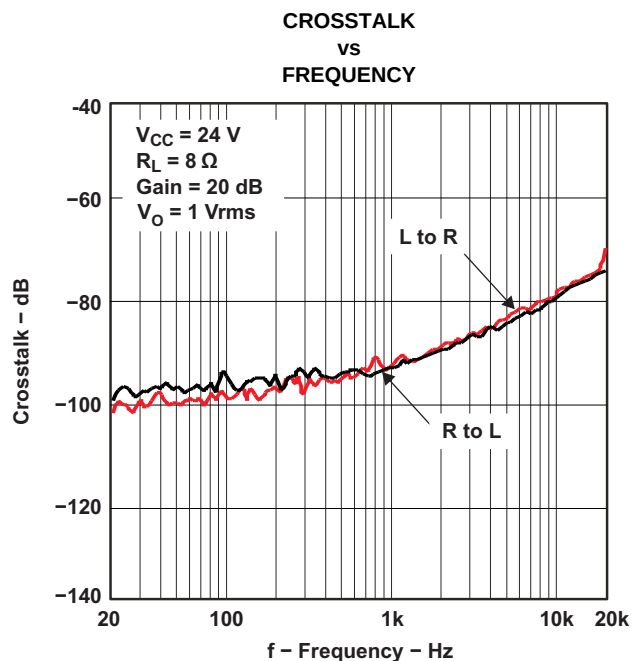


Figure 18.

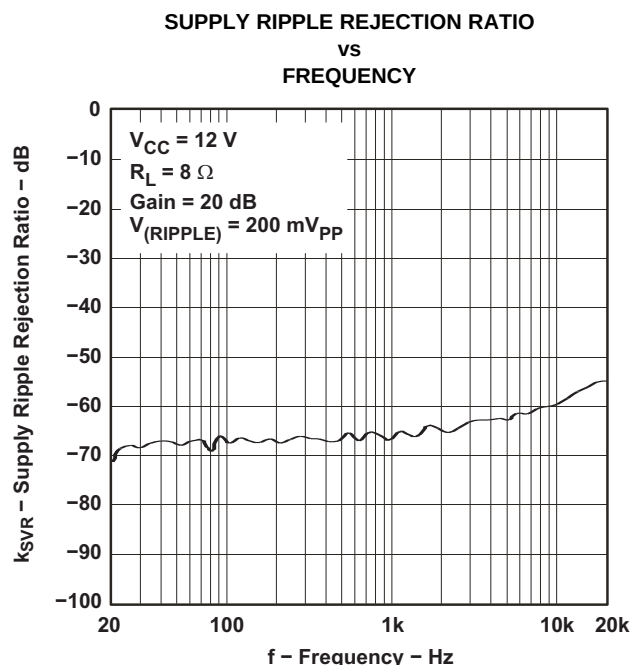


Figure 19.

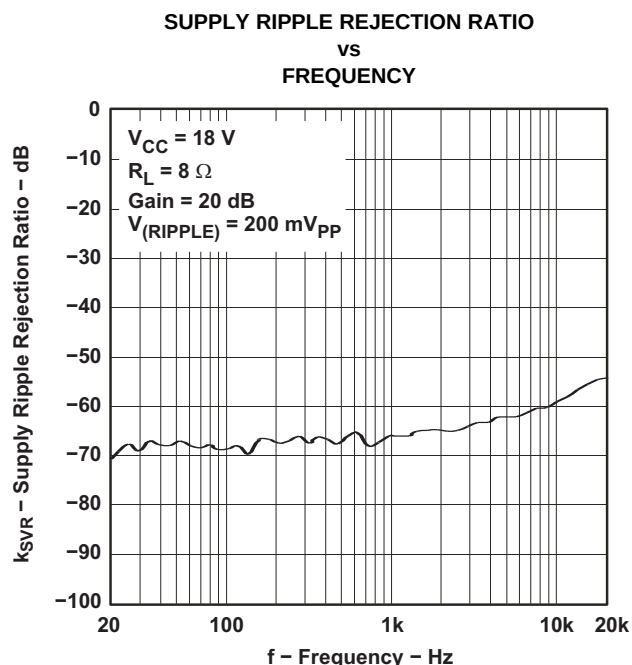


Figure 20.

## APPLICATION INFORMATION

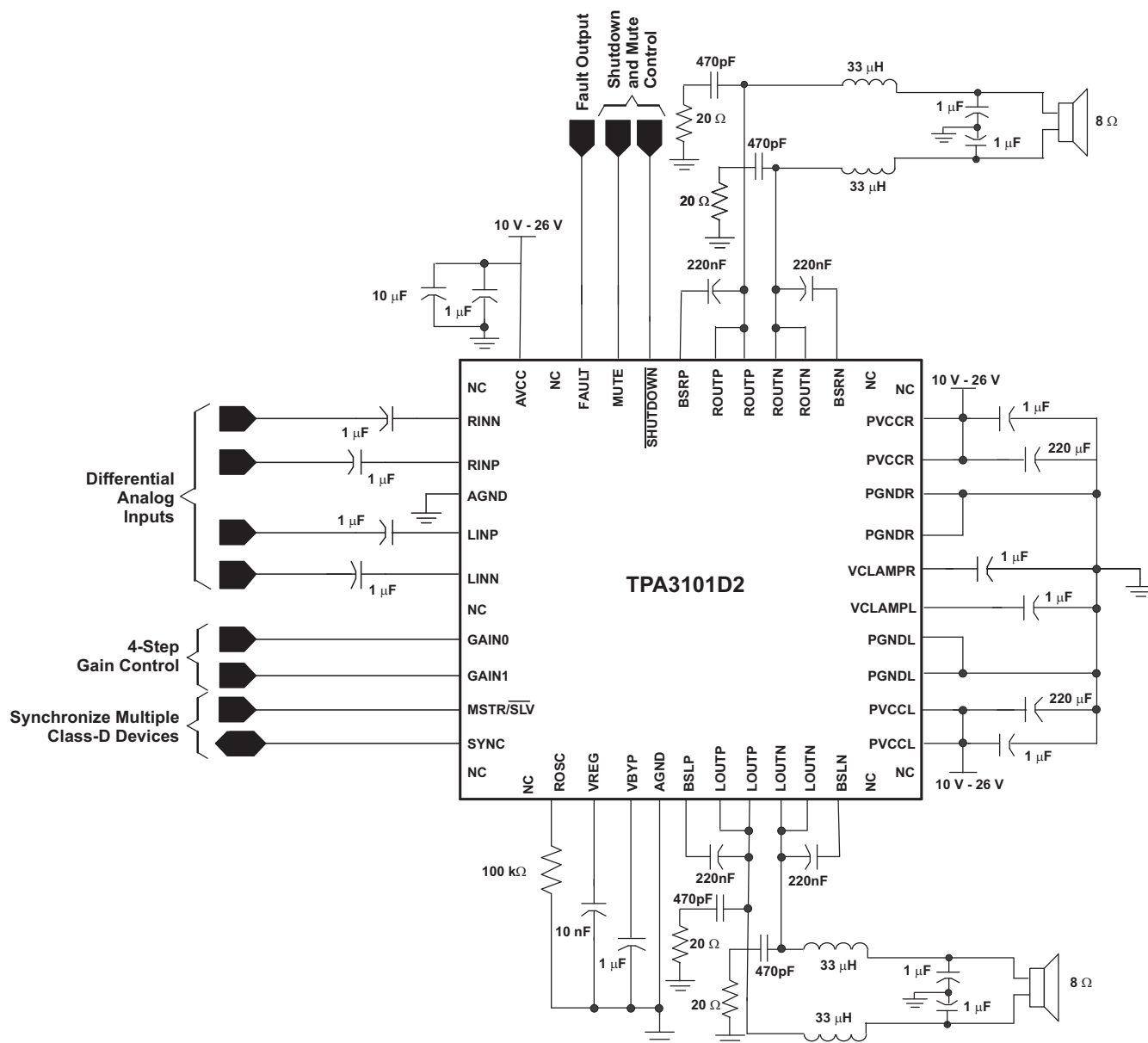


Figure 21. Stereo Class-D With Differential Inputs (QFN)

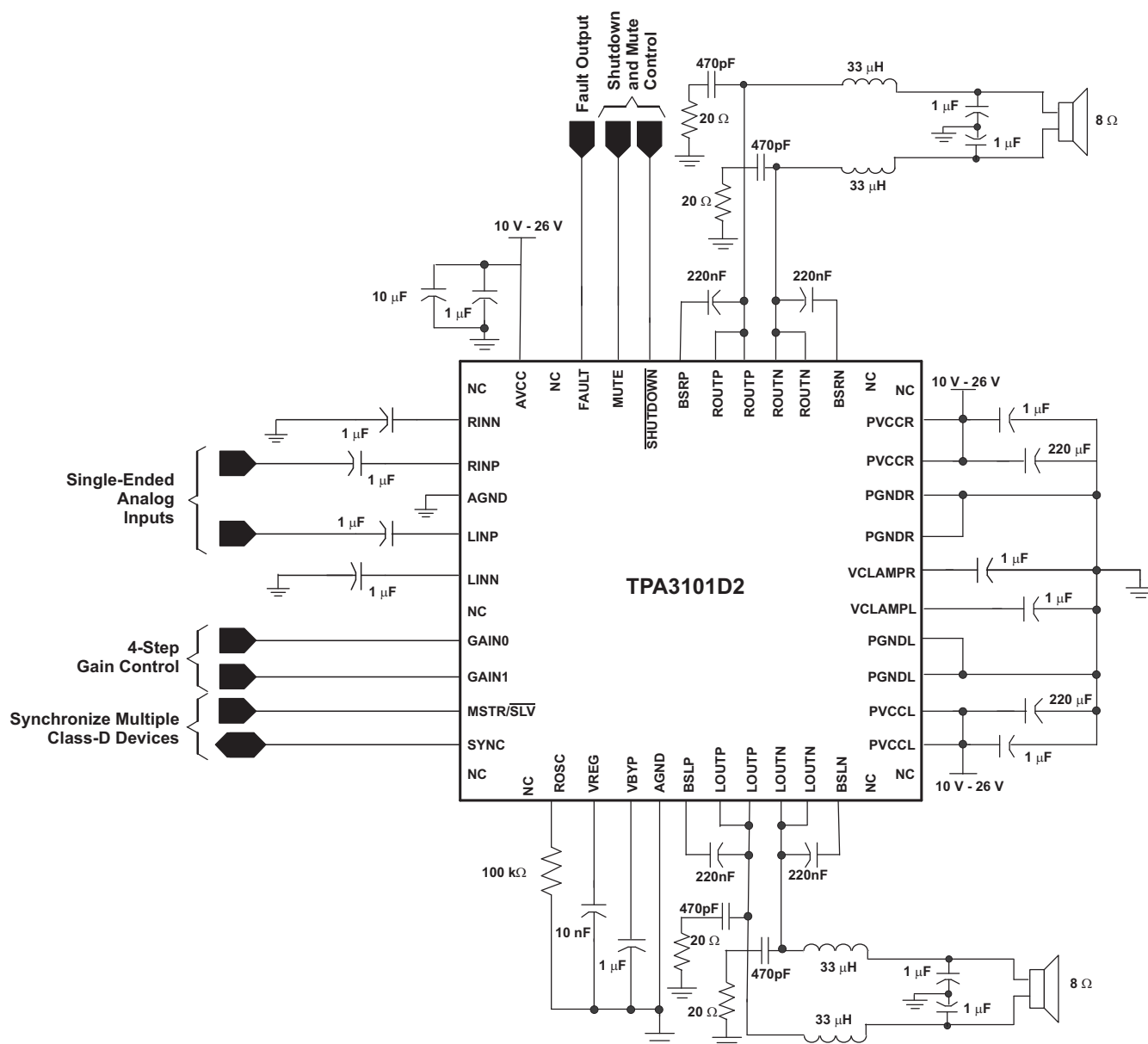


Figure 22. Stereo Class-D With Single-Ended Inputs (QFN)

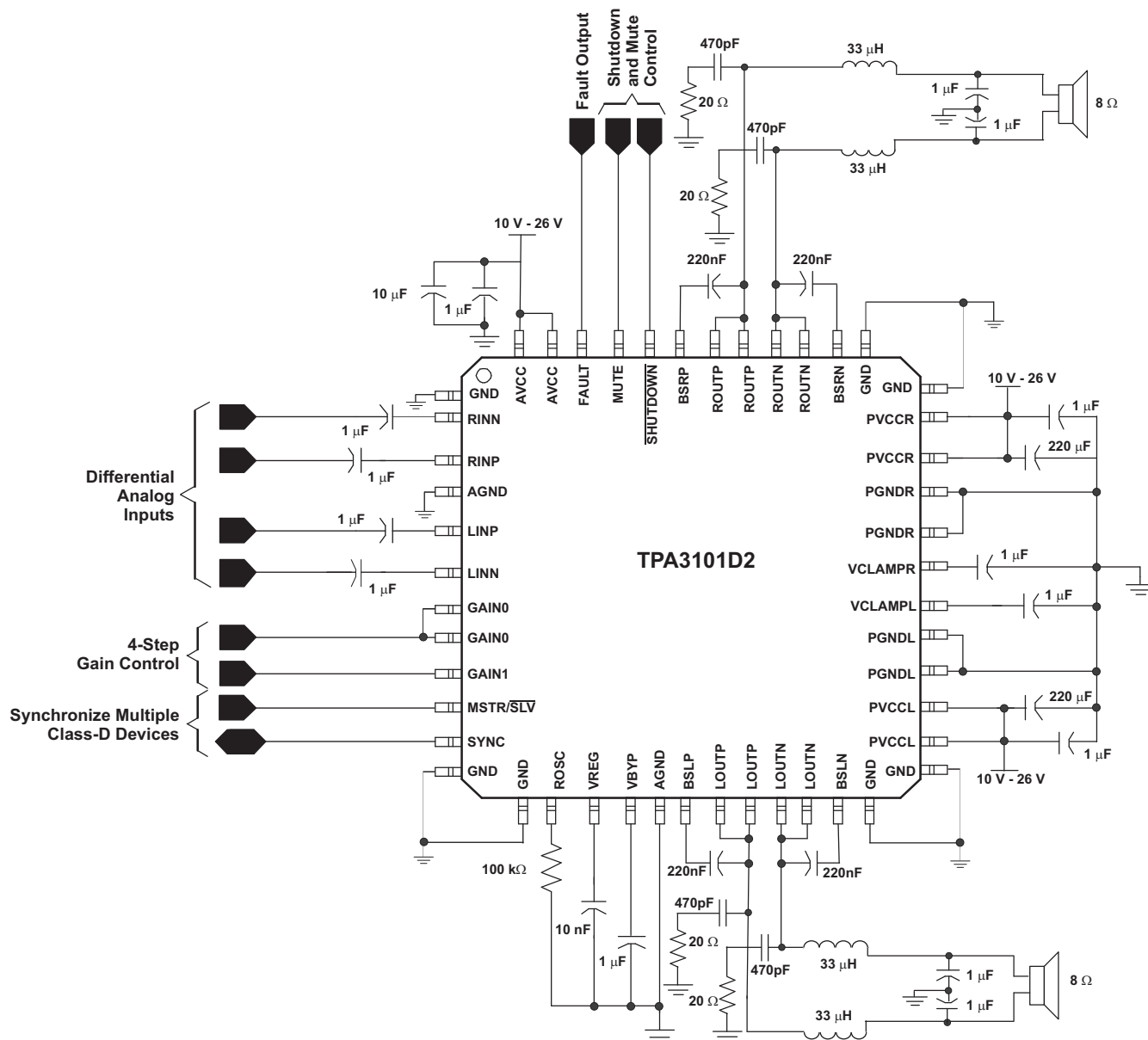


Figure 23. Stereo Class-D With Differential Inputs (HTQFP)

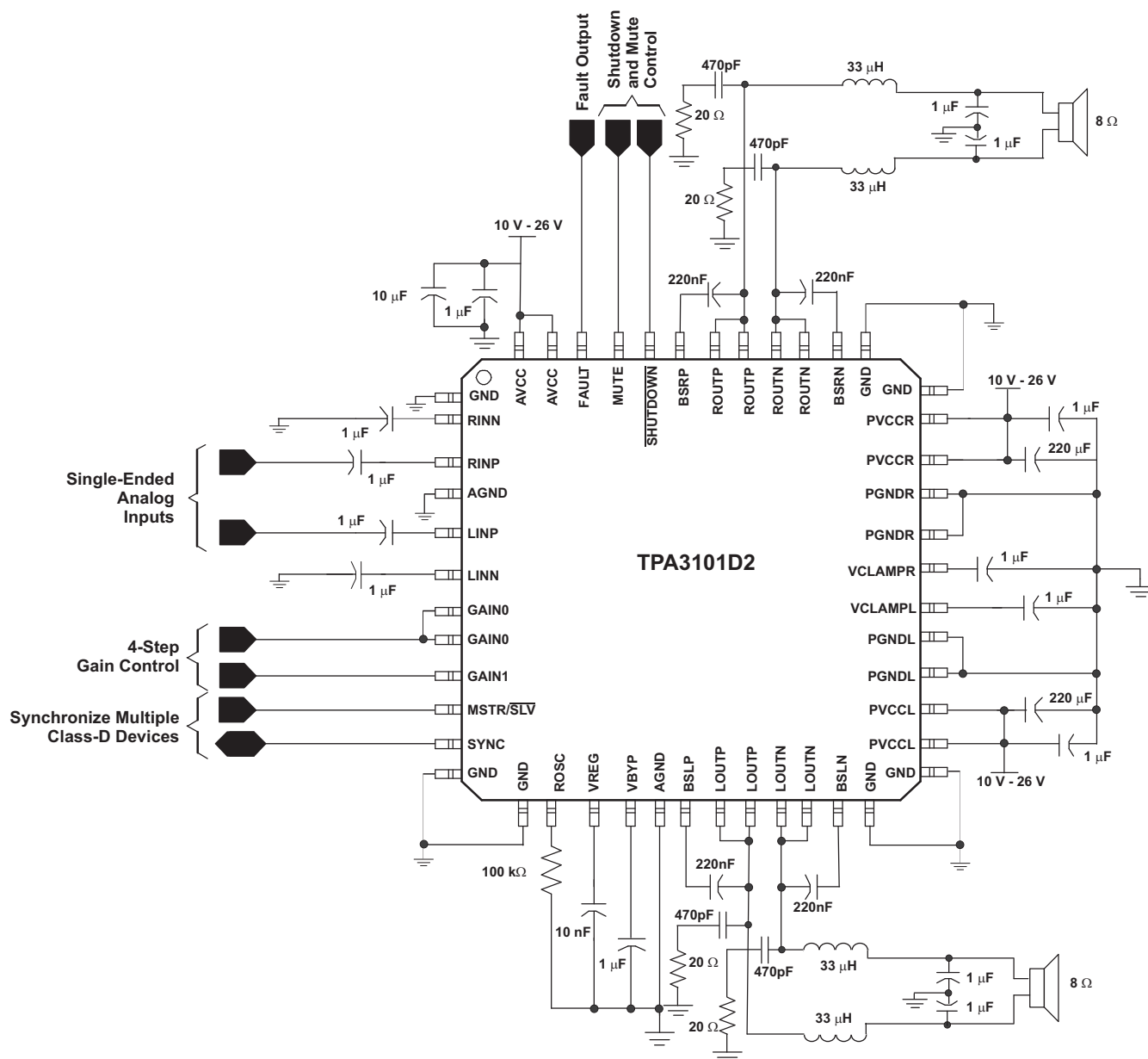


Figure 24. Stereo Class-D With Single-Ended Inputs (HTQFP)



## CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3101D2.

### Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage,  $V_{CC}$ . Therefore, the differential prefiltered output varies between positive and negative  $V_{CC}$ , where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 25. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss and thus causing a high supply current.

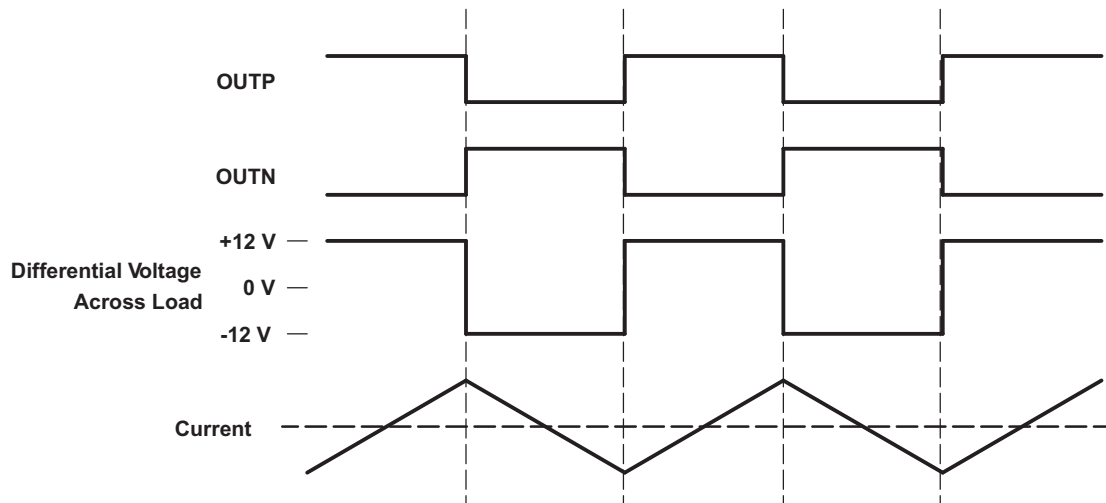
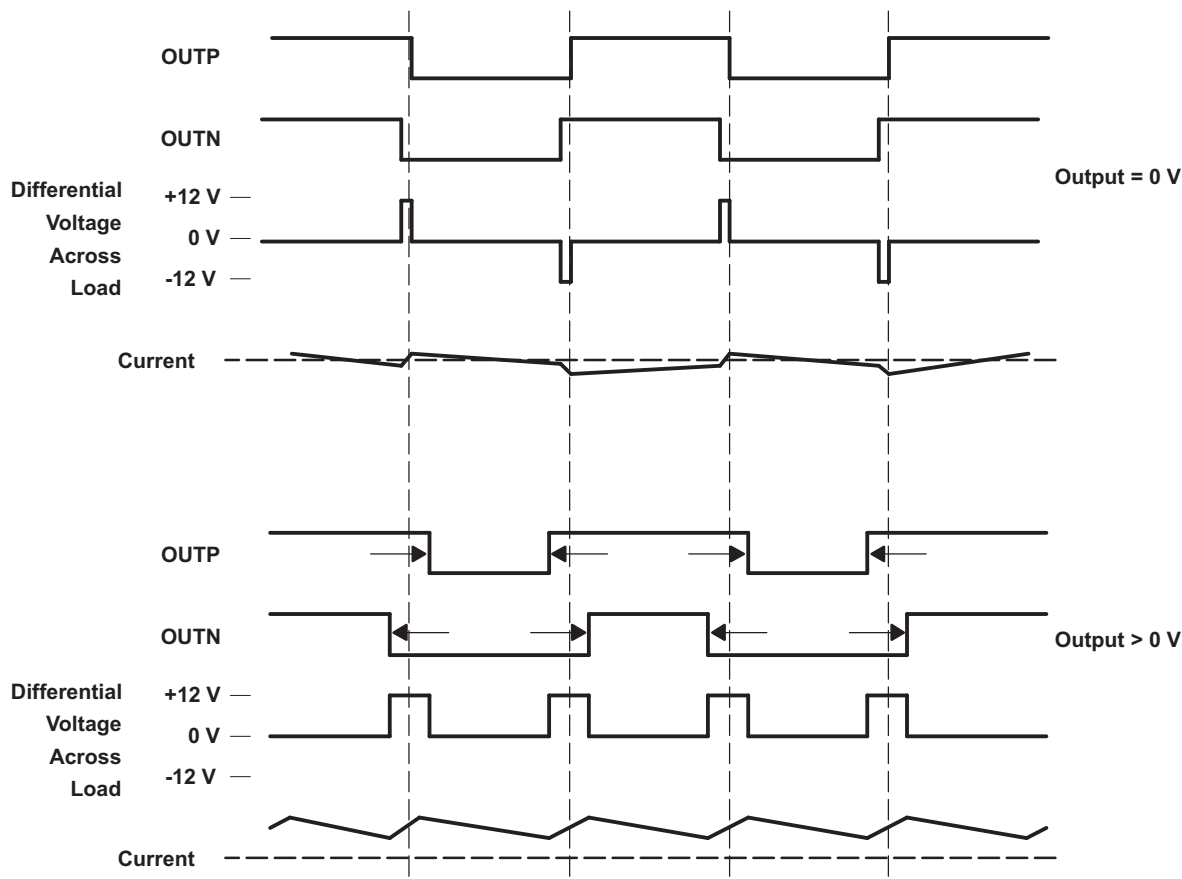


Figure 25. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms into an Inductive Load With No Input

### TPA3101D2 Modulation Scheme

The TPA3101D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any  $I^2R$  losses in the load.



**Figure 26. The TPA3101D2 Output Voltage and Current Waveforms Into an Inductive Load**

### Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is  $2 \times V_{CC}$ , and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3101D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is  $V_{CC}$  instead of  $2 \times V_{CC}$ . As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

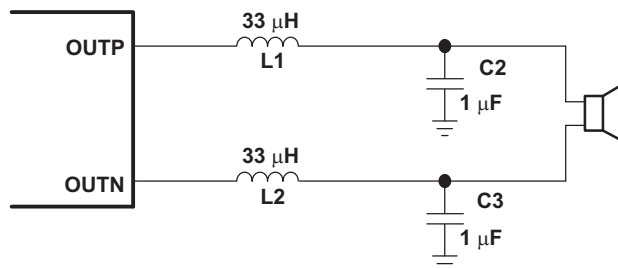
### When to Use an Output Filter for EMI Suppression

Design the TPA3101D2 without the filter if the traces from amplifier to speaker are short ( $< 10$  cm). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

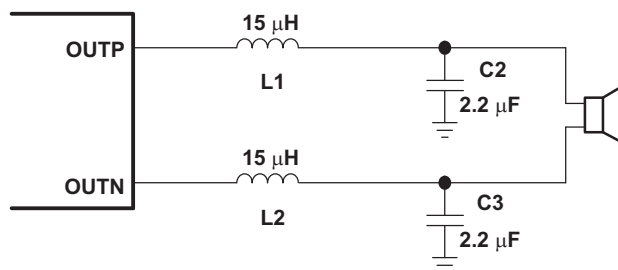
Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

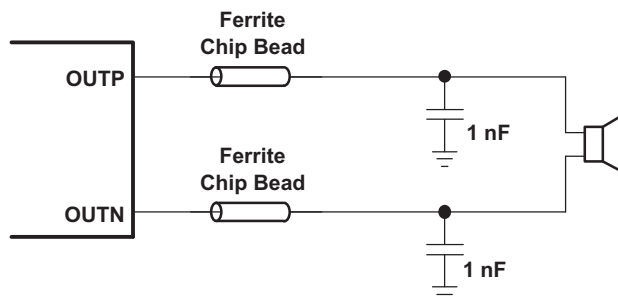
When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.



**Figure 27. Typical LC Output Filter, Cutoff Frequency of 28 kHz, Speaker Impedance = 8  $\Omega$**

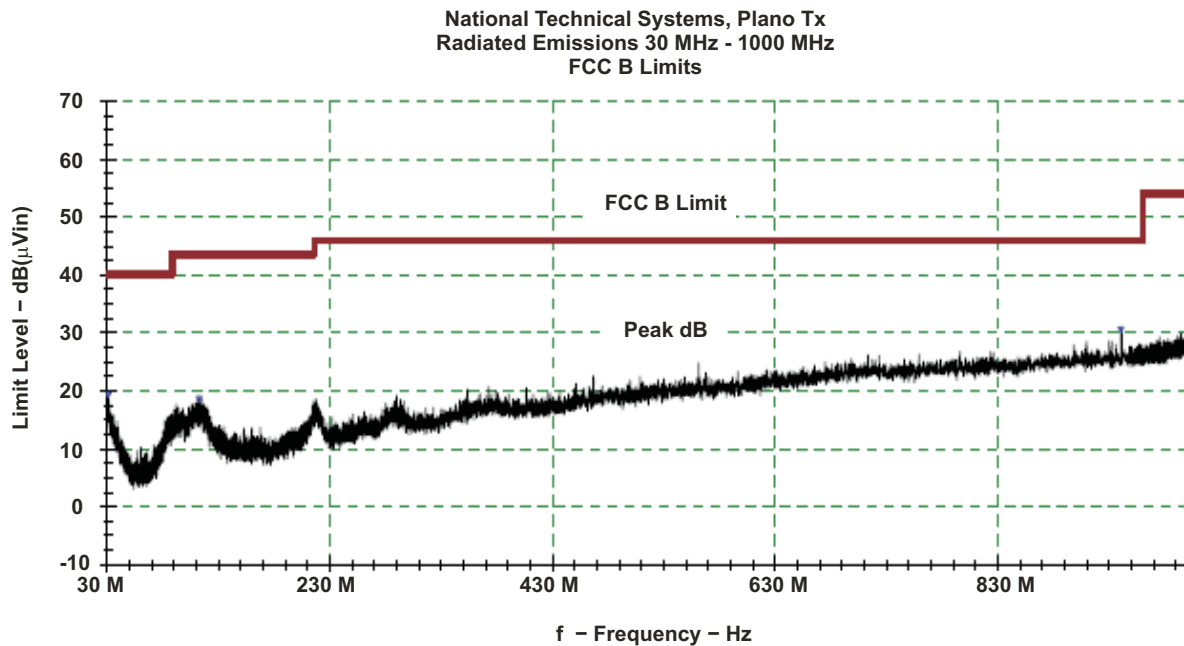


**Figure 28. Typical LC Output Filter, Cutoff Frequency of 28 kHz, Speaker Impedance = 4  $\Omega$**



**Figure 29. Typical Ferrite Chip Bead Filter (Chip Bead Example: Fair-Rite 2512067007Y3)**

Using the LC filter in [Figure 27](#), the TPA3101D2 EVM passed the FCC Part 15 Class B radiated emissions test with 21 inch speaker wires. Quasi-peak measurements were taken for the 4 standard test configurations, and the TPA3101D2 EVM passed with at least 14-dB margin. A plot of the peak measurement for the horizontal rear configuration is shown in [Figure 30](#).

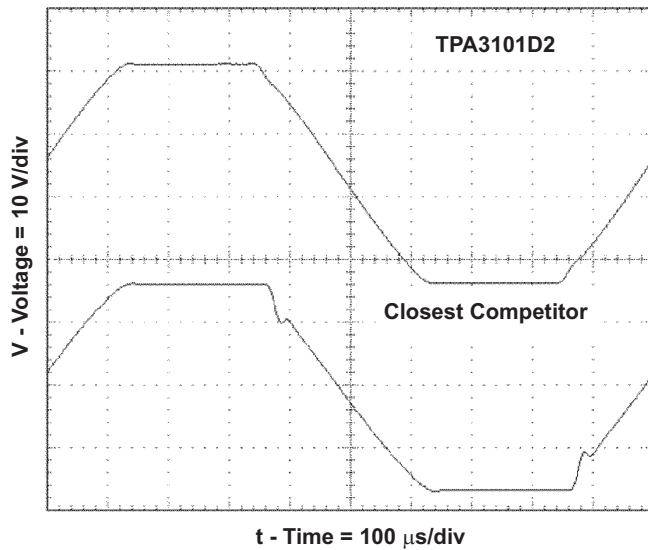


**Figure 30. Radiated Emissions Prescan 30 MHz - 1000 MHz**

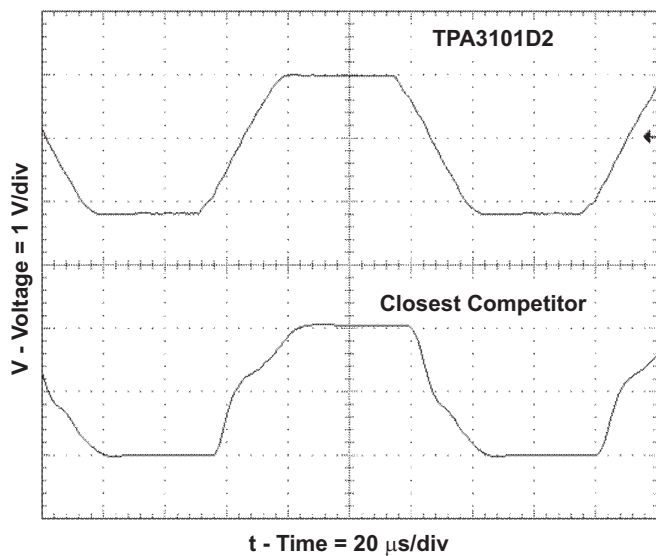
Inductors used in LC filters must be chosen carefully. A significant change in inductance at the peak output current of the TPA3101D2 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1  $\mu\text{H}$  per amp to avoid this. Also note that smaller inductors than 33  $\mu\text{H}$  may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power.

Capacitors used in LC filters must also be chosen carefully. A significant change in capacitance at the peak output voltage of the TPA3101D2 will cause increased distortion. LC filter capacitors should have DC-voltage ratings of at least twice the peak application voltage (the power supply voltage) and should be made of X5R or better material. In all cases, avoid using capacitors with loose temperature ratings like Y5V.

## Adaptive Dynamic Range Control



**Figure 31. 1-kHz Sine Output at 10% THD+N**



**Figure 32. 8-kHz Sine Output at 10% THD+N**

The Texas Instruments patent-pending adaptive dynamic range control (ADRC) technology removes the notch inherent in class-D audio power amplifiers when they come out of clipping. This effect is more severe at higher frequencies as shown in [Figure 32](#).

## Gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3101D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in [Table 2](#) are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance ( $Z_i$ ) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by  $\pm 20\%$  due to shifts in the actual resistance of the input resistors.

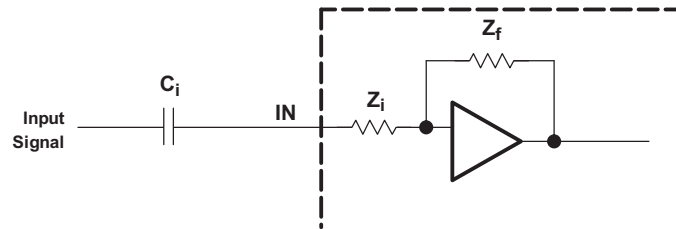
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 12.8 k $\Omega$ , which is the absolute minimum input impedance of the TPA3101D2. At the lower gain settings, the input impedance could increase as high as 38.4 k $\Omega$

**Table 2. Gain Setting**

| GAIN1 | GAIN0 | AMPLIFIER GAIN (dB) | INPUT IMPEDANCE (k $\Omega$ ) |
|-------|-------|---------------------|-------------------------------|
|       |       | TYP                 | TYP                           |
| 0     | 0     | 20                  | 32                            |
| 0     | 1     | 26                  | 16                            |
| 1     | 0     | 32                  | 16                            |
| 1     | 1     | 36                  | 16                            |

## INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 16 k $\Omega \pm 20\%$ , to the largest value, 32 k $\Omega \pm 20\%$ . As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

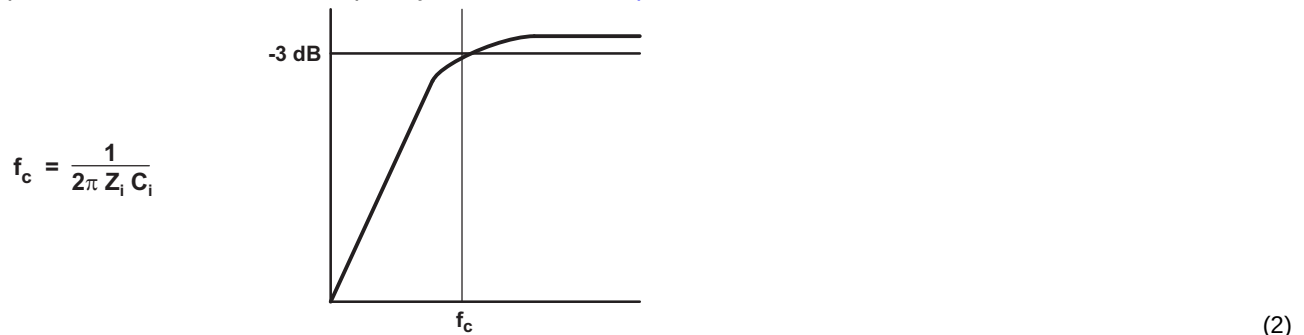


The -3-dB frequency can be calculated using [Equation 1](#). Use the  $Z_i$  values given in [Table 2](#).

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

### INPUT CAPACITOR, $C_i$

In the typical application, an input capacitor ( $C_i$ ) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_i$  and the input impedance of the amplifier ( $Z_i$ ) form a high-pass filter with the corner frequency determined in [Equation 2](#).



The value of  $C_i$  is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where  $Z_i$  is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. [Equation 2](#) is reconfigured as [Equation 3](#).

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (3)$$

In this example,  $C_i$  is 0.4 μF; so, one would likely choose a value of 0.47 μF as this value is commonly used. If the gain is known and is constant, use  $Z_i$  from [Table 2](#) to calculate  $C_i$ . A further consideration for this capacitor is the leakage path from the input source through the input network ( $C_i$ ) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

### Power Supply Decoupling, $C_s$

The TPA3101D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF to 1 μF placed as close as possible to the device  $V_{CC}$  lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220 μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 μF or larger capacitor should be placed on each PVCC terminal. A 10 μF capacitor on the AVCC terminal is adequate.

## IC Output Snubbers

In Figure 33, the 470-pF capacitors in series with 20-Ω resistors from the outputs of the TPA3101D2 IC to ground are switching snubbers. They linearize switching transitions and reduce overshoot and ringing. By doing so they improve THD+N at lower power levels and they improve EMC by 2 to 4 dB at middle frequencies. They increase quiescent current by 3 to 12 mA depending on power supply voltage.

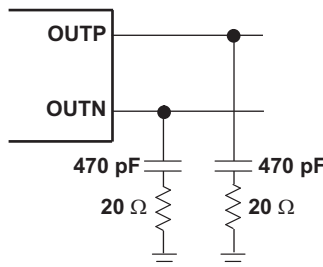


Figure 33. IC Output Snubbers

## BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220-nF capacitor must be connected from xOUTP to BSxx, and one 220-nF capacitor must be connected from xOUTN to BSxx. (See the application circuit diagram in Figure 21.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

## VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, two internal regulators clamp the gate voltage. Two 1-μF capacitors must be connected from VCLAMPL (pin 30) and VCLAMPR (pin 31) to ground and must be rated for at least 16 V. The voltages at the VCLAMP terminals may vary with  $V_{CC}$  and may not be used for powering any other circuitry.

## Internal Regulated 4-V Supply (VREG)

The VREG terminal (pin 15) is the output of an internally generated 4-V supply, used for the oscillator, preamplifier, and gain control circuitry. It requires a 10-nF capacitor, placed close to the pin, to keep the regulator stable.

This regulated voltage can be used to control GAIN0, GAIN1, MSTR/ $\overline{SLV}$ , and MUTE terminals, but should not be used to drive external circuitry.

## VBYP Capacitor Selection

The internal bias generator (VBYP) nominally provides a 1.25-V internal bias for the preamplifier stages. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the VBYP terminal is critical for achieving the best device performance. During power up or recovery from the shutdown state, the VBYP capacitor determines the rate at which the amplifier starts up. When the voltage on the VBYP capacitor equals VBYP, the device starts a 16.4-ms timer. When this timer completes, the outputs start switching. The charge rate of the capacitor is calculated using the standard charging formula for a capacitor,  $I = C \times dV/dT$ . The charge current is nominally equal to 250μA and dV is equal to VBYP. For example, a 1-μF capacitor on VBYP would take 5 ms to reach the value of VBYP and begin a 16.4-ms count before the outputs turn on. This equates to a turn-on time of <30 ms for a 1-μF capacitor on the VBYP terminal.

A secondary function of the VBYP capacitor is to filter high-frequency noise on the internal 1.25-V bias generator. A value of at least 0.47µF is recommended for the VBYP capacitor. For the best power-up and shutdown pop performance, the VBYP capacitor should be greater than or equal to the input capacitors.

### ROSC Resistor Selection

The resistor connected to the ROSC terminal controls the class-D output switching frequency using [Equation 4](#):

$$F_{osc} = \frac{1}{2 \times ROSC \times COSC} \quad (4)$$

COSC is an internal capacitor that is nominally equal to 20 pF. Variation over process and temperature can result in a ±15% change in this capacitor value.

For example, if ROSC is fixed at 100 kΩ, the frequency from device to device with this fixed resistance could vary from 217 kHz to 294 kHz with a 15% variation in the internal COSC capacitor. The tolerance of the ROSC resistor should also be considered to determine the range of expected switching frequencies from device to device. It is recommended that 1% tolerance resistors be used.

### Differential Input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3101D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3101D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance.

### SHUTDOWN OPERATION

The TPA3101D2 employs a shutdown mode of operation designed to reduce supply current ( $I_{CC}$ ) to the absolute minimum level during periods of nonuse for power conservation. The SHUTDOWN input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SHUTDOWN unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown or mute mode prior to removing the power supply voltage.

### MUTE Operation

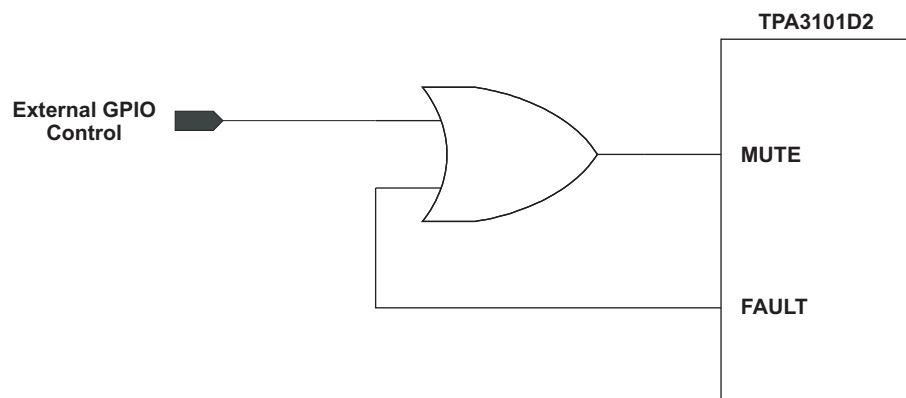
The MUTE pin is an input for controlling the output state of the TPA3101D2. A logic high on this terminal disables the outputs. A logic low on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources.

The MUTE terminal should never be left floating. For power conservation, the SHUTDOWN terminal should be used to reduce the quiescent current to the absolute minimum level.

The MUTE terminal can also be used with the FAULT output to automatically recover from a short-circuit event. When a short-circuit event occurs, the FAULT terminal transitions high indicating a short-circuit has been detected. When directly connected to MUTE, the MUTE terminal transitions high, and clears the internal fault flag. This causes the FAULT terminal to cycle low, and normal device operation resumes if the short-circuit is removed from the output. If a short remains at the output, the cycle continues until the short is removed.

If external MUTE control is desired, and automatic recovery from a short-circuit event is also desired, an OR gate can be used to combine the functionality of the FAULT output and external MUTE control, see [Figure 34](#).





**Figure 34. External MUTE Control**

## MSTR/ $\overline{\text{SLV}}$ and SYNC operation

The MSTR/ $\overline{\text{SLV}}$  and SYNC terminals can be used to synchronize the frequency of the class-D output switching. When the MSTR/ $\overline{\text{SLV}}$  terminal is high, the output switching frequency is determined by the selection of the resistor connected to the ROSC terminal (see ROSC Resistor Selection). The SYNC terminal becomes an output in this mode, and the frequency of this output is also determined by the selection of the ROSC resistor. This TTL compatible, push-pull output can be connected to another TPA3101D2, configured in the slave mode. The output switching is synchronized to avoid any beat frequencies that could occur in the audio band when two class-D amplifiers in the same system are switching at slightly different frequencies.

When the MSTR/ $\overline{\text{SLV}}$  terminal is low, the output switching frequency is determined by the incoming square wave on the SYNC input. The SYNC terminal becomes an input in this mode and accepts a TTL compatible square wave from another TPA3101D2 configured in the master mode or from an external GPIO. If connecting to an external GPIO, recommended frequencies are 200 kHz to 300 kHz for proper device operation, and the maximum amplitude is 4 V.

## USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

## SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

The TPA3101D2 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to- $V_{CC}$  shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the SHUTDOWN pin or MUTE pin. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

The FAULT terminal can be used for automatic recovery from a short-circuit event, or used to monitor the status with an external GPIO. For automatic recovery from a short-circuit event, connect the FAULT terminal directly to the MUTE terminal. When a short-circuit event occurs, the FAULT terminal transitions high indicating a short-circuit has been detected. When directly connected to MUTE, the MUTE terminal transitions high, and clears the internal fault flag. This causes the FAULT terminal to cycle low, and normal device operation resumes if the short-circuit is removed from the output. If a short remains at the output, the cycle continues until the short is removed. If external MUTE control is desired, and automatic recovery from a short-circuit event is also desired, an OR gate can be used to combine the functionality of the FAULT output and external MUTE control, see [Figure 34](#).

## THERMAL PROTECTION

Thermal protection on the TPA3101D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a  $\pm 15^\circ\text{C}$  tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. The device begins normal operation at this point with no external system interaction.

## PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TPA3101D2 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 1 $\mu\text{F}$  decoupling capacitors should be placed as close to the PVCC (pins 26, 27, 34, and 35) and AVCC (pin 48) terminals as possible. The VBYP (pin 16) capacitor, VREG (pin 15) capacitor, and VCLAMP (pins 30 and 31) capacitor should also be placed as close to the device as possible. Large (220  $\mu\text{F}$  or greater) bulk power supply decoupling capacitors should be placed near the TPA3101D2 on the PVCC, PVCCR, and AVCC terminals.
- Grounding—The AVCC (pin 48) decoupling capacitor, VREG (pin 15) capacitor, VBYP (pin 16) capacitor, and ROsc (pin 14) resistor should each be grounded to analog ground (AGND, pin 17). The PVCC decoupling capacitors and VCLAMP capacitors should each be grounded to power ground (PGND, pins 28, 29, 32, and 33). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3101D2.
- Output filter—The ferrite EMI filter ([Figure 29](#)) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter ([Figure 27](#) and [Figure 28](#)) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground. If both filters are used, the LC filter should be placed first, following the outputs.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 5,1 mm by 5,1 mm. Five rows of solid vias (five vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See TI Technical Briefs [SCBA017D](#) and [SLUA271](#) for more information about using the QFN thermal pad. See TI Technical Briefs [SLMA002](#) for more information about using the HTQFP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3101D2 Evaluation Module (TPA3101D2EVM) User Manual, (SLOU179). Both the EVM user manual and the thermal pad application note are available on the TI Web site at <http://www.ti.com>.

## BASIC MEASUREMENT SYSTEM

This application note focuses on methods that use the basic equipment listed below:

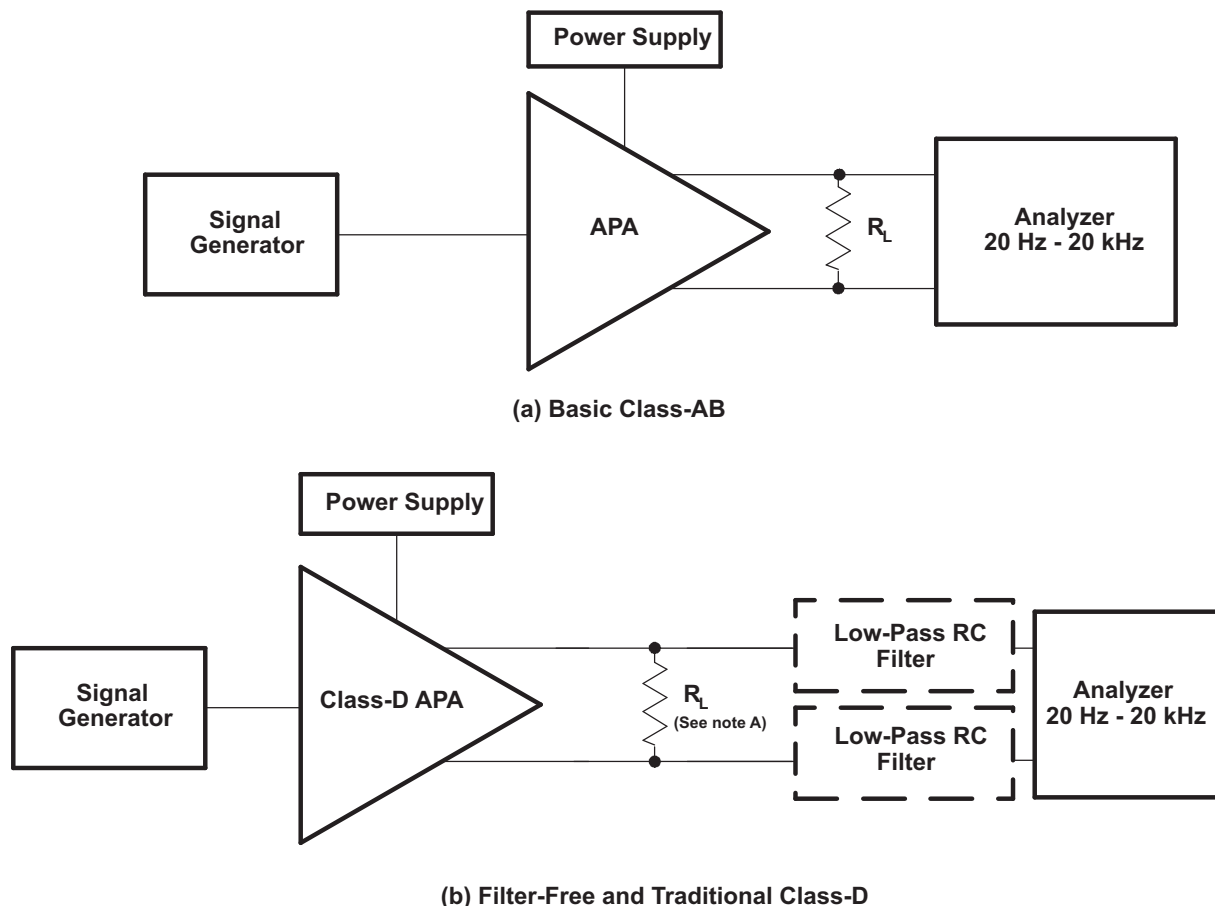
- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

Figure 35 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the APA output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two audio measurement system (AP-II) (Reference 1) by Audio Precision includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, ( $C_{IN}$ ), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer-input impedance should be high. The output resistance,  $R_{OUT}$ , of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 35(a) shows a class-AB amplifier system. It takes an analog signal input and produces an analog signal output. This amplifier circuit can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 35(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.



A. For efficiency measurements with filter-free Class-D,  $R_L$  should be an inductive load like a speaker.

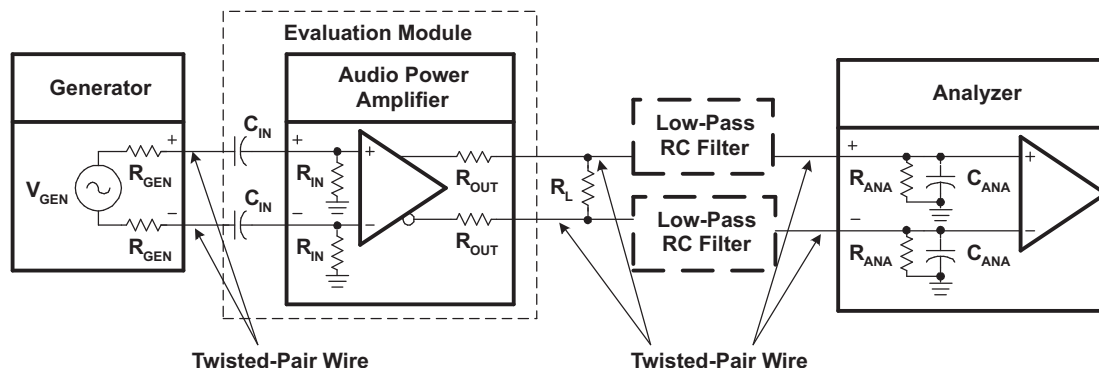
**Figure 35. Audio Measurement Systems**

The TPA3101D2 uses a modulation scheme that does not require an output filter for operation, but they do sometimes require an RC low-pass filter when making measurements. This is because some analyzer inputs cannot accurately process the rapidly changing square-wave output and therefore record an extremely high level of distortion. The RC low-pass measurement filter is used to remove the modulated waveforms so the analyzer can measure the output sine wave.

## DIFFERENTIAL INPUT AND BTL OUTPUT

All of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180 degrees out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc blocking capacitor.

A block diagram of the measurement circuit is shown in [Figure 36](#). The differential input is a balanced input, meaning the positive (+) and negative (-) pins have the same impedance to ground. Similarly, the BTL output equates to a balanced output.



**Figure 36. Differential Input, BTL Output Measurement Circuit**

The generator should have balanced outputs, and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common-mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure that the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see [Table 3](#)).

[Table 3](#) shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch long wire with a 20-kHz sine-wave signal at 25°C.

**Table 3. Recommended Minimum Wire Size for Power Cables**

| $P_{OUT}$ (W) | $R_L$ ( $\Omega$ ) | AWG Size |    | DC POWER LOSS (MW) |     | AC POWER LOSS (MW) |     |
|---------------|--------------------|----------|----|--------------------|-----|--------------------|-----|
| 10            | 4                  | 18       | 22 | 16                 | 40  | 18                 | 42  |
| 2             | 4                  | 18       | 22 | 3.2                | 8   | 3.7                | 8.5 |
| 1             | 8                  | 22       | 28 | 2                  | 8   | 2.1                | 8.1 |
| < 0.75        | 8                  | 22       | 28 | 1.5                | 6.1 | 1.6                | 6.2 |

## CLASS-D RC LOW-PASS FILTER

An RC filter is used to reduce the square-wave output when the analyzer inputs cannot process the pulse-width modulated class-D output waveform. This filter has little effect on the measurement accuracy because the cutoff frequency is set above the audio band. The high frequency of the square wave has negligible impact on measurement accuracy because it is well above the audible frequency range, and the speaker cone cannot respond at such a fast rate. The RC filter is not required when an LC low-pass filter is used, such as with the class-D APAs that employ the traditional modulation scheme (TPA032D0x, TPA005Dxx).

The component values of the RC filter are selected using the equivalent output circuit as shown in [Figure 37](#).  $R_L$  is the load impedance that the APA is driving for the test. The analyzer input impedance specifications should be available and substituted for  $R_{ANA}$  and  $C_{ANA}$ . The filter components,  $R_{FILT}$  and  $C_{FILT}$ , can then be derived for the system. The filter should be grounded to the APA near the output ground pins or at the power supply ground pin to minimize ground loops.

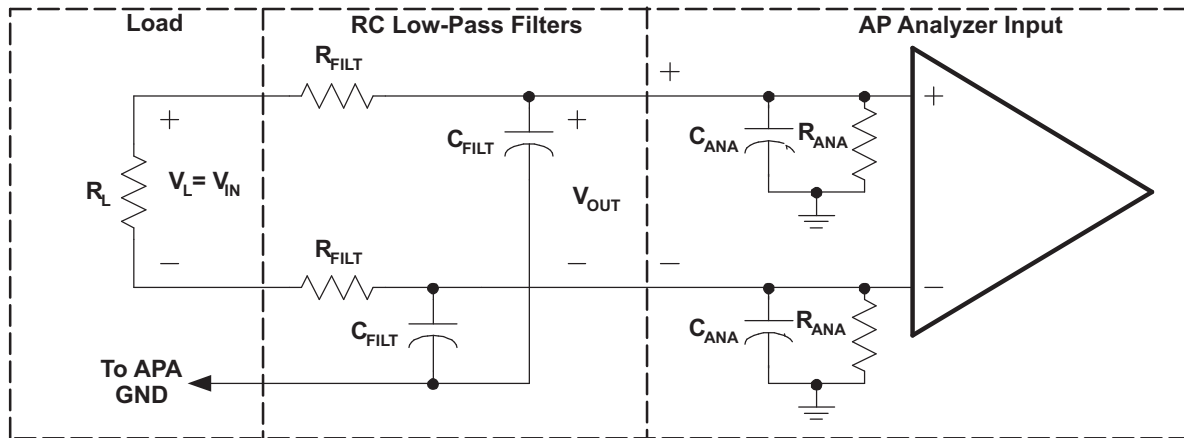


Figure 37. Measurement Low-Pass Filter Derivation Circuit-Class-D APAs

The transfer function for this circuit is shown in Equation 5 where  $\omega_O = R_{EQ}C_{EQ}$ ,  $R_{EQ} = R_{FILT} \parallel R_{ANA}$  and  $C_{EQ} = (C_{FILT} + C_{ANA})$ . The filter frequency should be set above  $f_{MAX}$ , the highest frequency of the measurement bandwidth, to avoid attenuating the audio signal. Equation 6 provides this cutoff frequency,  $f_C$ . The value of  $R_{FILT}$  must be chosen large enough to minimize current that is shunted from the load, yet small enough to minimize the attenuation of the analyzer-input voltage through the voltage divider formed by  $R_{FILT}$  and  $R_{ANA}$ . A general rule is that  $R_{FILT}$  should be small ( $\sim 100 \Omega$ ) for most measurements. This reduces the measurement error to less than 1% for  $R_{ANA} \geq 10 \text{ k}\Omega$ .

$$\left( \frac{V_{OUT}}{V_{IN}} \right) = \frac{\left( \frac{R_{ANA}}{R_{ANA} + R_{FILT}} \right)}{1 + j \left( \frac{\omega}{\omega_O} \right)} \quad (5)$$

$$f_C = \sqrt{2} \times f_{max} \quad (6)$$

An exception occurs with the efficiency measurements, where  $R_{FILT}$  must be increased by a factor of ten to reduce the current shunted through the filter.  $C_{FILT}$  must be decreased by a factor of ten to maintain the same cutoff frequency. See Table 4 for the recommended filter component values.

Once  $f_C$  is determined and  $R_{FILT}$  is selected, the filter capacitance is calculated using . When the calculated value is not available, it is better to choose a smaller capacitance value to keep  $f_C$  above the minimum desired value calculated in Equation 7.

$$C_{FILT} = \frac{1}{2\pi \times f_C \times R_{FILT}} \quad (7)$$

Table 4 shows recommended values of  $R_{FILT}$  and  $C_{FILT}$  based on common component values. The value of  $f_C$  was originally calculated to be 28 kHz for an  $f_{MAX}$  of 20 kHz.  $C_{FILT}$ , however, was calculated to be 57,000 pF, but the nearest values of 56,000 pF and 51,000 pF were not available. A 47,000-pF capacitor was used instead, and  $f_C$  is 34 kHz, which is above the desired value of 28 kHz.

Table 4. Typical RC Measurement Filter Values

| MEASUREMENT            | $R_{FILT}$    | $C_{FILT}$ |
|------------------------|---------------|------------|
| Efficiency             | 1000 $\Omega$ | 5,600 pF   |
| All other measurements | 100 $\Omega$  | 56,000 pF  |

## REVISION HISTORY

| Changes from Revision B (September 2007) to Revision C                                    | Page              |
|-------------------------------------------------------------------------------------------|-------------------|
| • Replaced the TYPICAL DISSIPATION RATINGS table with the Thermal Information Table ..... | <a href="#">2</a> |



## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPA3101D2PHP     | ACTIVE        | HTQFP        | PHP                | 48   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | TPA3101D2               | <a href="#">Samples</a> |
| TPA3101D2PHPR    | ACTIVE        | HTQFP        | PHP                | 48   | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | TPA3101D2               | <a href="#">Samples</a> |
| TPA3101D2RGZR    | ACTIVE        | VQFN         | RGZ                | 48   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | TPA<br>3101D2           | <a href="#">Samples</a> |
| TPA3101D2RGZT    | ACTIVE        | VQFN         | RGZ                | 48   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | TPA<br>3101D2           | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

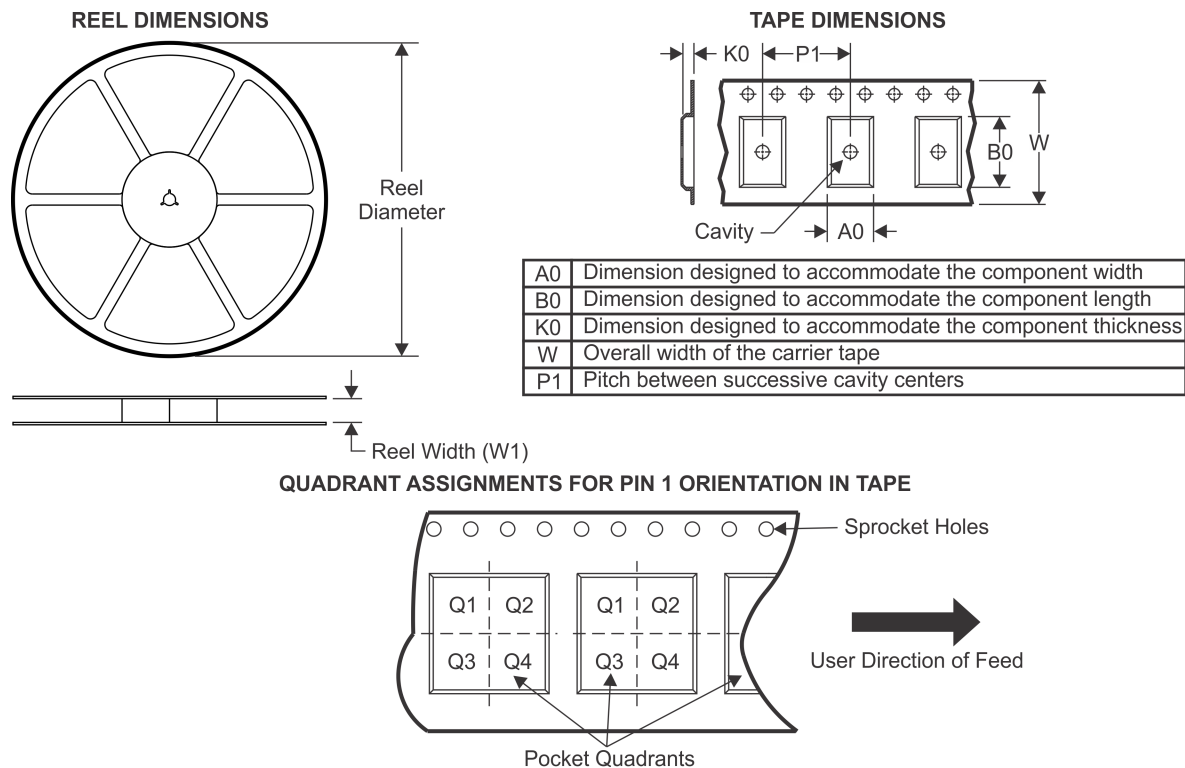
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

---

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

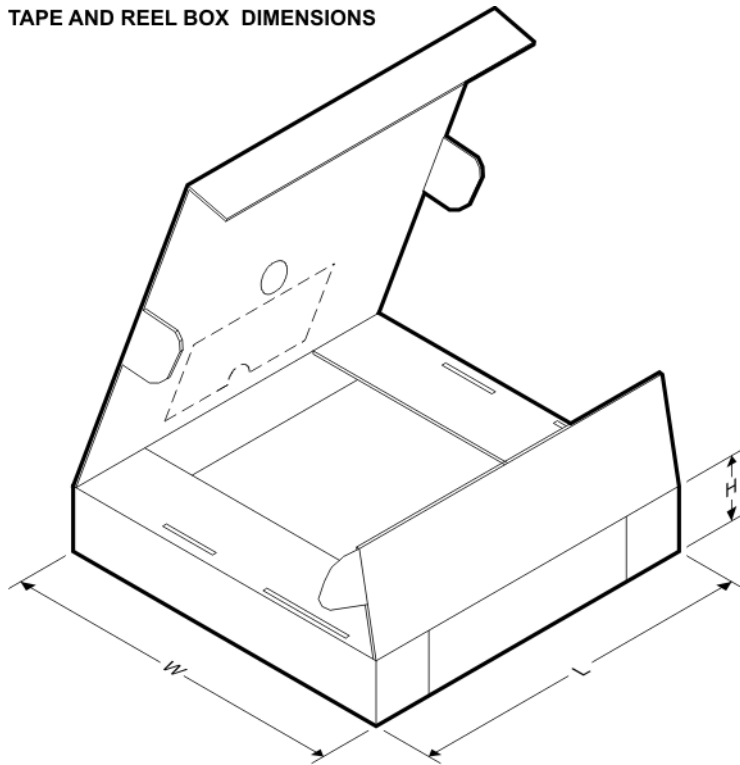
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPA3101D2PHPR | HTQFP        | PHP             | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.5     | 12.0    | 16.0   | Q2            |
| TPA3101D2RGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| TPA3101D2RGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

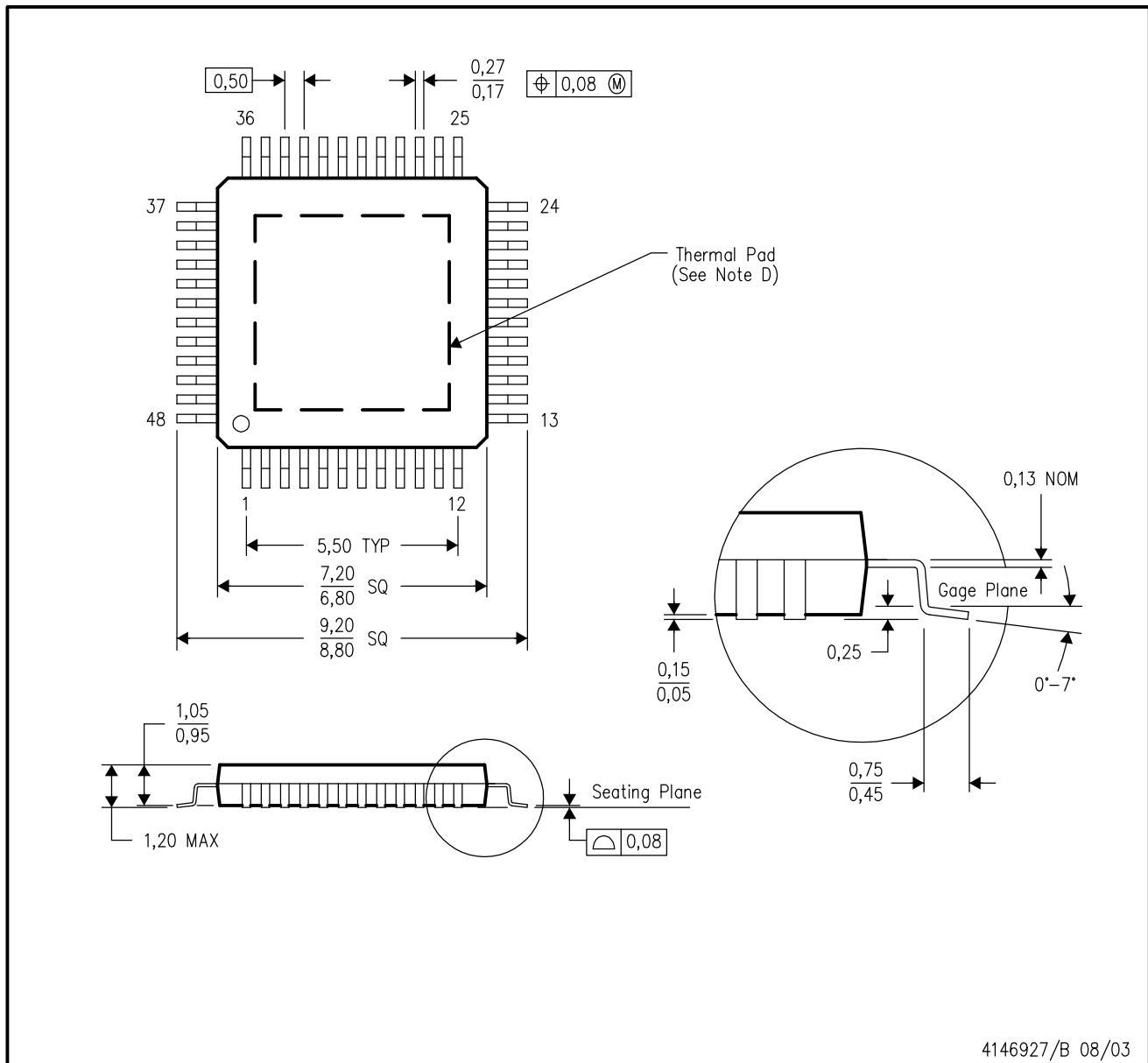


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPA3101D2PHPR | HTQFP        | PHP             | 48   | 1000 | 350.0       | 350.0      | 43.0        |
| TPA3101D2RGZR | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| TPA3101D2RGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

## THERMAL PAD MECHANICAL DATA

PHP (S-PQFP-G48)

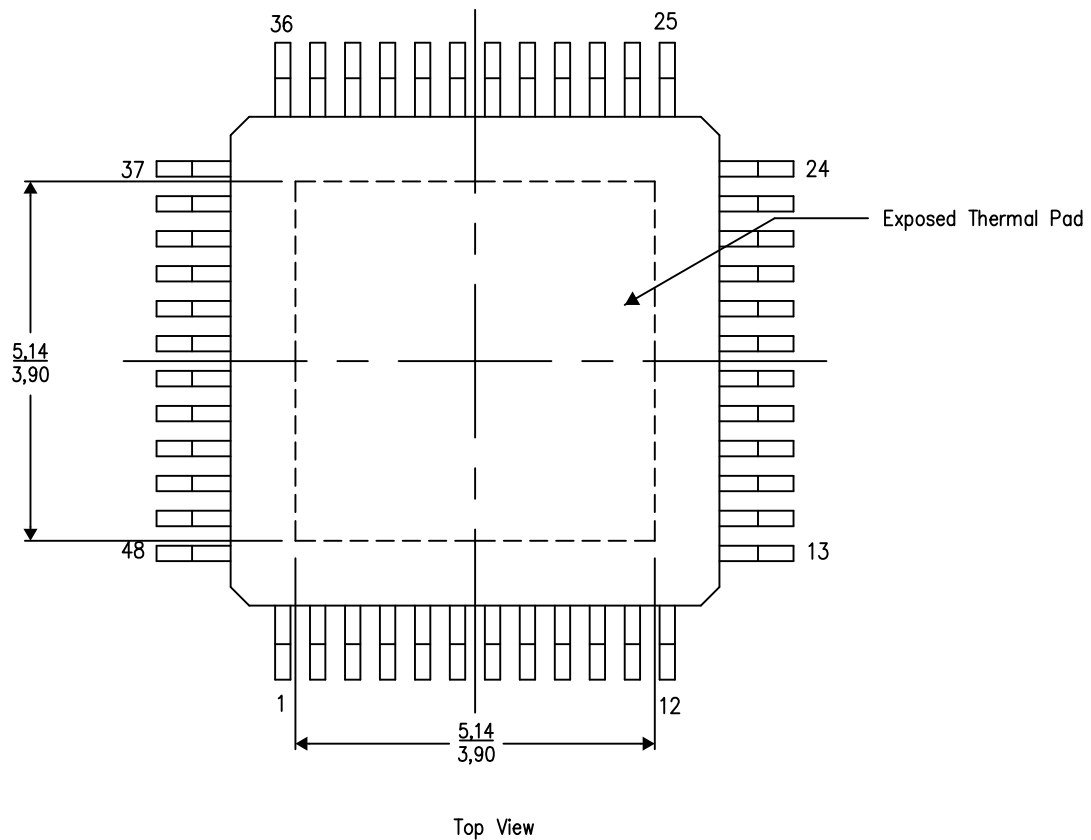
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

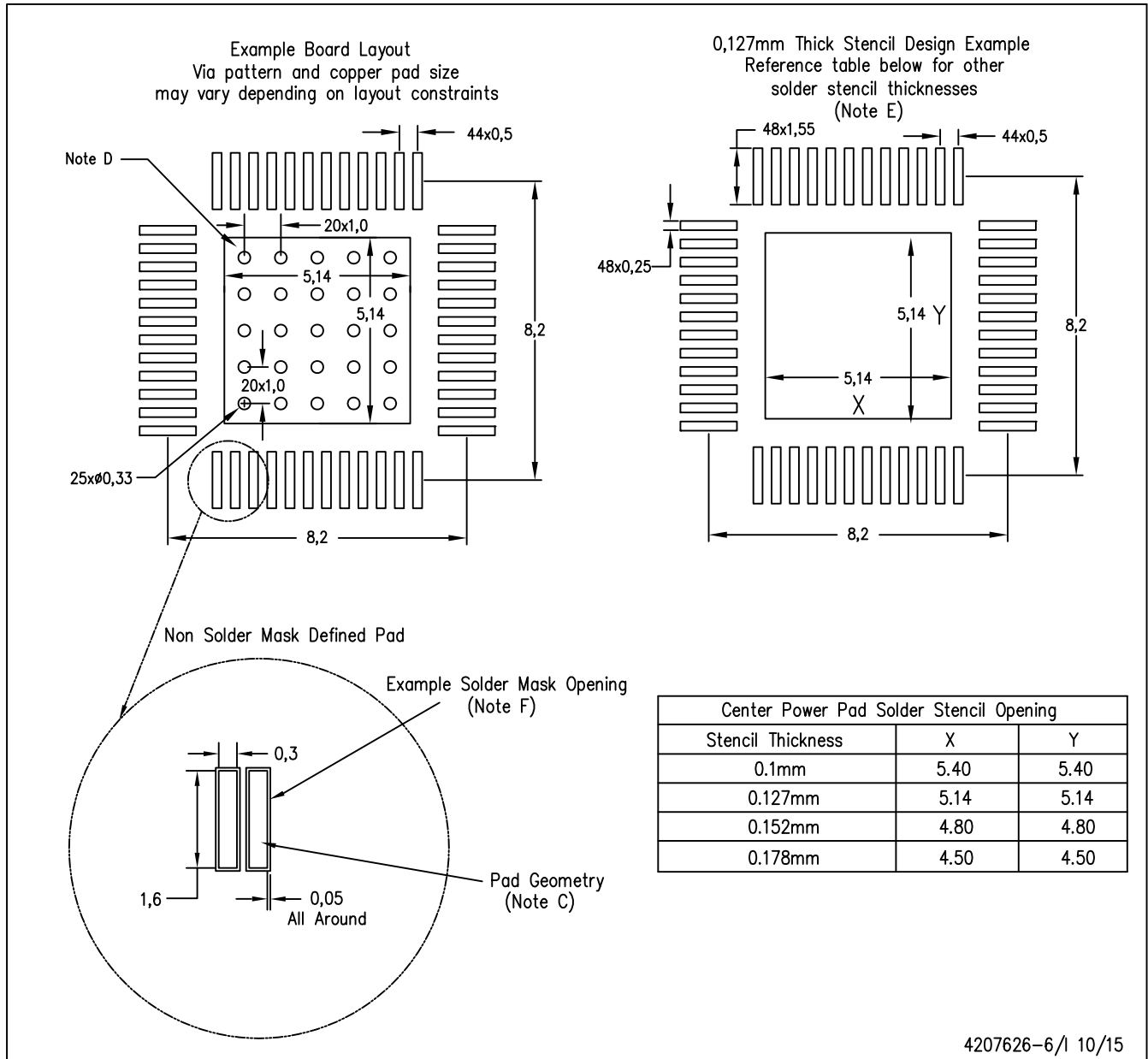
4206329-6/P 03/15

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

PowerPAD is a trademark of Texas Instruments

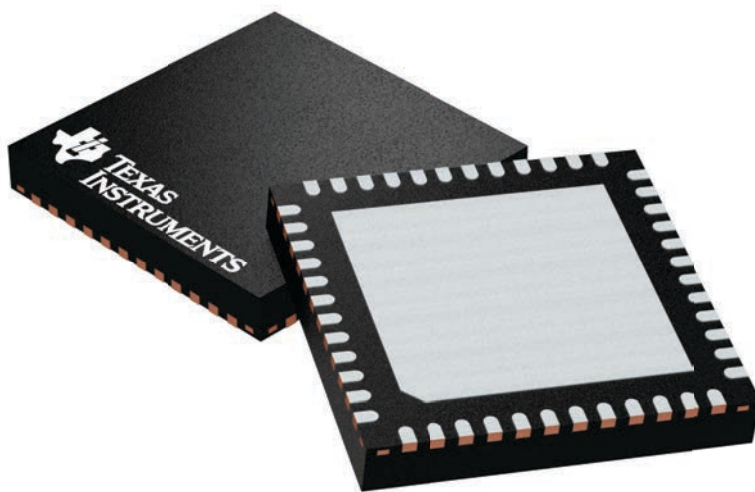
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

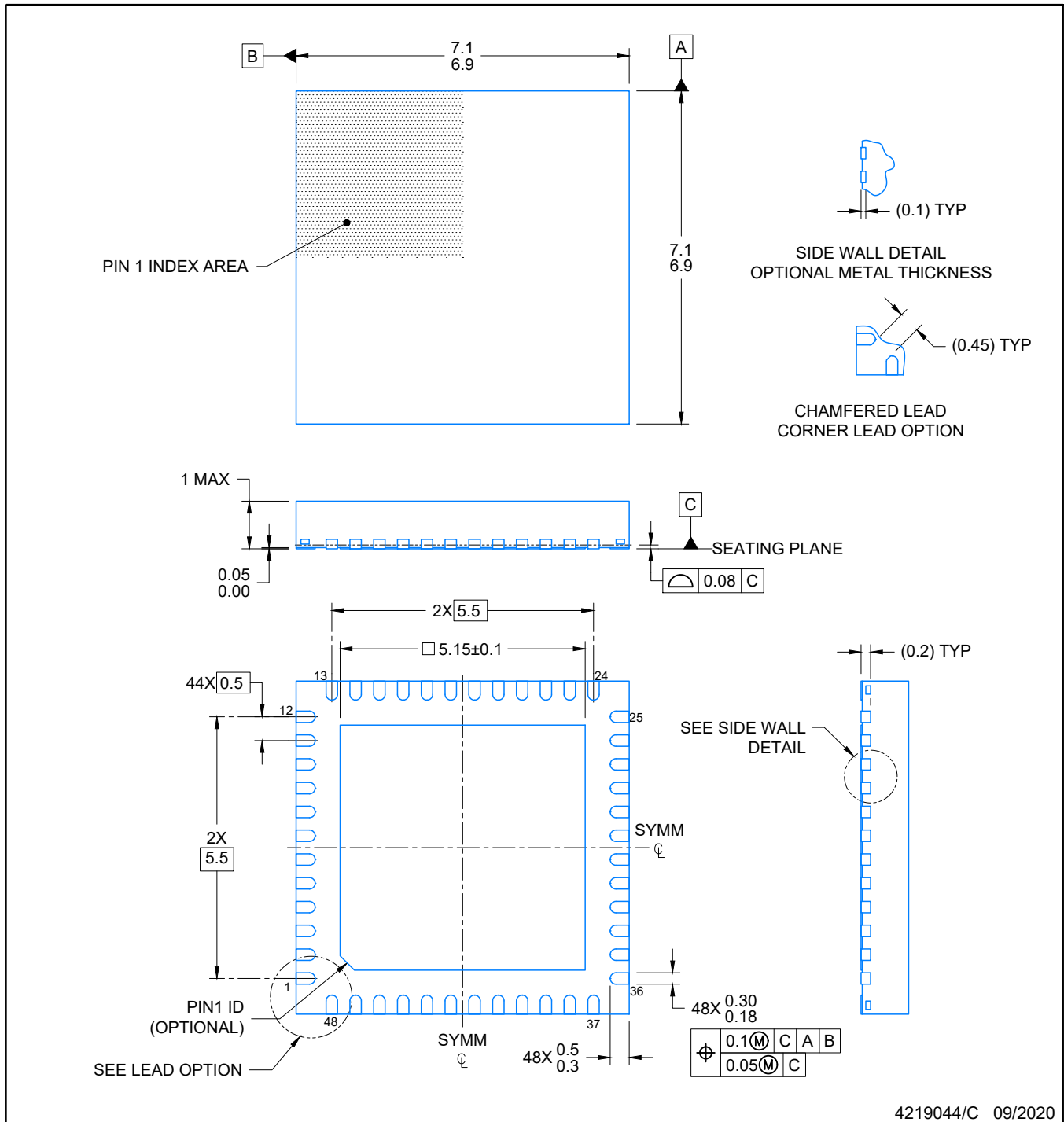
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

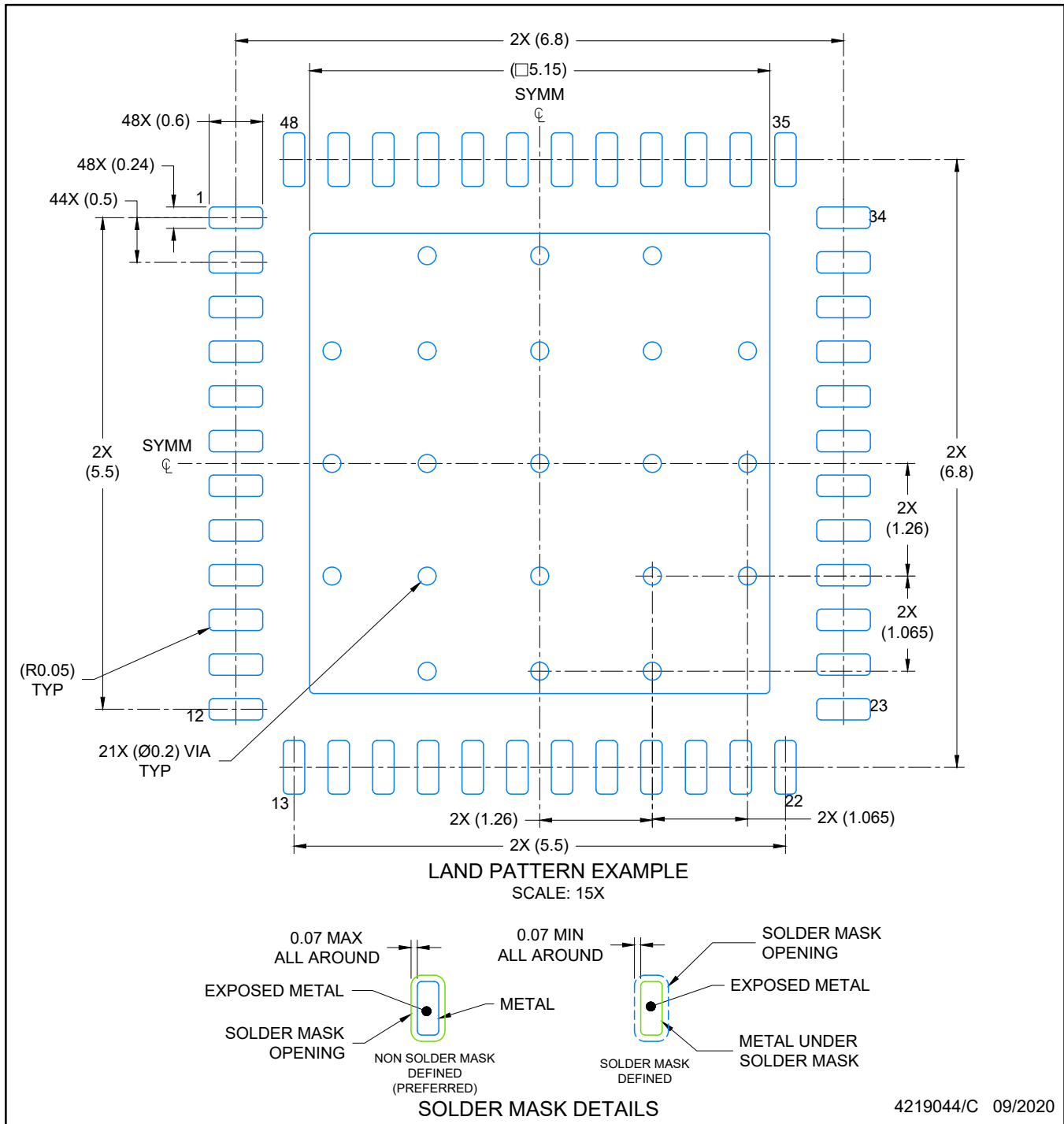
4224671/A





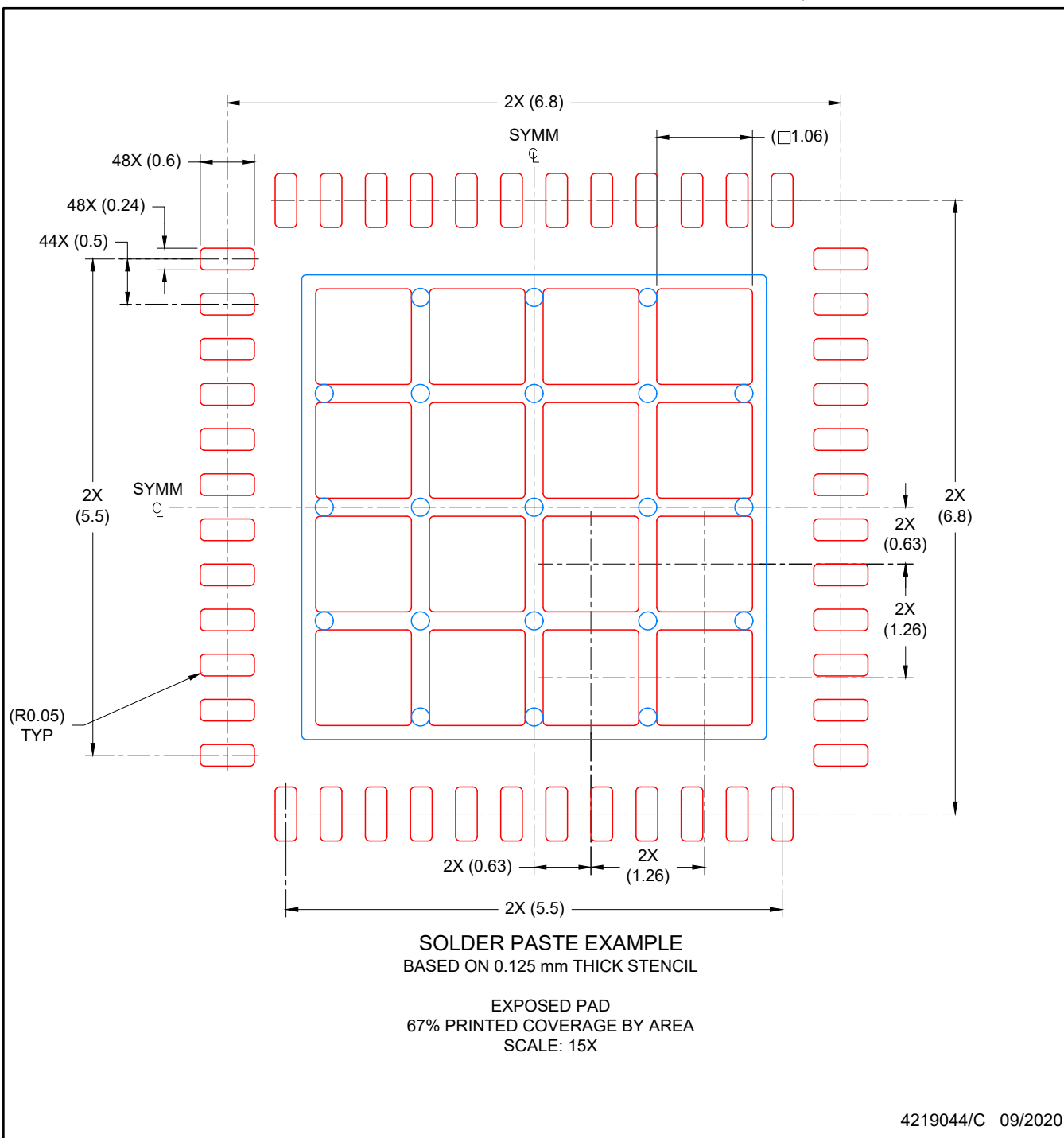
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated