

LM9076Q 150mA Ultra-Low Quiescent Current LDO Regulator with Delayed Reset Output

Check for Samples: [LM9076Q](#)

FEATURES

- AEC-Q100 Grade1 Qualified (-40°C to +125°C)
- Available with 5.0V or 3.3V Output Voltage
- Ultra Low Ground Pin Current, 25 μ A Typical for 100 μ A Load
- V_{OUT} Initial Accuracy of $\pm 1.5\%$
- V_{OUT} Accurate to $\pm 3\%$ Over Load and Temperature Conditions
- Low Dropout Voltage, 200 mV Typical with 150 mA Load
- Low Off State Ground Pin Current for LM9076QBMA
- Delayed $\overline{\text{RESET}}$ Output Pin for Low V_{OUT} Detection
- +70V/-50V Voltage Transients
- Operational V_{IN} up to +40V

DESCRIPTION

The LM9076Q is a $\pm 3\%$, 150 mA logic controlled voltage regulator. The regulator features an active low delayed reset output flag which can be used to reset a microprocessor system at turn-ON and in the event that the regulator output voltage falls below a minimum value. An external capacitor programs a delay time interval before the reset output pin can return high.

Designed for automotive and industrial applications, the LM9076Q contains a variety of protection features such as thermal shutdown, input transient protection and a wide operating temperature range. The LM9076Q uses an PNP pass transistor which allows low drop-out voltage operation.



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Typical Applications

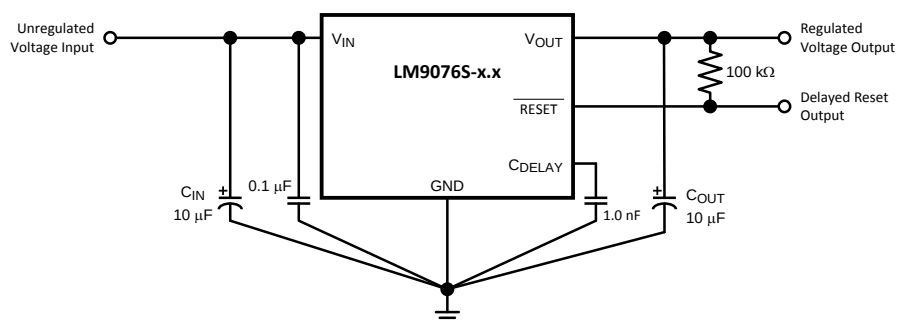


Figure 1. LM9076QS-x.x In 5 lead SFM package

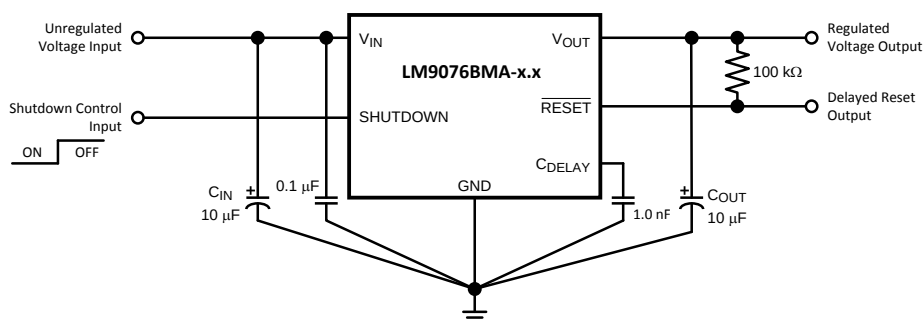


Figure 2. LM9076QBMA-x.x in 8 lead SOIC package

Connection Diagram

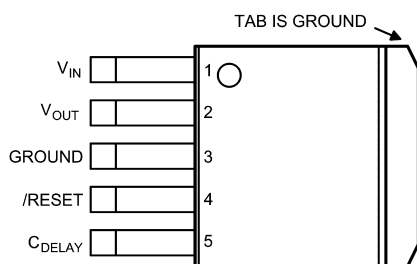


Figure 3. Top View
See SFM Package Number KTT0005B

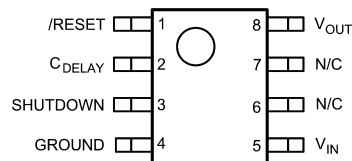


Figure 4. Top View
See SOIC Package Number D0008A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

$V_{IN}(DC)$	-15V to +55V
$V_{IN}(+Transient) t < 10ms$, Duty Cycle <1%	+70V
$V_{IN}(-Transient) t < 1ms$, Duty Cycle <1%	-50V
SHUTDOWN Pin	-15V to +52V
RESET Pin	-0.3V to 20V
C_{DELAY} Pin	-0.3V to $V_{OUT} + 0.3V$
Storage Temperature	-65°C to +150°C
Junction Temperature (T_J)	+175C
ESD, HBM, per AEC - Q100 - 002	+/- 2 kV
ESD, MM, per AEC - Q100 - 003	+/-250V

- (1) Absolute Maximum Ratings indicate the limits beyond which the device may cease to function, and/or damage to the device may occur.
 (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings ⁽¹⁾

V _{IN} Pin		5.35V to 40V
V _{SHUTDOWN} Pin		0V to 40V
Junction Temperature		−40°C < T _J < +125°C
Thermal Resistance KTT0005B ⁽²⁾	θ _{ja}	75°C/W
	θ _{jc}	2.9°C/W
Thermal Resistance D0008A ⁽²⁾	θ _{ja}	156°C/W
	θ _{jc}	59°C/W

- (1) Absolute Maximum Ratings indicate the limits beyond which the device may cease to function, and/or damage to the device may occur.
 (2) Worst case (FREE AIR) per EIA/JESD51–3.

Electrical Characteristics for LM9076Q–3.3

The following specifications apply for $V_{IN} = 14V$; $I_{LOAD} = 10\text{ mA}$; $T_J = +25^\circ\text{C}$; $C_{OUT} = 10\text{ }\mu\text{F}$, $0.5\Omega < \text{ESR} < 4.0\Omega$; unless otherwise specified. **Bold values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$.** ^{(1) (2)} Minimum and Maximum limits are specified through test, design or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LM9076Q–3.3 REGULATOR CHARACTERISTICS						
V_{OUT}	Output Voltage		3.251	3.30	3.349	V
		$-20^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ $1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	3.234	3.30	3.366	V
		$1\text{mA} \leq I_{LOAD} \leq 150\text{ mA}$	3.201	3.30	3.399	V
		$V_{IN} = 60V$, $R_{LOAD} = 1\text{ k}\Omega$, $t \leq 40ms$	2.970	3.30	3.630	V
	Output Voltage Off LM9076Q BMA only	$V_{SHUTDOWN} \geq 2V$, $R_{LOAD} = 1\text{ k}\Omega$	–	0	250	mV
	Reverse Battery	$V_{IN} = -15V$, $R_{LOAD} = 1\text{ k}\Omega$	–300	0	–	mV
ΔV_{OUT}	Line Regulation	$9.0V \leq V_{IN} \leq 16V$, $I_{LOAD} = 10\text{ mA}$	–	4	25	mV
		$16V \leq V_{IN} \leq 40V$, $I_{LOAD} = 10\text{ mA}$	–	17	35	mV
	Load Regulation	$1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	–	42	60	mV

- (1) The regulated output voltage specification is not ensured for the entire range of V_{IN} and output loads. Device operational range is limited by the maximum junction temperature (T_J). The junction temperature is influenced by the ambient temperature (T_A), package selection, input voltage (V_{IN}), and the output load current. When operating with maximum load currents the input voltage and/or ambient temperature will be limited. When operating with maximum input voltage the load current and/or the ambient temperature will be limited.
 (2) Pulse testing used maintain constant junction temperature (T_J).

Electrical Characteristics for LM9076Q–3.3 (continued)

The following specifications apply for $V_{IN} = 14V$; $I_{LOAD} = 10\text{ mA}$; $T_J = +25^\circ\text{C}$; $C_{OUT} = 10\text{ }\mu\text{F}$, $0.5\Omega < \text{ESR} < 4.0\Omega$; unless otherwise specified. **Bold values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$.**^{(1) (2)} Minimum and Maximum limits are specified through test, design or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DO}	Dropout Voltage	$I_{LOAD} = 10\text{ mA}$	–	30	50	mV
		$I_{LOAD} = 50\text{ mA}$	–	80	–	mV
		$I_{LOAD} = 150\text{ mA}$	–	150	250	mV
I_{GND}	Ground Pin Current	$9V \leq V_{IN} \leq 16V$, $I_{LOAD} = 100\text{ }\mu\text{A}$	–	25	45	μA
		$9V \leq V_{IN} \leq 40V$, $I_{LOAD} = 10\text{ mA}$	–	125	160	μA
		$9V \leq V_{IN} \leq 40V$, $I_{LOAD} = 50\text{ mA}$	–	0.6	–	mA
		$9V \leq V_{IN} \leq 16V$, $I_{LOAD} = 150\text{ mA}$	–	3.6	4.5	mA
I_{SC}	V_{OUT} Short Circuit Current	$V_{IN} = 14V$, $R_{LOAD} = 1\Omega$	200	400	750	mA
PSRR	Ripple Rejection	$V_{IN} = (14V_{DC}) + (1V_{RMS} @ 120\text{Hz})$ $I_{LOAD} = 50\text{ mA}$	50	60	–	dB
RESET PIN CHARACTERISTICS						
V_{OR}	Minimum V_{IN} for valid RESET Status		⁽³⁾ –	1.3	2.0	V
V_{THR}	V_{OUT} Threshold for RESET Low	⁽³⁾	0.83	0.89	0.94	X V_{OUT} (Nom)
V_{OH}	$\overline{\text{RESET}}$ pin high voltage	External pull-up resistor to $V_{OUT} = 100\text{ k}\Omega$	$V_{OUT} \times 0.90$	$V_{OUT} \times 0.99$	V_{OUT}	V
V_{OL}	$\overline{\text{RESET}}$ pin low voltage	$C_{DELAY} < 4.0V$, $I_{SINK} = 250\text{ }\mu\text{A}$	–	0.2	0.3	V
C_{DELAY} PIN CHARACTERISTICS						
I_{DELAY}	C_{DELAY} Charging Current	$V_{IN} = 14V$, $V_{DELAY} = 0V$	-0.70	-0.42	-0.25	μA
V_{OL}	C_{DELAY} pin low voltage	$V_{OUT} < 4.0V$, $I_{SINK} = I_{DELAY}$	–	0.100	–	V
t_{DELAY}	Reset Delay Time	$V_{IN} = 14V$, $C_{DELAY} = 0.001\text{ }\mu\text{F}$ V_{OUT} rising from 0V, Δt from $V_{OUT} > V_{OR}$ to RESET pin HIGH	4.7	7.8	13.2	ms

(3) Not Production tested, Specified by Design. Minimum, Typical, and/or Maximum values are provided for informational purposes only.

Electrical Characteristics for LM9076Q–5.0

The following specifications apply for $V_{IN} = 14V$; $V_{SHUTDOWN} = \text{Open}$; $I_{LOAD} = 10 \text{ mA}$; $T_J = +25^\circ\text{C}$; $C_{OUT} = 10 \mu\text{F}$, $0.5\Omega < \text{ESR} < 4.0\Omega$; unless otherwise specified. **Bold Values indicate $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$.** ⁽¹⁾, ⁽²⁾ Minimum and Maximum limits are specified through test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LM9076Q–5.0 REGULATOR CHARACTERISTICS						
V_{OUT}	Output Voltage		4.925	5.00	5.075	V
		$-20^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ $1 \text{ mA} \leq I_{LOAD} \leq 150 \text{ mA}$	4.900	5.00	5.100	V
		$1 \text{ mA} \leq I_{LOAD} \leq 150 \text{ mA}$	4.850	5.00	5.150	V
		$V_{IN} = 60V$, $R_{LOAD} = 1 \text{ k}\Omega$, $t \leq 40\text{ms}$	4.500	5.00	5.500	V
	Output Voltage Off LM9076Q BMA only	$V_{SHUTDOWN} \geq 2V$, $R_{LOAD} = 1 \text{ k}\Omega$	–	0	250	mV
	Reverse Battery	$V_{IN} = -15V$, $R_{LOAD} = 1 \text{ k}\Omega$	–300	0	–	mV
ΔV_{OUT}	Line Regulation	$9.0V \leq V_{IN} \leq 16V$, $I_{LOAD} = 10 \text{ mA}$	–	4	25	mV
		$16V \leq V_{IN} \leq 40V$, $I_{LOAD} = 10 \text{ mA}$	–	17	35	mV
	Load Regulation	$1 \text{ mA} \leq I_{LOAD} \leq 150 \text{ mA}$	–	42	60	mV
V_{DO}	Dropout Voltage	$I_{LOAD} = 10 \text{ mA}$	–	30	50	mV
		$I_{LOAD} = 50 \text{ mA}$	–	80	–	mV
		$I_{LOAD} = 150 \text{ mA}$	–	150	250	mV
I_{GND}	Ground Pin Current	$9V \leq V_{IN} \leq 16V$, $I_{LOAD} = 100 \mu\text{A}$	–	25	45	μA
		$9V \leq V_{IN} \leq 40V$, $I_{LOAD} = 10 \text{ mA}$	–	125	160	μA
		$9V \leq V_{IN} \leq 40V$, $I_{LOAD} = 50 \text{ mA}$	–	0.6	–	mA
		$9V \leq V_{IN} \leq 16V$, $I_{LOAD} = 150 \text{ mA}$	–	3.6	4.5	mA
	Ground Pin Current in Shutdown Mode	$9V \leq V_{IN} \leq 40V$, $V_{SHUTDOWN} = 2V$	–	15	25	μA
I_{SC}	V_{OUT} Short Circuit Current	$V_{IN} = 14V$, $R_{LOAD} = 1\Omega$	200	400	750	mA
PSRR	Ripple Rejection	$V_{IN} = (14V_{DC}) + (1V_{RMS}$ @ 120Hz) $I_{LOAD} = 50 \text{ mA}$	50	60	–	dB
RESET PIN CHARACTERISTICS						
V_{OR}	Minimum V_{IN} for valid RESET Status		⁽³⁾ –	1.3	2.0	V
V_{THR}	V_{OUT} Threshold for RESET Low	⁽³⁾	0.83	0.89	0.94	X V_{OUT} (Nom)
V_{OH}	$\overline{\text{RESET}}$ pin high voltage	External pull-up resistor to $V_{OUT} = 100 \text{ k}\Omega$	$V_{OUT} \times 0.90$	$V_{OUT} \times 0.99$	V_{OUT}	V
V_{OL}	$\overline{\text{RESET}}$ pin low voltage	$C_{DELAY} < 4.0V$, $I_{SINK} = 250 \mu\text{A}$	–	0.2	0.3	V
C_{DELAY} PIN CHARACTERISTICS						
I_{DELAY}	C_{DELAY} Charging Current	$V_{IN} = 14V$, $V_{DELAY} = 0V$	–0.70	–0.42	–0.25	μA

(1) Pulse testing used maintain constant junction temperature (T_J).

(2) The regulated output voltage specification is not ensured for the entire range of V_{IN} and output loads. Device operational range is limited by the maximum junction temperature (T_J). The junction temperature is influenced by the ambient temperature (T_A), package selection, input voltage (V_{IN}), and the output load current. When operating with maximum load currents the input voltage and/or ambient temperature will be limited. When operating with maximum input voltage the load current and/or the ambient temperature will be limited.

(3) Not Production tested, Specified by Design. Minimum, Typical, and/or Maximum values are provided for informational purposes only.

Electrical Characteristics for LM9076Q–5.0 (continued)

The following specifications apply for $V_{IN} = 14V$; $V_{SHUTDOWN} = \text{Open}$; $I_{LOAD} = 10 \text{ mA}$; $T_J = +25^\circ\text{C}$; $C_{OUT} = 10 \mu\text{F}$, $0.5\Omega < \text{ESR} < 4.0\Omega$; unless otherwise specified. **Bold Values indicate $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$.** ⁽¹⁾, ⁽²⁾ Minimum and Maximum limits are specified through test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	C_{DELAY} pin low voltage	$V_{OUT} < 4.0V$, $I_{SINK} = I_{DELAY}$	–	0.100	–	V
t_{DELAY}	Reset Delay Time	$V_{IN} = 14V$, $C_{DELAY} = 0.001 \mu\text{F}$ V_{OUT} rising from 0V, Δt from $V_{OUT} > V_{OR}$ to RESET pin HIGH	7.1	11.9	20.0	ms
SHUTDOWN CONTROL LOGIC — LM9076QBMA-5.0 Only						
$V_{IL(SD)}$	SHUTDOWN Pin Low Threshold Voltage	$V_{SHUTDOWN}$ pin falling from 5.0V until $V_{OUT} > 4.5V$ ($V_{OUT} = \text{On}$)	1	1.5	–	V
$V_{IH(SD)}$	SHUTDOWN Pin High Threshold Voltage	$V_{SHUTDOWN}$ pin rising from 0V until $V_{OUT} < 0.5V$ ($V_{OUT} = \text{Off}$)	–	1.5	2	V
$I_{IH(SD)}$	SHUTDOWN Pin High Bias Current	$V_{SHUTDOWN} = 40V$	–	35	–	μA
		$V_{SHUTDOWN} = 5V$	–	15	35	μA
		$V_{SHUTDOWN} = 2V$	–	6	10	μA
$I_{IL(SD)}$	SHUTDOWN Pin Low Bias Current	$V_{SHUTDOWN} = 0V$	–	0	–	μA

Typical Performance Characteristics

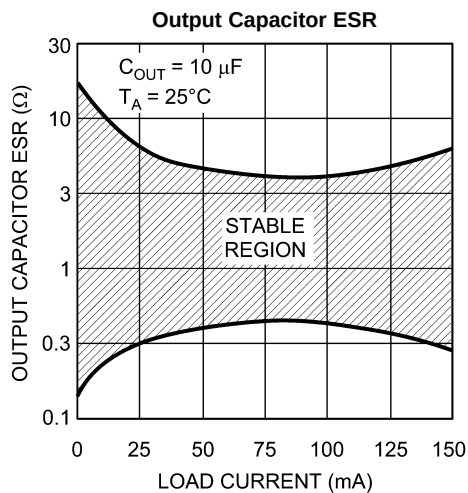


Figure 5.

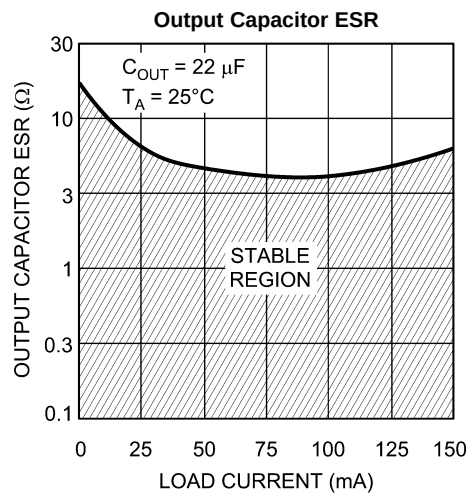


Figure 6.

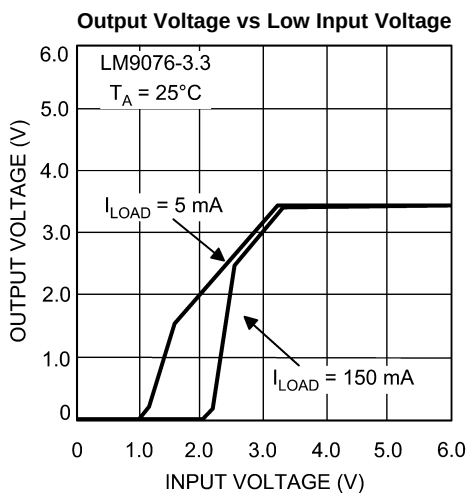


Figure 7.

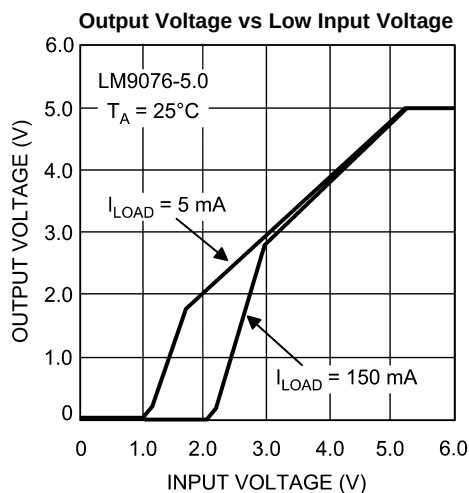


Figure 8.

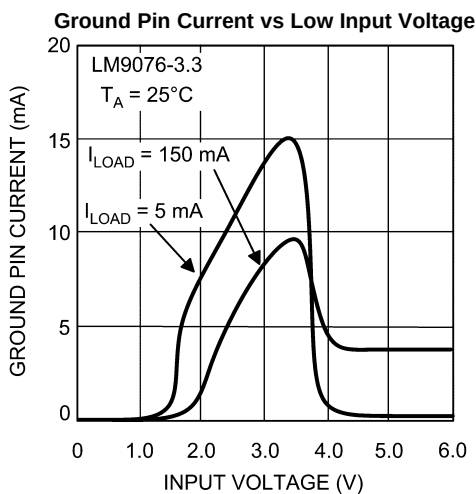


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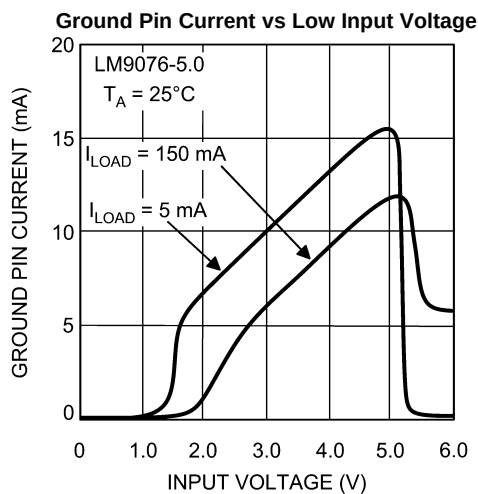


Figure 10.

Typical Performance Characteristics (continued)

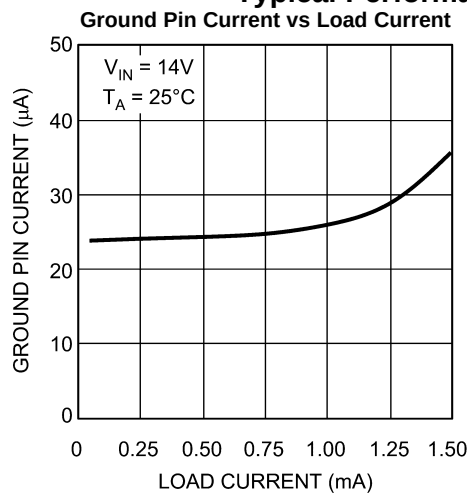


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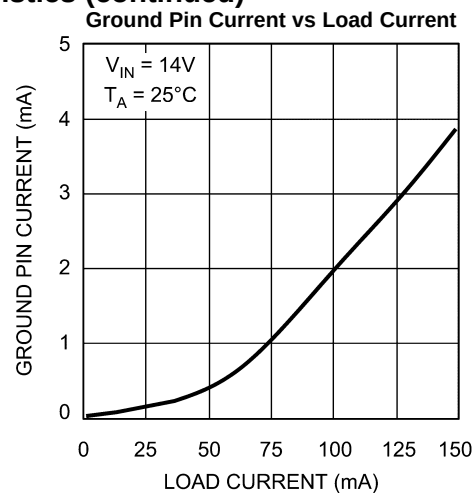


Figure 12.

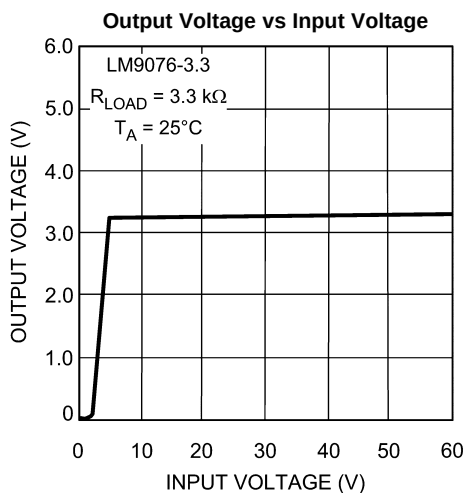


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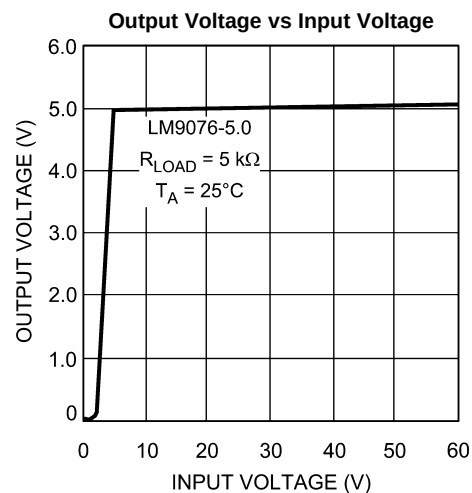


Figure 14.

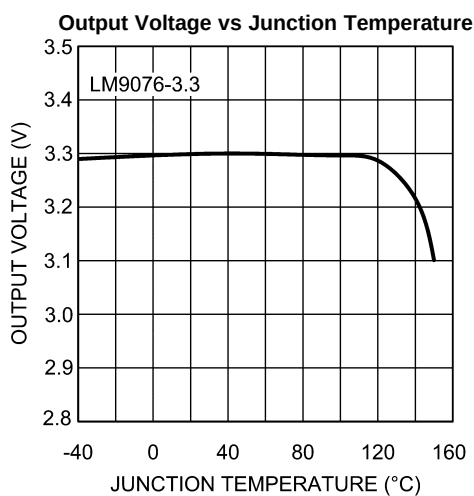


Figure 15.

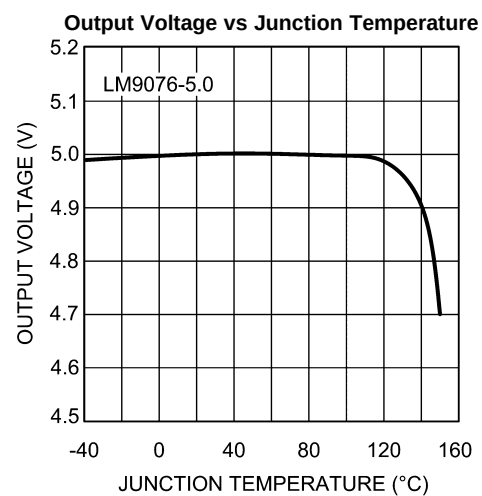


Figure 16.

Typical Performance Characteristics (continued)

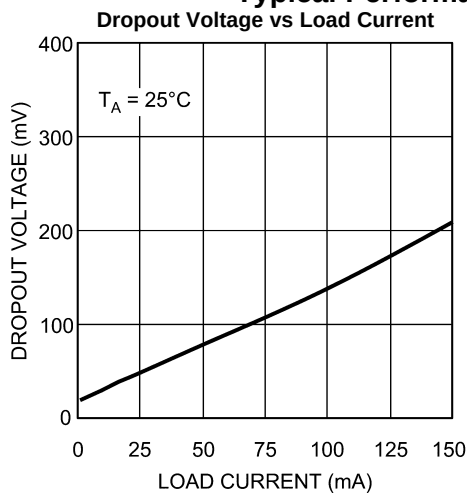


Figure 17.

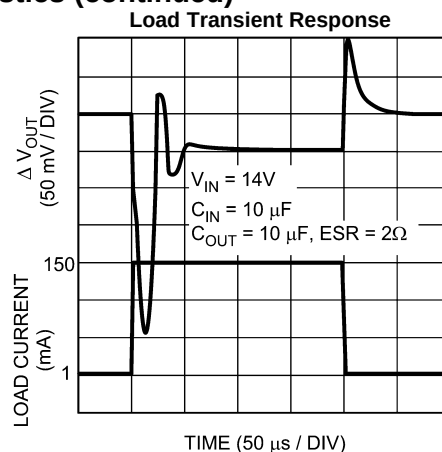


Figure 18.

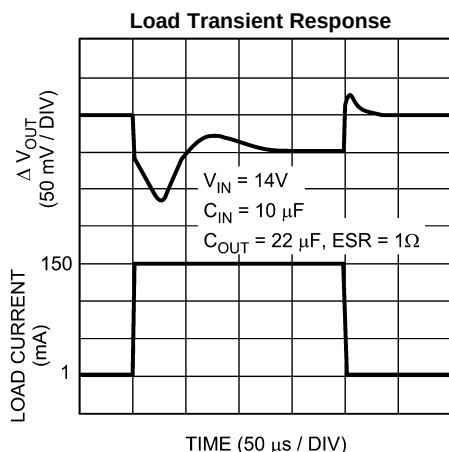


Figure 19.

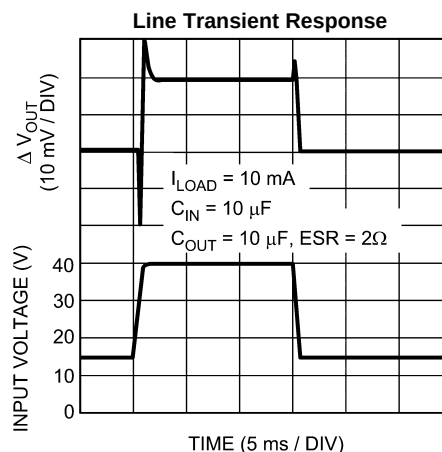


Figure 20.

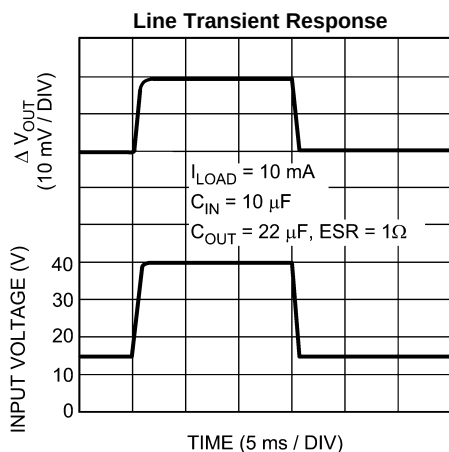


Figure 21.

Delayed Reset Time vs V_{IN} Normalized to $V_{IN} = 14\text{V}$

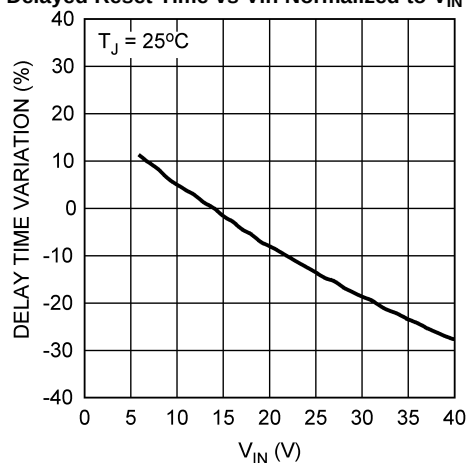


Figure 22.

Typical Performance Characteristics (continued)

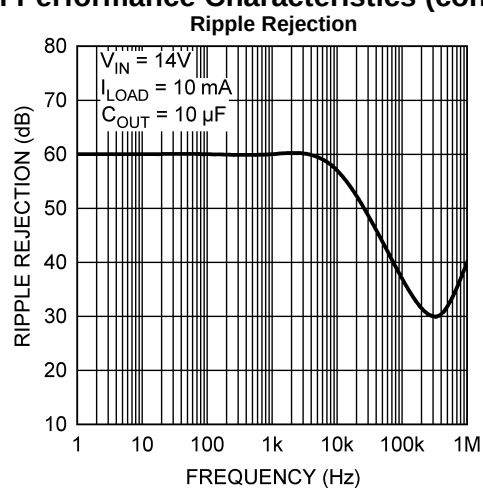


Figure 23.

APPLICATION INFORMATION

REGULATOR BASICS

The LM9076Q regulator is suitable for Automotive and Industrial applications where continuous connection to a battery supply is required (refer to the Typical Application circuit).

The pass element of the regulator is a PNP device which requires an output bypass capacitor for stability. The minimum bypass capacitance for the output is 10 μF (refer to ESR limitations). A 22 μF , or larger, output bypass capacitor is recommended for typical applications

INPUT CAPACITOR

The LM9076Q requires a low source impedance to maintain regulator stability because critical portions of the internal bias circuitry are connected to directly to V_{IN} . In general, a 10 μF electrolytic capacitor, located within two inches of the LM9076Q, is adequate for a majority of applications. Additionally, and at a minimum, a 0.1 μF ceramic capacitor should be located between the LM9076Q V_{IN} and Ground pin, and as close as is physically possible to the LM9076Q itself .

OUTPUT CAPACITOR

An output bypass capacitor is required for stability. This capacitance must be placed between the LM9076Q V_{OUT} pin and Ground pin, as close as is physically possible, using traces that are not part of the load current path.

The output capacitor must meet the requirements for minimum capacitance and also maintain the appropriate ESR value across the entire operating ambient temperature range. There is no limit to the maximum output capacitance as long as ESR is maintained.

The minimum bypass capacitance for the output is 10 μF (refer to ESR limitations). A 22 μF , or larger, output bypass capacitor is recommended for typical applications.

Solid tantalums capacitors are recommended as they generally maintain capacitance and ESR ratings over a wide temperature range. Ceramic capacitor types XR7 and XR5 may be used if a series resistor is added to simulate the minimum ESR requirement. See [Figure 24](#).

Aluminum electrolytic capacitors are not recommended as they are subject to wide changes in capacitance and ESR across temperature.

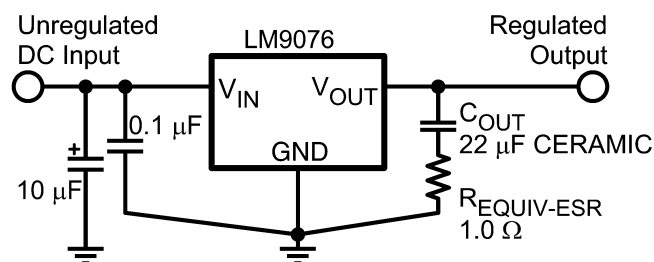


Figure 24. Using Low ESR Capacitors

DELAY CAPACITOR

The capacitor on the Delay pin must be a low leakage type since the charge current is minimal (420 nA typical) and the pin must fully charge to V_{OUT} . Ceramic, Mylar, and polystyrene capacitor types are generally recommended, although changes in capacitance values across temperature changes will have some effect on the delay timing.

Any leakage of the I_{DELAY} current, be it through the delay capacitor or any other path, will extend the delay time, possibly to the point that the Reset pin output does not go high.

SHUTDOWN PIN - LM9076QBMA ONLY

The basic On/Off control of the regulator is accomplished with the SHUTDOWN pin. By pulling the SHUTDOWN pin high the regulator output is switched Off. When the regulator is switched Off the load on the battery will be primarily due to the SHUTDOWN pin current.

When the SHUTDOWN pin is low, or left open, the regulator is switched On. When an unregulated supply, such as V BATTERY, is used to pull the SHUTDOWN pin high a series resistor in the range of 10KΩ to 50KΩ is recommended to provide reverse voltage transient protection of the SHUTDOWN pin. Adding a small capacitor (0.001μF typical) from the SHUTDOWN pin to Ground will add noise immunity to prevent accidental turn on due to noise on the supply line.

RESET FLAG

The $\overline{\text{RESET}}$ pin is an open collector output which requires an external pull-up resistor to develop the reset signal. The external pull-up resistor should be in the range of 10 kΩ to 200 kΩ.

At V_{IN} values of less than typically 2V the $\overline{\text{RESET}}$ pin voltage will be high. For V_{IN} values between typically 2V and approximately $V_{\text{OUT}} + V_{\text{BE}}$ the $\overline{\text{RESET}}$ pin voltage will be low. For V_{IN} values greater than approximately $V_{\text{OUT}} + V_{\text{BE}}$ the $\overline{\text{RESET}}$ pin voltage will be dependent on the status of the V_{OUT} pin voltage and the Delayed Reset circuitry. The value of V_{BE} is typically 600 mV at 25°C and will decrease approximately 2 mV for every 1°C increase in the junction temperature. During normal operation the $\overline{\text{RESET}}$ pin voltage will be high.

Any load condition that causes the V_{OUT} pin voltage to drop below typically 89% of normal will activate the Delayed Reset circuit and the $\overline{\text{RESET}}$ pin will go low for the duration of the delay time.

Any line condition that causes V_{IN} pin voltage to drop below typically $V_{\text{OUT}} + V_{\text{BE}}$ will cause the $\overline{\text{RESET}}$ pin to go low without activating the Delayed Reset circuitry.

Excessive thermal dissipation will raise the junction temperature and could activate the Thermal Shutdown circuitry which, in turn, will cause the $\overline{\text{RESET}}$ pin to go low.

For the LM9076QBMA devices, pulling the SHUTDOWN pin high will turn off the output which, in turn, will cause the $\overline{\text{RESET}}$ pin to go low once the V_{OUT} voltage has decayed to a value that is less than typically 89% of normal. See [Figure 25](#).

RESET DELAY TIME

When the regulator output is switched On, or after recovery from brief V_{OUT} fault condition, the $\overline{\text{RESET}}$ flag can be programmed to remain low for an additional delay time. This will give time for any system reference voltages, clock signals, etc., to stabilize before the micro-controller resumes normal operation.

This delay time is controlled by the capacitor value on the C_{DELAY} pin. During normal operation the C_{DELAY} capacitor is charged to near V_{OUT} . When a V_{OUT} fault causes the $\overline{\text{RESET}}$ pin to go low, the C_{DELAY} capacitor is quickly discharged to ground. When the V_{OUT} fault is removed, and V_{OUT} returns to the normal operating value, the C_{DELAY} capacitor begins charging at a typical constant 0.420 uA rate. When the voltage on the C_{DELAY} capacitor reaches the same potential as the V_{OUT} pin the $\overline{\text{RESET}}$ pin will be allowed to return high.

The typical $\overline{\text{RESET}}$ delay time can be calculated with the following formula:

$$t_{\text{DELAY}} = V_{\text{OUT}} \times (C_{\text{DELAY}} / I_{\text{DELAY}}) \quad (1)$$

For the LM9076Q–3.3 with a C_{DELAY} value of 0.001 uF and a I_{DELAY} value of 0.420 uA the typical $\overline{\text{RESET}}$ delay time is:

$$t_{\text{DELAY}} = 3.3\text{V} \times (0.001 \text{ uF} / 0.420 \text{ uA}) = 7.8 \text{ ms} \quad (2)$$

For the LM9076Q–5.0 with a C_{DELAY} value of 0.001 uF and a I_{DELAY} value of 0.420 uA the typical $\overline{\text{RESET}}$ delay time is:

$$t_{\text{DELAY}} = 5.0\text{V} \times (0.001\text{uF} / 0.420\text{uA}) = 11.9 \text{ ms} \quad (3)$$

THERMAL PROTECTION

Device operational range is limited by the maximum junction temperature (T_{J}). The junction temperature is influenced by the ambient temperature (T_{A}), package selection, input voltage (V_{IN}), and the output load current. When operating with maximum load currents the input voltage and/or ambient temperature will be limited. When operating with maximum input voltage the load current and/or the ambient temperature will be limited.

Even though the LM9076Q is equipped with circuitry to protect itself from excessive thermal dissipation, it is not recommended that the LM9076Q be operated at, or near, the maximum recommended die junction temperature (T_J) as this may impair long term device reliability.

The thermal protection circuitry monitors the temperature at the die level. When the die temperature exceeds typically 160°C the voltage regulator output will be switched off.

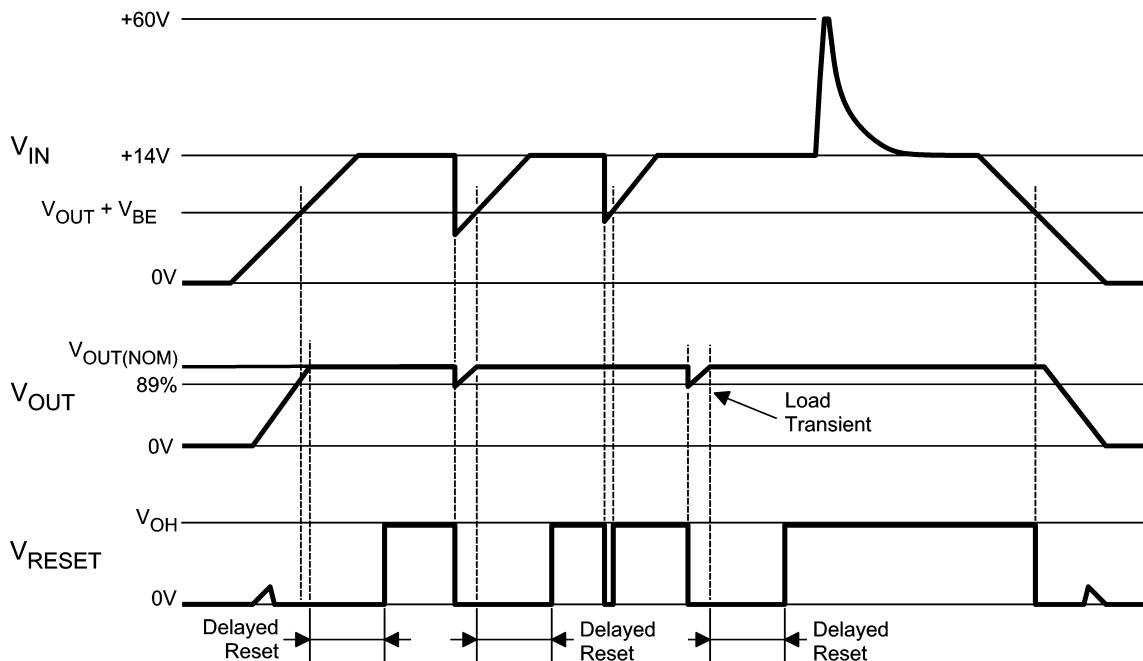


Figure 25. Typical $\overline{\text{Reset}}$ Pin Operational Waveforms

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9076QBMA-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B QMA3.3	Samples
LM9076QBMA-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B QMA5.0	Samples
LM9076QBMAX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B QMA3.3	Samples
LM9076QBMAX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B QMA5.0	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

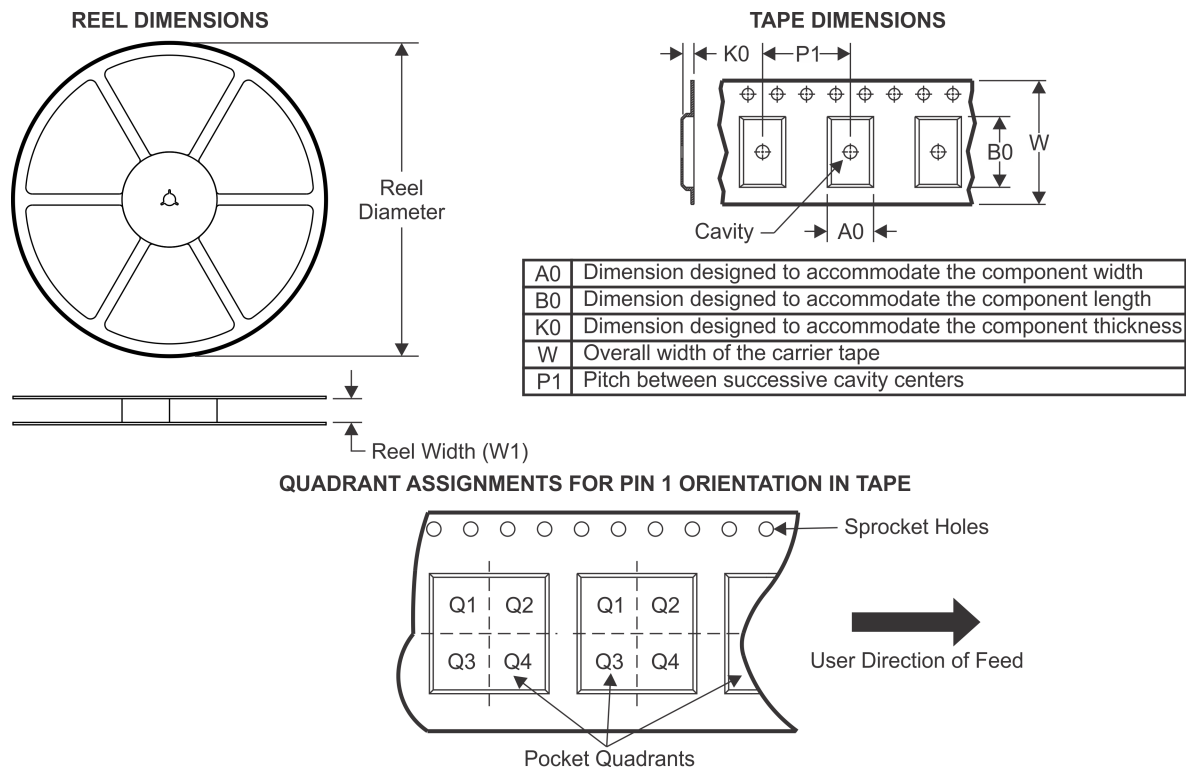
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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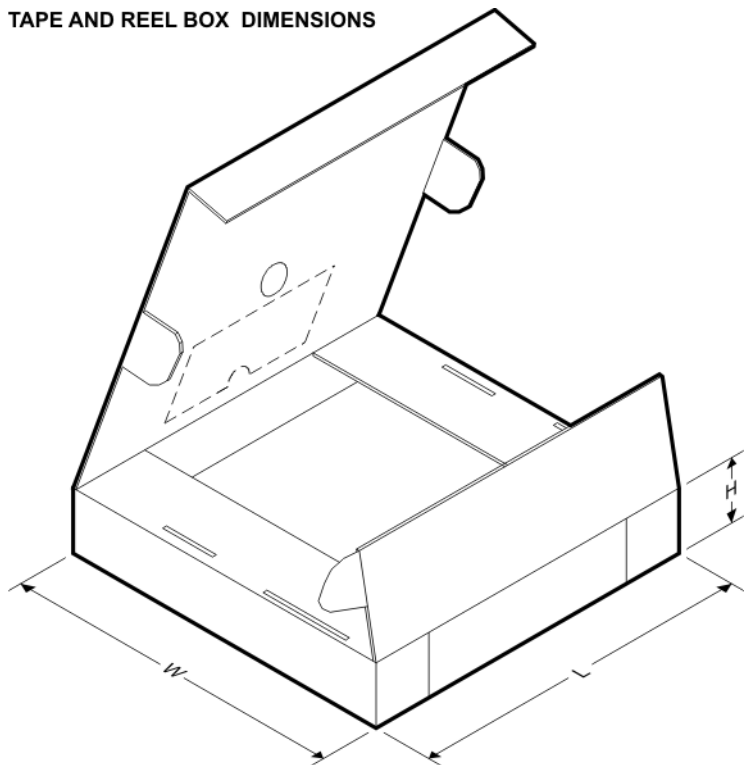
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TAPE AND REEL INFORMATION


*All dimensions are nominal

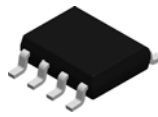
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9076QBMAX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9076QBMAX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9076QBMAX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9076QBMAX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

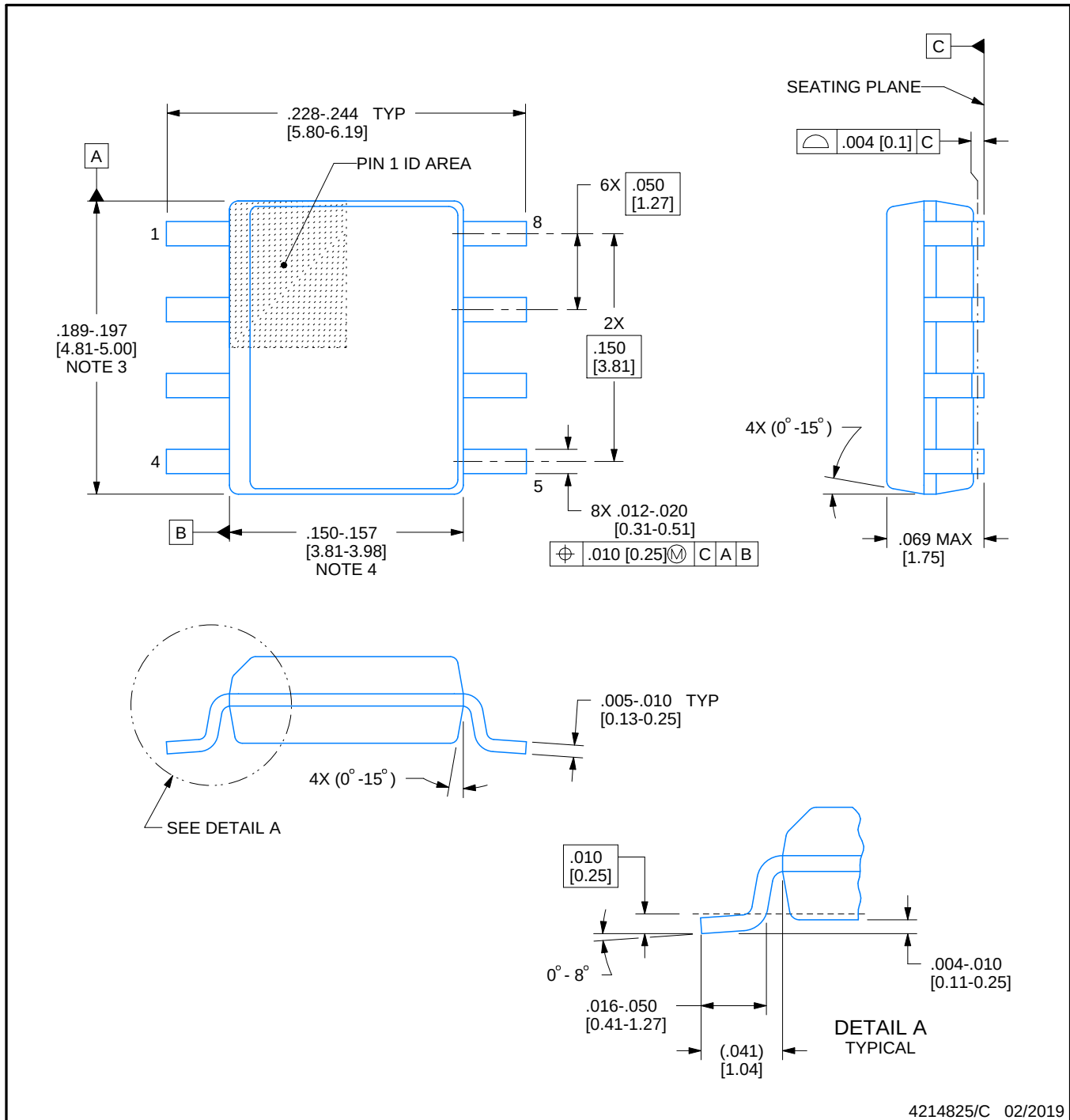


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

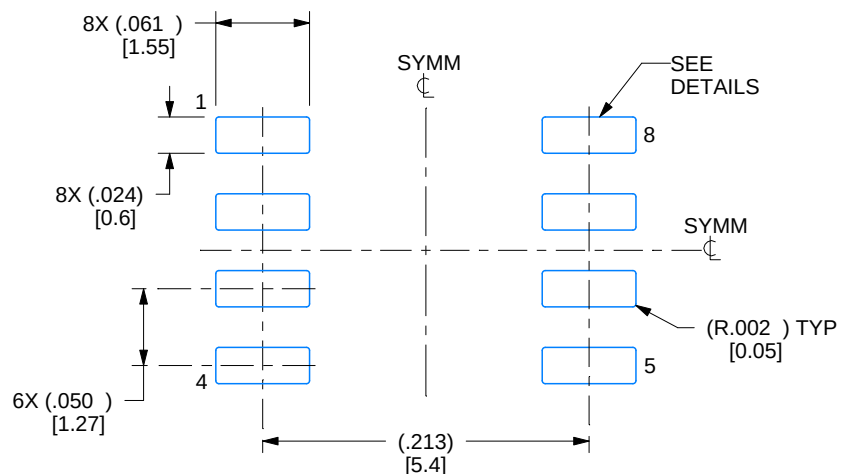
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

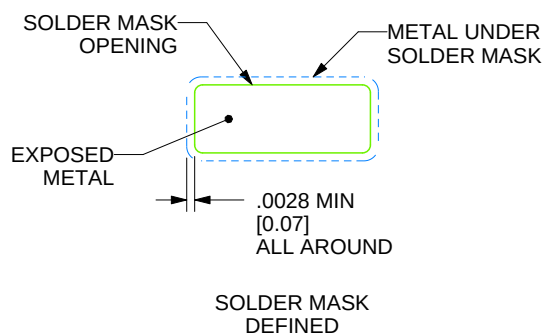
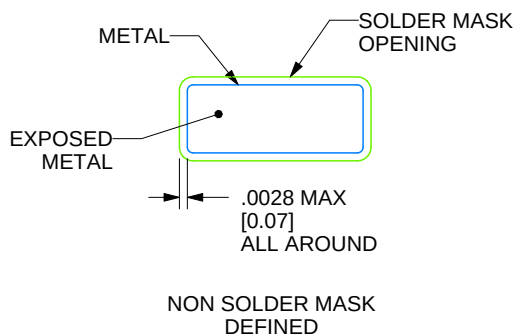
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

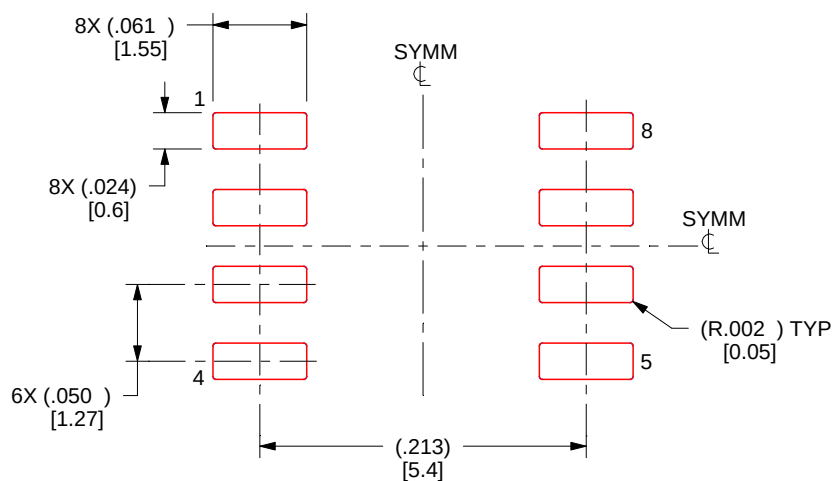
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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