TLC59731
3-Channel, 8-Bit, PWM LED Driver With Single-Wire Interface (EasySet)

1 Features

- Three Sink Current Channels
- Current Capability:
  - 50 mA per Channel
- Grayscale (GS) Control With PWM:
  - 8-Bit (256 Steps) With Simple Gamma Correction
- Single-Wire Interface (EasySet™)
- Power-Supply (VCC) Voltage Range:
  - No Internal Shunt Regulator Mode: 3 V to 5.5 V
  - Internal Shunt Regulator Mode: 3 V to 6 V
- OUT Terminals Maximum Voltage: Up to 21 V
- Integrated Shunt Regulator
- Data Transfer Maximum Rate:
  - Bits per Second (bps): 600 kbps
- Internal GS Clock Oscillator: 6 MHz (Typical)
- Display Repeat Rate: 3.1 kHz (Typical)
- Output Delay Switching to Prevent Inrush Current
- Unlimited Device Cascading
- Operating Temperature: –40°C to 85°C

2 Applications

RGB LED Cluster Lamp Displays

3 Description

The TLC59731 device is an easy-to-use, 3-channel, 50-mA sink current LED driver. The single-wire, 600-kbps serial interface (EasySet) provides a solution for minimizing wiring cost. The LED driver provides 8-bit pulse width modulation (PWM) resolution and a simple gamma correction feature. The display repeat rate is achieved at 3.1 kHz (typical) with an integrated 6-MHz grayscale (GS) clock oscillator. The driver also provides unlimited cascading capability.

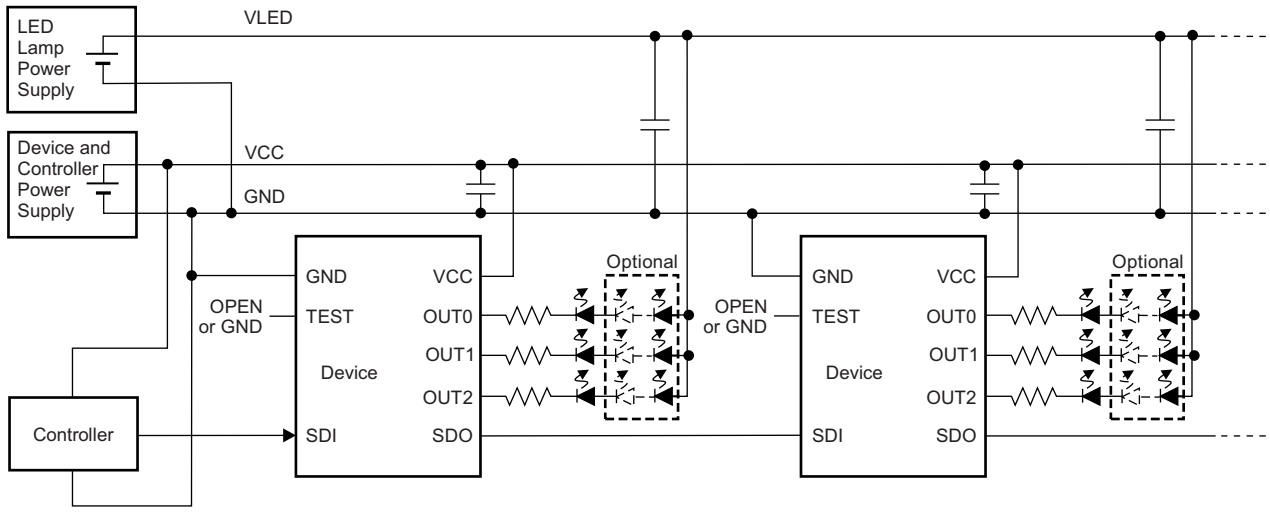
Output sink current can be set by each external resistor connected to the OUT*n* terminal in series. The TLC59731 has an internal shunt regulator that can be used for higher VCC power-supply voltage applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59731	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit Example (No Internal Shunt Regulator Mode)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C — **Page**

- Deleted *Constant Sink Current Value* section ... 12
- Changed the *Grayscale (GS) Control* description for clarity ... 13
- Changed *Grayscale (GS) Function (PWM Control)* section: corrected number of bits throughout section and corrected Table 2 accordingly ... 14
- Added 2nd sentence to 3rd paragraph of *Grayscale (GS) Function (PWM Control)* section ... 14
- Changed the *PWM Control* section to account for a 24-bit GS data latch instead of a 36-bit data latch ... 15
- Deleted the *One-Wire Interface (EasySet) Data Writing Method* section from the *Device Functional Modes* ... 15

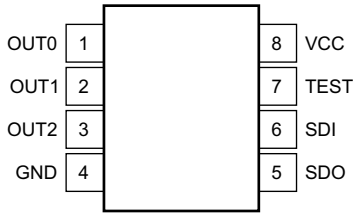
Changes from Revision A (April 2013) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Grayscale (GS) Control*, *EasySet and Shunt Regulator*, and *No Limit Cascading* sections ... 13
- Changed *Connector Design* title ... 13
- Changed Figure 12: changed OUT*n* traces GSDATA = 4093 and GSDATA = 4094 ... 15

Changes from Original (February 2013) to Revision A **Page**

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	4	—	Power ground
OUT0	1	O	Sink driver outputs. Multiple outputs can be configured in parallel to increase the sink drive current capability. Different voltages can be applied to each output.
OUT1	2	O	
OUT2	3	O	
SDI	6	I	Serial data input. This pin is internally pulled down to GND with a 1-MΩ (typical) resistor.
SDO	5	O	Serial data output
TEST	7	—	TI internal test terminal. This pin must be connected to GND or left open.
VCC	8	—	Power-supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage(2)	Supply, V_{CC}	VCC	–0.3	7.0	V
	Input, V_{IN}	SDI	–0.3	V_{CC} + 1.2	
	Output, V_{OUT}	OUT0 to OUT2	–0.3	21	
		SDO	–0.3	7.0	
Current	Output (DC), I_{OUT}	OUT0 to OUT2	0	60	mA
Temperature	Operating junction, T_J		–40	150	°C
	Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply voltage	No internal shunt regulator mode	3.0	5	5.5	V
		Internal shunt regulator mode			6	
V_O	Voltage applied to output	OUT0 to OUT2			21	V
V_{IH}	High-level input voltage	SDI	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SDI	GND		0.3 × V_{CC}	V
V_{IHYST}	Input voltage hysteresis	SDI		0.2 × V_{CC}		V
I_{OH}	High-level output current	SDO			–2	mA
I_{OL}	Low-level output current	SDO			2	mA
		OUT0 to OUT2			50	
I_{REG}	Shunt regulator sink current	VCC			20	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC CHARACTERISTICS						
$f_{CLK\ (SDI)}$	Data transfer rate	SDI	20		600	kHz
t_{SDI}	SDI input pulse duration	SDI	275		0.5 / f_{CLK}	ns
t_{WH}	Pulse duration, high	SDI	14			ns
t_{WL}	Pulse duration, low	SDI	14			ns
t_{H0}	Hold time: end of sequence (EOS)	SDI↑ to SDI↑	3.5 / f_{CLK}		5.5 / f_{CLK}	µs
t_{H1}	Hold time: data latch (GSLAT)	SDI↑ to SDI↑	8 / f_{CLK}			µs

6.4 Thermal Information

THERMAL METRIC[1]		TLC59731 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

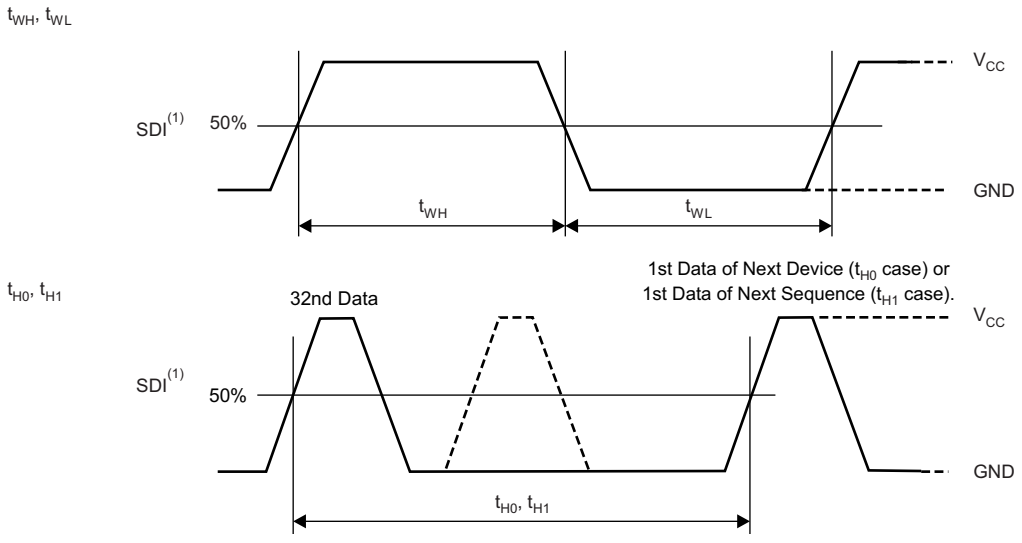
At T_A = –40°C to +85°C, V_{CC} = 3 V to 6.0 V, and C_{VCC} = 0.1 µF. Typical values at T_A = 25°C and V_{CC} = 5.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (SDO)	I_{OH} = –2 mA		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage (SDO)	I_{OL} = 2 mA		0		0.4	V
V_R	Shunt regulator output voltage (V_{CC})	I_{CC} = 1 mA, SDI = low			5.9		V
I_{CC0}	Supply current (V_{CC})	V_{CC} = 3 V to 5.5 V, SDI = low, all grayscale (GS*n*) = FFh, V_{OUTn} = 0.6 V, SDO = 15 pF			2.3	3.5	mA
I_{CC1}		V_{CC} = 3 V to 5.5V , SDI = 600 kHz, GS*n* = FFh, V_{OUTn} = 0.6 V, SDO = 15 pF			2.6	4.5	
I_{OL}	LED output current (OUT0 to OUT2)	All OUT*n* = on, V_{OUTn} = 0.6 V		32	40		mA
I_{OLKG}	Output leakage current (OUT0 to OUT2)	GS*n* = 00h, V_{OUTn} = 21 V	T_J = –40°C to +85°C			0.1	µA
			T_J = +85°C to +125°C			0.2	
R_{PD}	Internal pulldown resistance (SDI)	At SDI			1		MΩ

6.6 Switching Characteristics

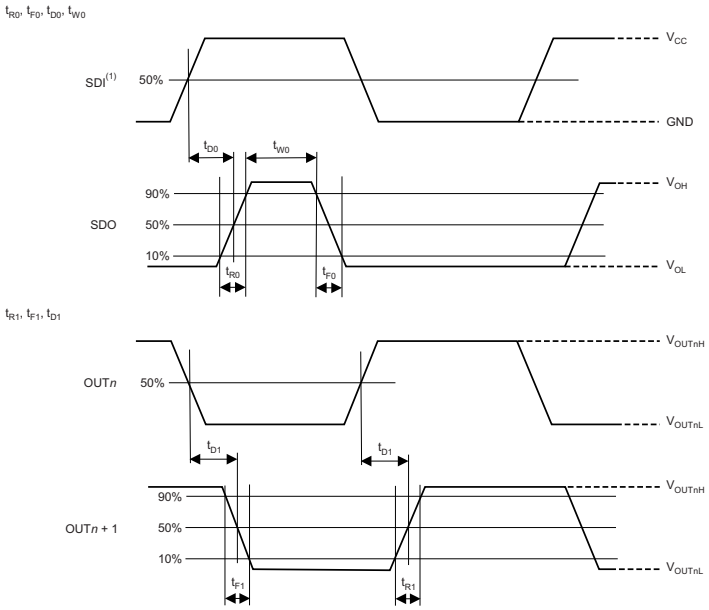
At T_A = –40°C to 85°C, V_{CC} = 3.0 V to 5.5 V, C_L = 15 pF, R_L = 110 Ω, and V_{LED} = 5 V, unless otherwise noted. Typical values are at T_A = 25°C and V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{R0}	Rise time	SDO	2	6	12	ns
t_{R1}		OUT*n* (on → off)		200	400	ns
t_{F0}	Fall time	SDO	2	6	12	ns
t_{F1}		OUT*n* (off → on)		200	400	ns
t_{D0}	Propagation delay	SDI↑ to SDO↑		30	50	ns
t_{D1}		OUT0↓ to OUT1↓, OUT1↓to OUT2↓, OUT0↑ to OUT1↑, OUT1↑to OUT2↑		25		ns
t_{WO}	Shift data output one pulse duration	SDO↑ to SDO↓	75	125	250	ns
f_{OSC}	Internal GS oscillator frequency		4	6	8	MHz



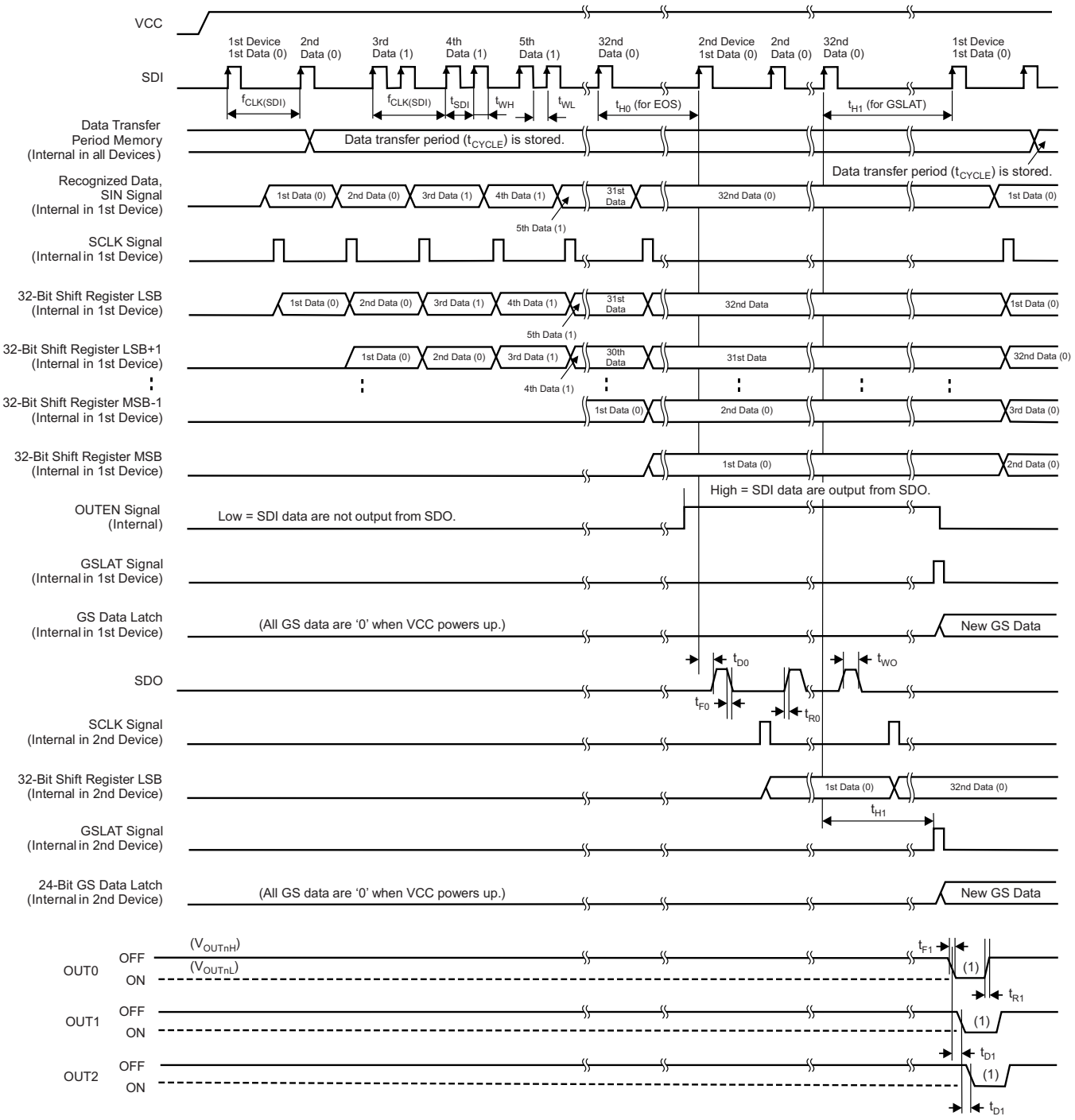
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 1. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 2. Output Timing



(1) OUT*n* ON-time changes, depending on the data in the 24-bit GS data latch.

Figure 3. Data Write and Out*n* Switching Timing

6.7 Typical Characteristics

at T_A = 25°C and V_{CC} = 12 V (unless otherwise noted)

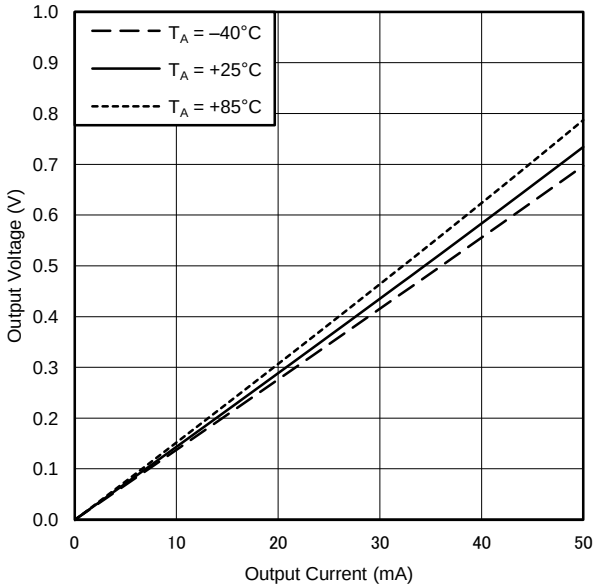


Figure 4. Output Current vs Output Voltage (Out*n*)

7 Parameter Measurement Information

7.1 Pin-Equivalent Input and Output Schematic Diagrams

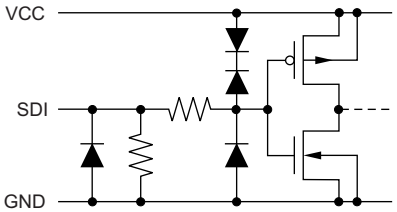


Figure 5. SDI

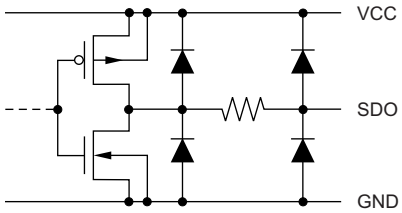
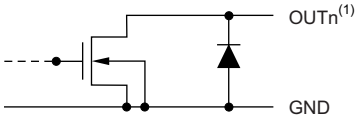


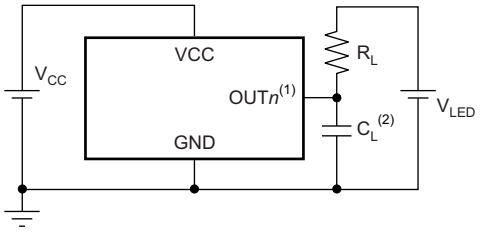
Figure 6. SDO



(1) n = 0 to 2.

Figure 7. OUT0 Through OUT2

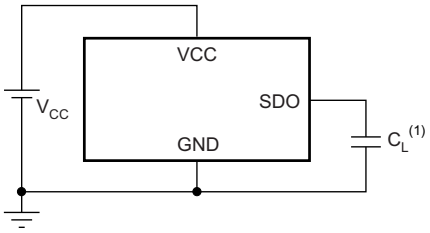
7.2 Test Circuits



(1) n = 0 to 2.

(2) C_L includes measurement probe and jig capacitance.

Figure 8. Rise Time and Fall Time Test Circuit for Out*n*



(1) C_L includes measurement probe and jig capacitance.

Figure 9. Rise Time and Fall Time Test Circuit for SDO

8 Detailed Description

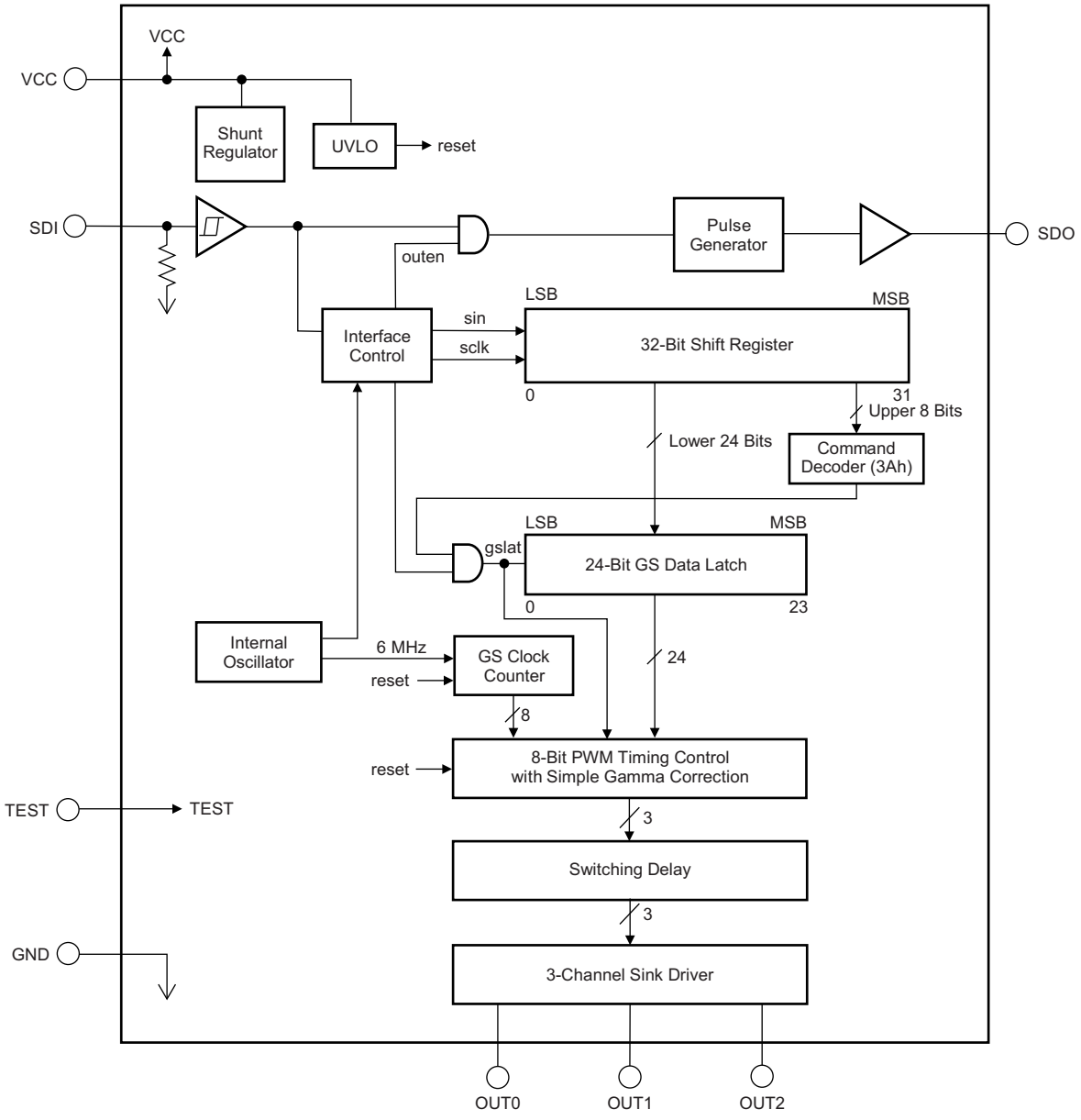
8.1 Overview

The TLC59731 is a 3-channel constant-current sink driver. Each channel has an individually-adjustable, 256-step, pulse-width modulation (PWM) grayscale (GS) brightness control. GS data are input through a serial single-wire interface port.

The TLC59731 has a 50-mA current capability. The maximum current value of each channel is determined by the external resistor. The TLC59731 can function without external CLK signals because the device is integrated with a 6-MHz internal oscillator.

The TLC59731 is integrated with a shunt regulator that can be used for higher VCC power-supply voltage applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Sink Current Value Setting

The typical sink current value of each channel (I_{OUTn}) can be set by resistor (R_{Ln}) that is placed between the LED cathode and OUT*n* pins; see Figure 10. The typical sink current value can be calculated by Equation 1 and the typical resistor value can be calculated by Equation 2.

$$I_{OUTn}\,(mA) = \frac{V_{LED}\,(V) - V_{F\_TOTAL}\,(V) - V_{OUTn}\,(V)}{R_{Ln}\,(\Omega)} \quad (1)$$

where

- n = 0 to 2

$$R_{Ln}\,(\Omega) = \frac{V_{LED}\,(V) - V_{F\_TOTAL}\,(V) - V_{OUTn}\,(V)}{I_{OUTn}\,(mA)} \quad (2)$$

where

- n = 0 to 2
- V_{LED} = the LED anode voltage
- V_{F_TOTAL} = the total LED forward voltage
- V_{OUTn} = the OUT*n* output voltage

Note that the typical V_{OUTn} value is 0.6 V with a 40-mA output current, as shown in Figure 4.

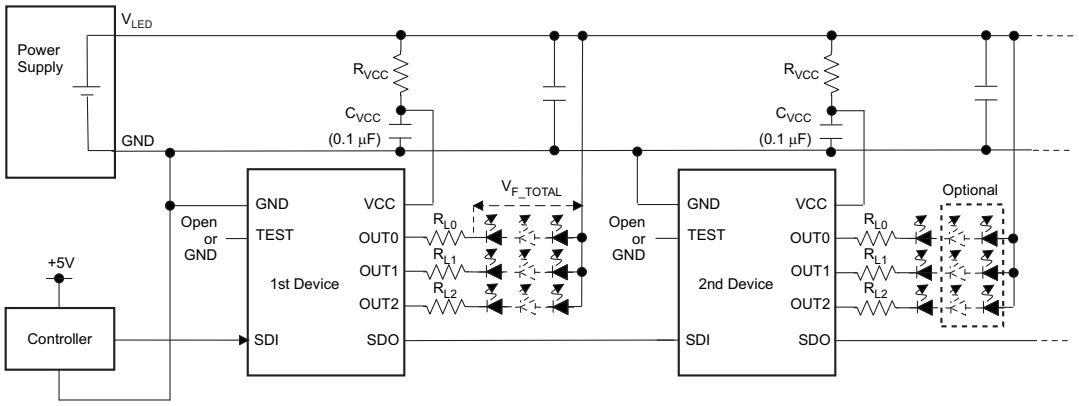


Figure 10. Internal Shunt Regulator Mode Application Circuit

8.3.2 Resistor and Capacitor Value Setting for Shunt Regulator

The TLC59731 internally integrates a shunt regulator to regulate V_{CC} voltage. Figure 4 shows an application circuit that uses the internal shunt regulator through a resistor, R_{VCC}. The recommended R_{VCC} value can be calculated by Equation 3.

$$\frac{V_{LED}\,(V) - 5.9\ V}{8\ mA} < R_{VCC} < \frac{V_{LED}\,(V) - 5.9\ V}{6\ mA} \quad (3)$$

Table 1 shows the typical resistor value for several V_{LED} voltages. Note that the C_{VCC} value must be 0.1 µF.

Table 1. Resistor Example for Shunt Resistor Versus LED Voltage

V_{LED} (V)	R_{VCC} (Ω)	RESISTOR WATTAGE (W)
9	470	0.02
12	910	0.04
18	1800	0.08
24	2700	0.12

8.3.3 Grayscale (GS) Control

This control feature is an 8-bit (256-step) grayscale (GS) control that provides a wide range of color generation. Connect the LEDs to the device OUT*n* pins, as described in the *Layout Guidelines* section.

8.3.4 EasySet and Shunt Regulator

This device includes a single-wire serial interface (EasySet) and a shunt regulator. The total number of wires for power supply and data write operations can be reduced with the EasySet and shunt regulator included in the design.

8.3.5 No Limit Cascading

This feature results in no limitation on the number of total cascaded devices used in series in an application. This advantage is attained because a timing-adjusted pulse generator is implemented in the device.

8.3.6 Connector Design

When the connector pin of the device application printed circuit board (PCB) is connected or disconnected to other PCBs, the power must be turned off to avoid device malfunction or failure. Furthermore, designing the connector GND pin to be longer than other pins (as shown in Figure 11) is preferable. This arrangement allows the GND line to either be connected first or disconnected last, which is imperative for proper device function.

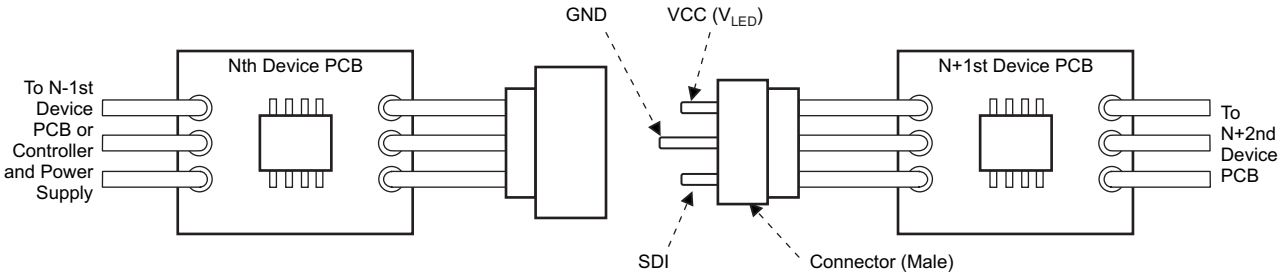


Figure 11. Connector Pin Design Application

8.4 Device Functional Modes

8.4.1 Grayscale (GS) Function (PWM Control)

The TLC59731 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The PWM data bit length for each output is 8 bits. The architecture of 8 bits per channel results in 256 brightness steps, from 0% to 99.98% ON-time duty cycle.

The PWM operation for OUT*n* is controlled by an 8-bit grayscale (GS) counter. The GS counter increments on each internal GS clock (GSCLK) rising edge. All OUT*n* are turned on when the GS count is '1', except when OUT*n* are programed to GS data '0' in the 24-bit GS data latch. After turning on, each output turns off when the GS counter value exceeds the programmed GS data for the output. The GS counter resets to 00h and all outputs are forced off when the GS data are written to the 24-bit GS data latch. Afterwards, the GS counter begins incrementing and PWM control is started from the next internal GS clock.

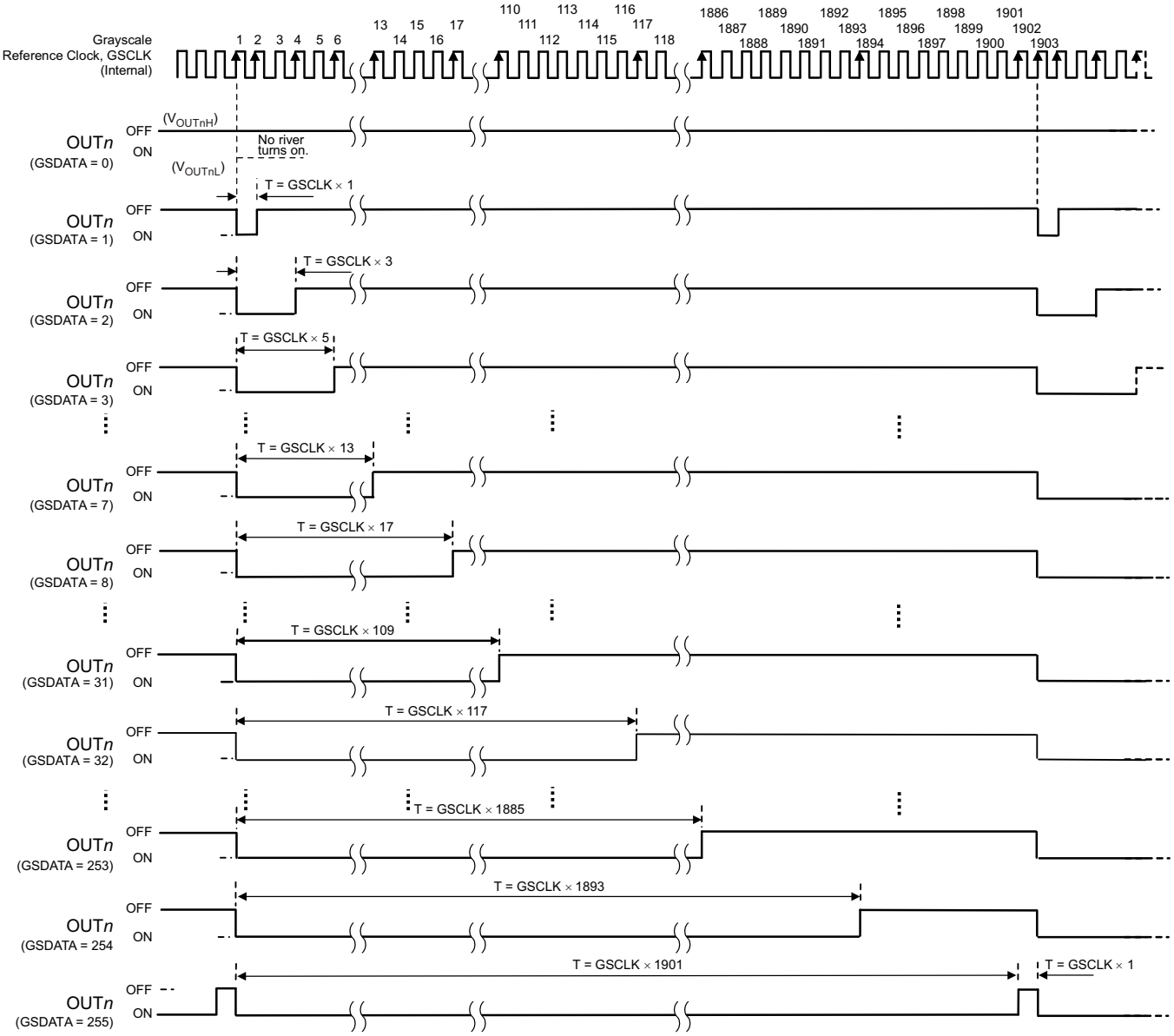
Table 2 summarizes the GS data values versus the output ideal ON-time duty cycle. The on-time duty cycle is not proportional to the GS data because a simple gamma correction is implemented in the TLC59731. Furthermore, actual ON-time differs from the ideal ON-time because the output drivers and control circuit have some timing delay. When the device is powered on, all outputs are forced off and remain off until the non-zero GS data are written to the 24-bit GS data latch.

Table 2. Output Duty Cycle and Total ON-Time vs GS Data

GS DATA		NO. OF GSCLKs OUT*n* TURNS ON	NO. OF GSCLKs OUT*n* TURNS OFF	TOTAL IDEAL TIME (µs)	ON-TIME DUTY (%)
DECIMAL	HEX				
0	0	Off	Off	0	0
1	1	1	2	0.08	0.02
2	2	1	4	0.17	0.05
3	3	1	6	0.8	0.3
—	—	—	—	—	—
6	6	1	12	1.8	0.6
7	7	1	14	2.2	0.7
8	8	1	18	2.8	0.9
9	9	1	22	3.5	1.1
10	10	1	26	4.2	1.3
—	—	—	—	—	—
30	1E	1	106	17.5	5.5
31	1F	1	110	18.2	5.7
32	20	1	118	19.5	6.2
33	21	1	126	20.8	6.6
34	22	1	134	22.2	7.0
—	—	—	—	—	—
62	3E	1	358	59.5	18.8
63	3F	1	366	60.8	19.2
64	40	1	374	62.2	19.6
65	41	1	382	63.5	20.0
66	42	1	390	64.8	20.5
—	—	—	—	—	—
127	7F	1	878	146.2	46.1
128	80	1	886	147.5	46.5
129	81	1	894	148.8	47.0
—	—	—	—	—	—
253	FD	1	1886	314.2	99.1
254	FE	1	1894	315.5	99.5
255	FF	1	1902	316.8	99.9

8.4.1.1 PWM Control

The GS counter keeps track of the number of grayscale reference clocks (GSCLKs) from the internal oscillator. Each output stays on when the counter is less than or equal to the programmed GS value. Each output turns off when the GS counter is greater than the GS value in the 24-bit GS data latch. Figure 12 shows the PWM operation timing.



(1) Actual ON-time differs from the ideal ON-time.

Figure 12. PWM Operation

8.5 Programming

8.5.1 One-Wire Interface (EasySet) Data Writing Method

There are four sequences to write GS data into the TLC59731 through a single-wire interface. This section discusses each sequence in detail.

8.5.1.1 Data Transfer Rate (T_{CYCLE}) Measurement Sequence

The TLC59731 measures the time between the first and second SDI rising edges either after the device is powered up or when the GS data latch sequence is executed (as described in the *GS Data Latch Sequence (GSLAT)* section) and the time is internally stored as t_{CYCLE}. t_{CYCLE} serves as a base time used to recognize one complete data write operation, a 32-bit data write operation, and a GS data write operation to the GS data latch. t_{CYCLE} can be set between 1.66 µs and 50 µs ($f_{CLK(SDI)}$ = 20 kHz to 600 kHz). In this sequence, two instances of data 0 are written to the LSB side of the 32-bit shift register. Figure 13 shows the t_{CYCLE} measurement timing.

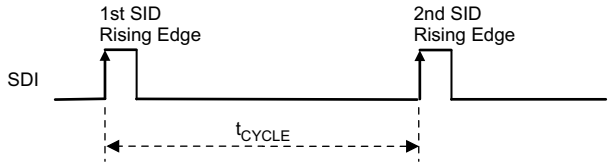


Figure 13. Data Transfer Rate (T_{CYCLE}) Measurement

8.5.1.2 Data 0 and Data 1 Write Sequence (Data Write Sequence)

When the second SDI rising edge is not input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the second rising edge is recognized as data 0. When the second SDI rising edge is input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the second rising edge is recognized as data 1. This write sequence must be repeated 30 times after the t_{CYCLE} measurement sequence to send the write command to the lower 6-bit (3Ah) and 24-bit GS data. Figure 14 shows the data 0 and 1 write timing.

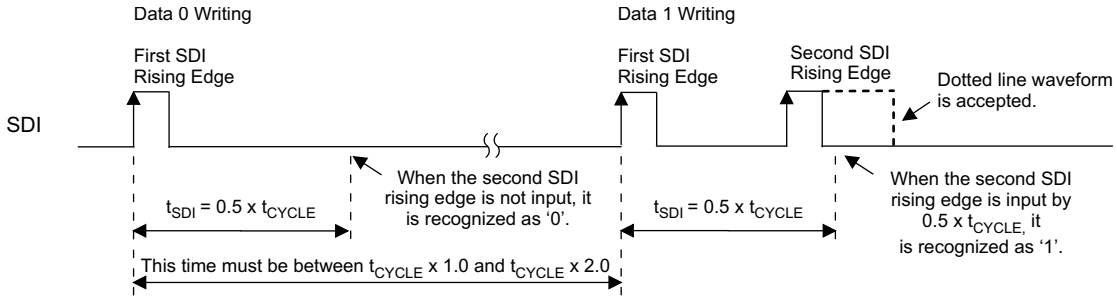


Figure 14. Data 0 and 1 Write Operation

Programming (continued)

8.5.1.3 One Communication Cycle End of Sequence (EOS)

One communication cycle end of sequence (EOS) must be input after the 32-bit data are written because the TLC59731 does not count the number of input data. When SDI is held low for the EOS hold time (t_{H0}), the 32-bit shift register values are locked and a buffered SDI signal is output from SDO to transfer GS data to the next device. Figure 15 shows the EOS timing.

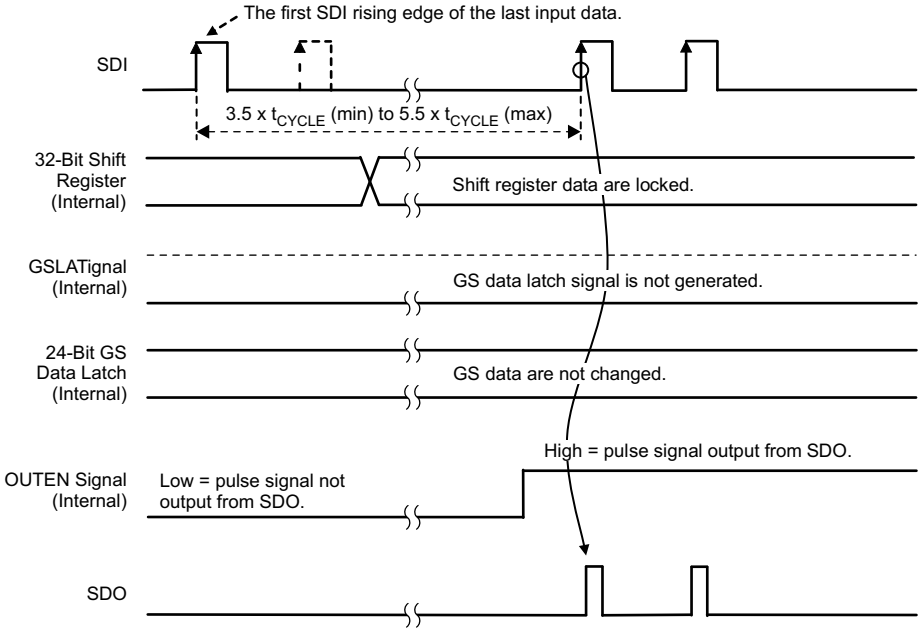


Figure 15. End of Sequence (EOS)

Programming (continued)

8.5.1.4 GS Data Latch (GSLAT) Sequence

A GS data latch (GSLAT) sequence must be input after the 32-bit data for all cascaded devices are written. When SDI is held low for the data latch hold time (t_{H1}), the 32-bit shift register data in all devices are copied to the GS data latch in each device. Furthermore, PWM control starts with the new GS data at the same time. Figure 16 shows the GSLAT timing.

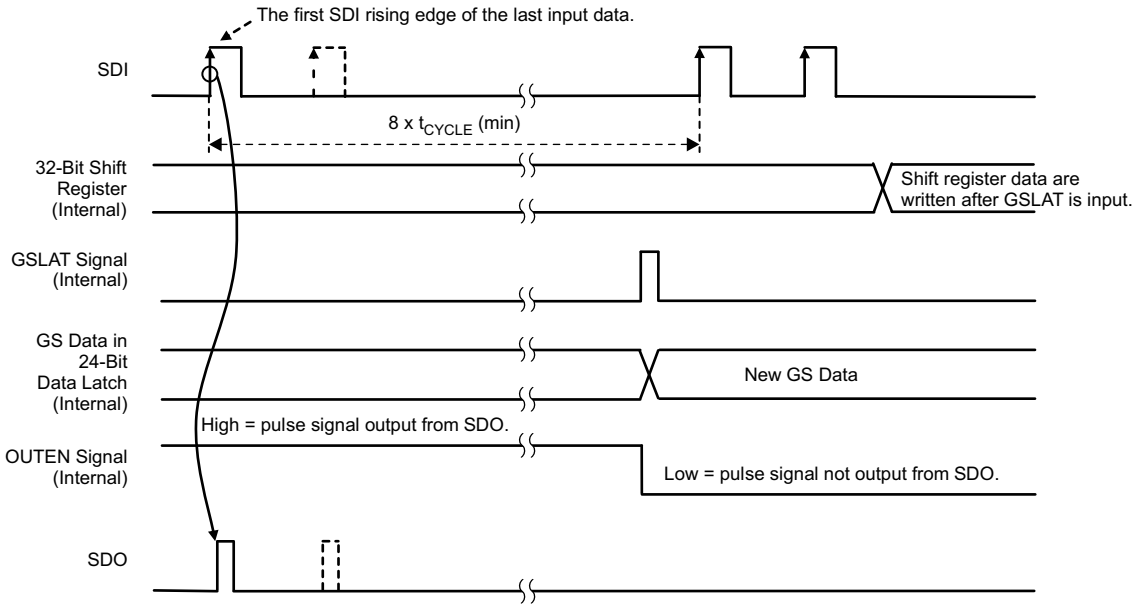


Figure 16. GS Data Latch Sequence (GSLAT)

8.5.1.5 How to Control Devices Connected in Series

The 8-bit write command and 24-bit grayscale (GS) data for OUT0 to OUT2 (for a total of 32 bits of data) must be written to the device. Figure 17 shows the 32-bit data packet configuration. When multiple devices are cascaded (see Figure 18), *N* times the packet must be written into each TLC59731 in order to control all devices. There is no limit on how many devices can be cascaded, as long as proper VCC voltage is supplied. The packet for all devices must be written again whenever any GS data changes.

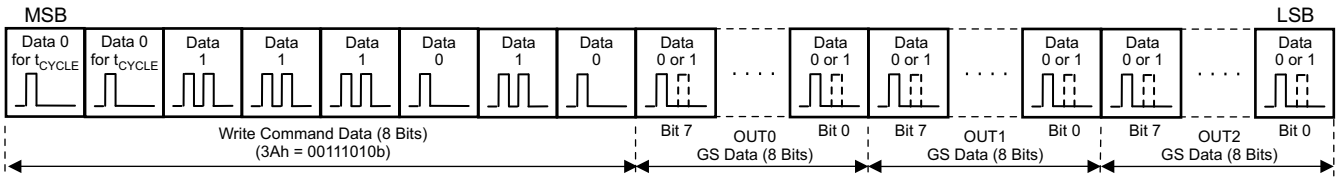


Figure 17. 32-Bit Data Packet Configuration for One TLC59731

Programming (continued)

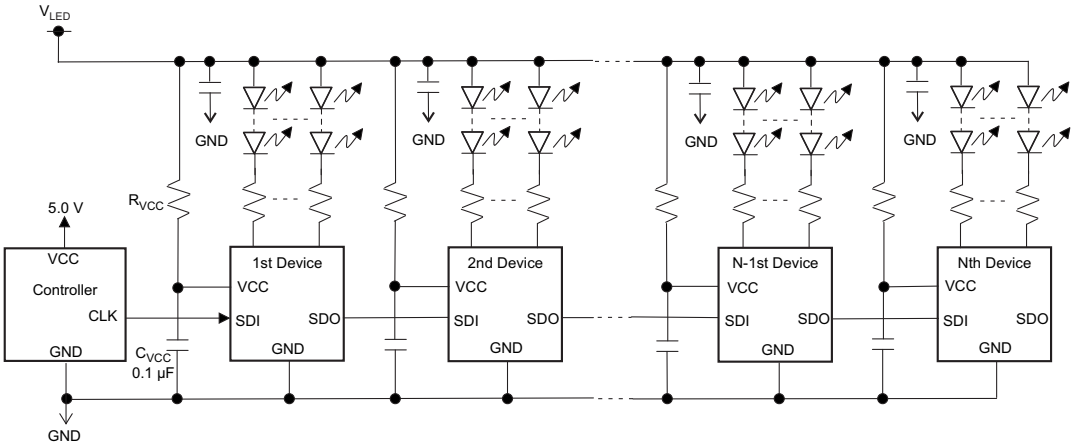


Figure 18. Cascade Connection of *N* TLC59731 Units (Internal Shunt Regulator Mode)

Figure 19 shows the 32-bit data packet, EOS, and GSLAT input timing of all devices. The function setting write procedure and display control is as follows:

1. Power up VCC (V_{LED}); all OUT*n* are off because GS data are not written yet.
2. Write the 32-bit data packet (MSB-first) for the first device using t_{CYCLE} and the data write sequences illustrated in and . The first 8-bits of the 32-bit data packet are used as the write command. The write command must be 3Ah (00111010b); otherwise, the 24-bit GS data in the 32-bit shift register are not copied to the 24-bit GS data latch.
3. Execute one communication cycle EOS (refer to) for the first device.
4. Write the 32-bit data packet for the second TLC59731 as described step 2. However, t_{CYCLE} must be set to the same timing as the first device.
5. Execute one communication cycle EOS for the second device.
6. Repeat Steps 4 and 5 until all devices have GS data.
7. The number of total bits is 32 × *N*. After all data are written, execute a GSLAT sequence as described in in order to copy the 24-bit LSBs in the 32-bit shift resister to the 24-bit GS data latch in each device; PWM control starts with the written GS data at the same time.

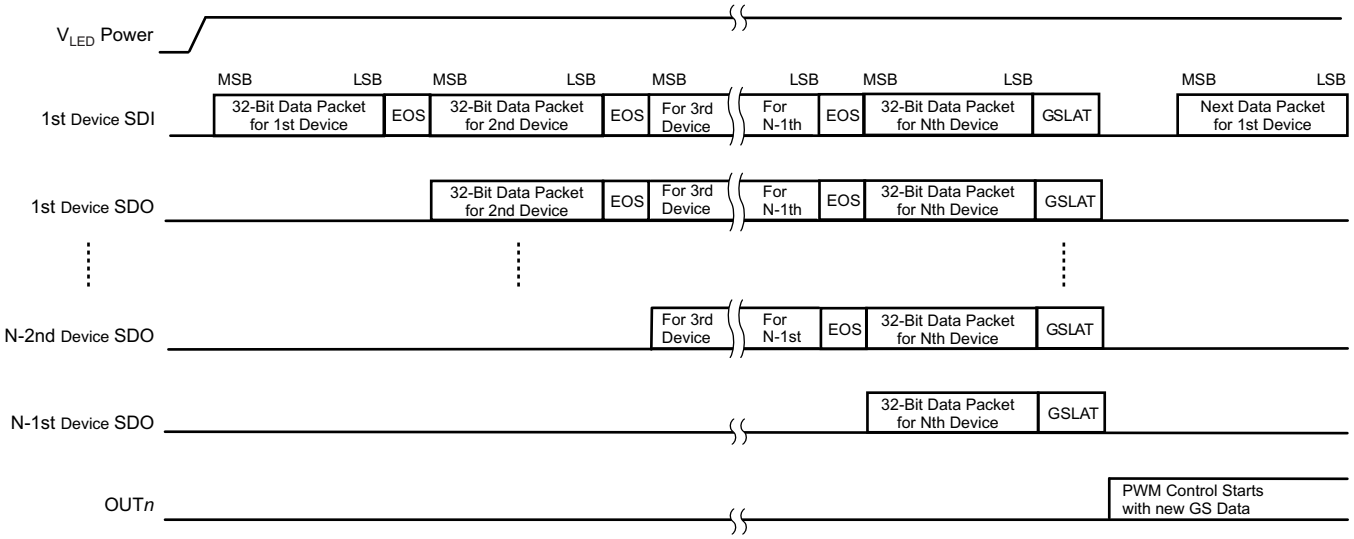


Figure 19. Data Packet Input Order for *N* TLC59731 Units

8.6 Register Maps

8.6.1 Register and Data Latch Configuration

The TLC59731 has a 32-bit shift register and a 24-bit data latch that stores GS data. When the internal GS data latch pulse is generated and the data of the eight MSBs in the shift register are 3Ah, the lower 24-bit data in the 32-bit shift register are copied into the 24-bit GS data latch. If the data of the eight MSBs is not 3Ah, the 24-bit data are not copied into the 24-bit GS data latch. Figure 20 shows the shift register and GS data latch configurations. Table 3 shows the 32-bit shift register bit assignment.

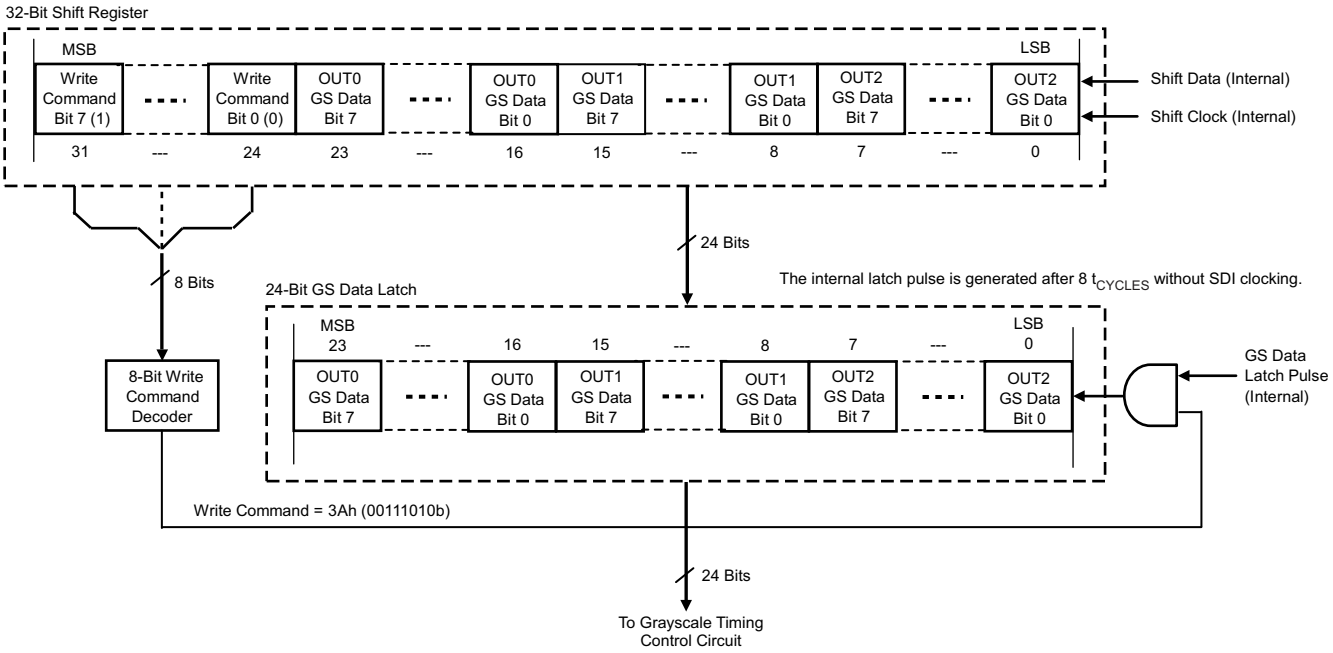


Figure 20. Common Shift Register and Control Data Latches Configuration

Table 3. 32-Bit Shift Register Data Bit Assignment

BIT	BIT NAME	CONTROLLED CHANNEL AND FUNCTIONS
0 to 7	GSOUT2	GS data bits 0 to 7 for OUT2
8 to 15	GSOUT1	GS data bits 0 to 7 for OUT1
16 to 23	GSOUT0	GS data bits 0 to 7 for OUT0
24 to 32	WRTCMD	Data write command (3Ah) for GS data. The lower 24-bit GS data in the 32-bit shift register are copied to the GS data latch when the internal GS latch is generated (when these data bits are 3Ah, *00111010b*).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a 3-channel, constant sink current, LED driver. This device can be connected in series to drive many LED lamps with only a few controller ports. Output current control data and PWM control data can be written from the SIN input terminal. The PWM timing reference clock can be supplied from the internal oscillation.

9.2 Typical Application

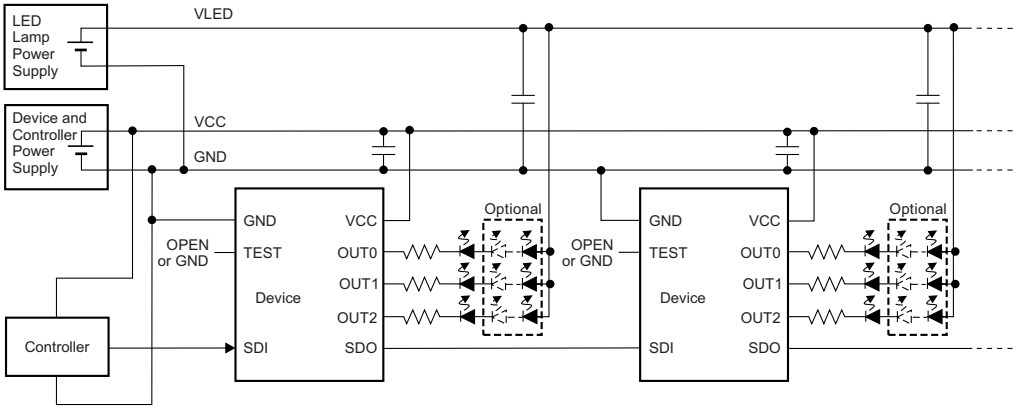


Figure 21. Typical Application Circuit Example (No Internal Shunt Regulator Mode)

9.2.1 Design Requirements

For this design example, use Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC Input Voltage Range	3 V to 5.5 V
LED Lamp (V_{LED}) Input Voltage Range	21 V Maximum
SDI Voltage Range	Low Level = GND, High Level = VCC

9.2.2 Detailed Design Procedure

9.2.2.1 Define Basic Parameters

To begin the design process, a few parameters must be decided:

- Maximum output constant-current value for each color LED lamp
- Maximum LED forward voltage (Vf) and Maximum V_{LED}
- Total LEDs and Cascaded IC Number

9.2.2.2 Grayscale (GS) Data

32-bit GS data packets are sent through single-wire interface for the PWM control of three output channels. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

9.2.3 Application Curve

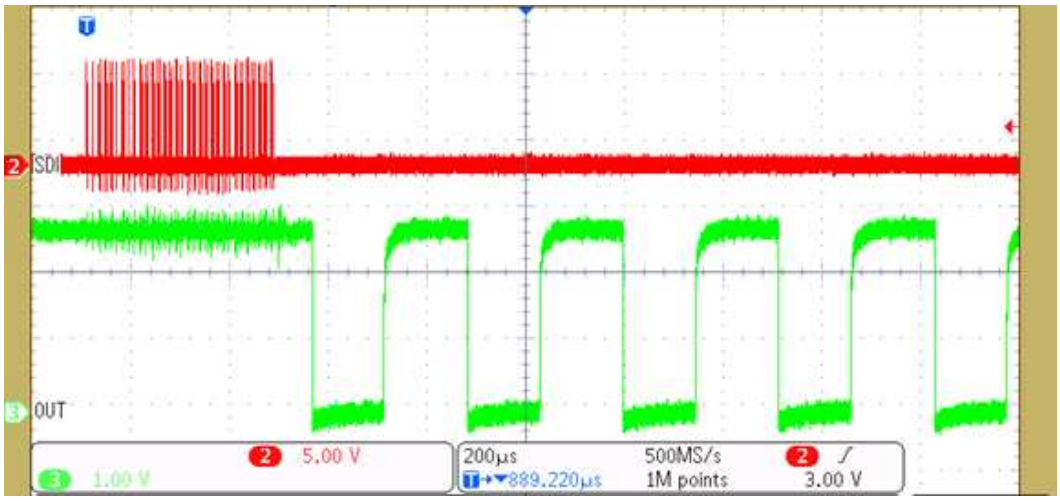


Figure 22. Output Waveform Without GS Data Latch Input

9.3 System Examples

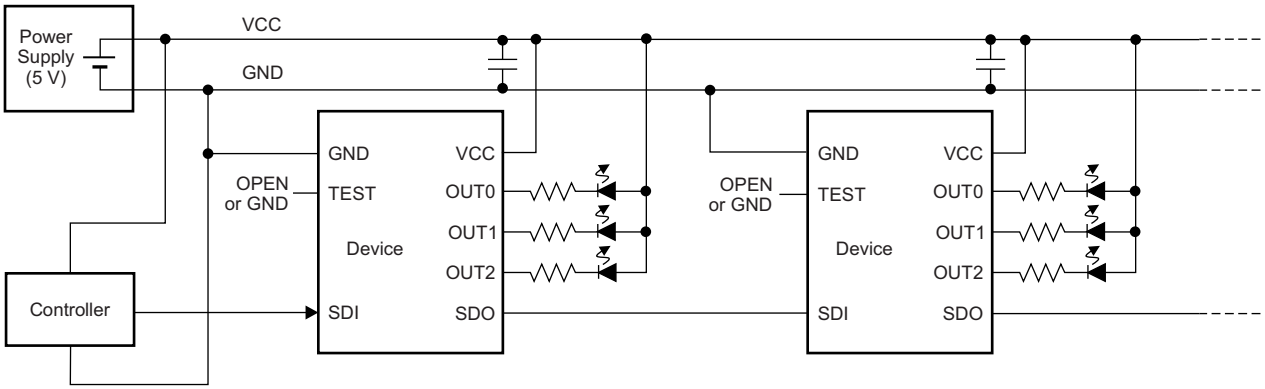


Figure 23. Typical Application Circuit Example (No Internal Shunt Regulator Mode)

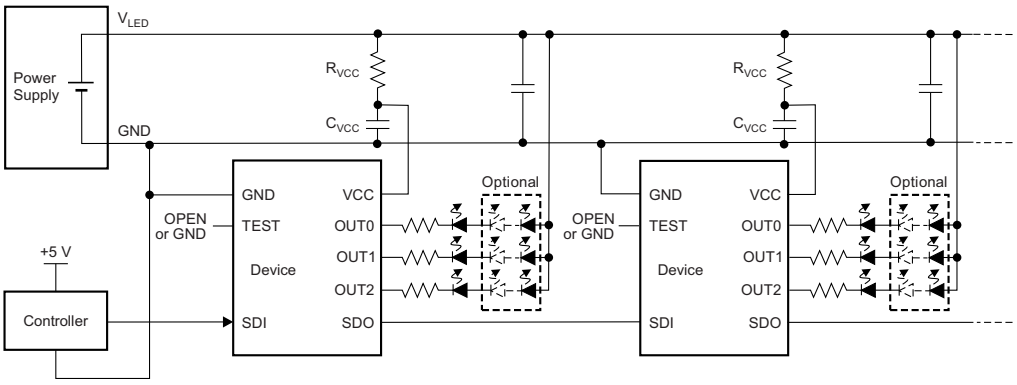


Figure 24. Typical Application Circuit Example (Internal Shunt Regulator Mode)

9.4 Do's and Don'ts

When the connector pin of the device application printed-circuit-board (PCB) is connected or disconnected to other PCBs, the power must be turned off to avoid device malfunction or failure. Furthermore, designing the connector GND pin to be longer than other pins (as shown in Figure 25) is preferable. This arrangement allows the GND line to either be connected first or disconnected last, which is imperative for proper device function.

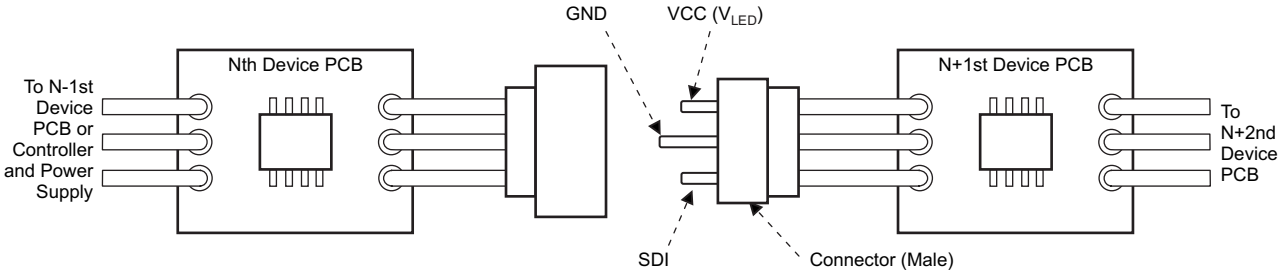


Figure 25. Connector Pin Design Application

10 Power Supply Recommendations

Decouple the V_{cc} power supply voltage by placing a 0.1-µF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on board equally distributed to get a well regulated LED supply voltage (V_{LED}). V_{LED} voltage ripple must be less than 5% of its nominal value.

11 Layout

11.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC pin and GND plane.
2. Route the GND pattern as widely as possible for large GND currents.
3. Routing wire between the LED cathode side and the device OUTn pin must be as short and straight as possible to reduce wire inductance.
4. When several ICs are chained, symmetric placements are recommended.

11.2 Layout Example

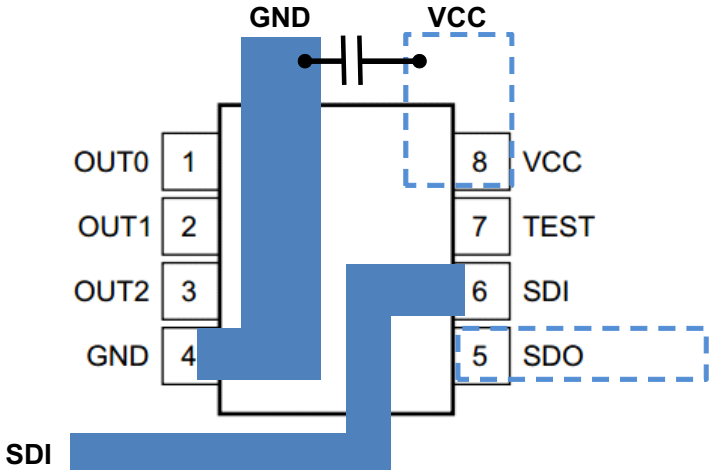


Figure 26. Layout Recommendation

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

EasySet, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59731D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59731	Samples
TLC59731DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59731	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

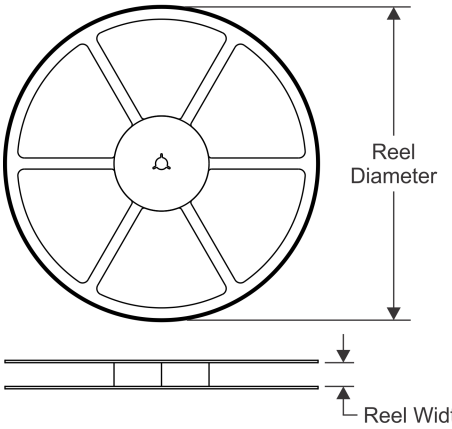
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

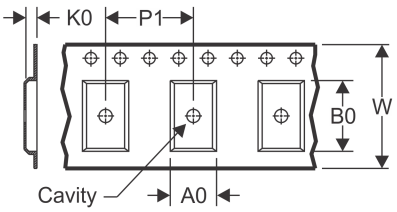
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

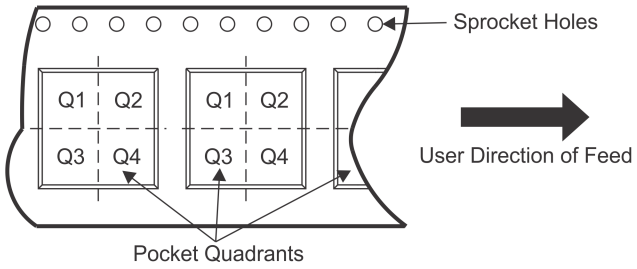


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

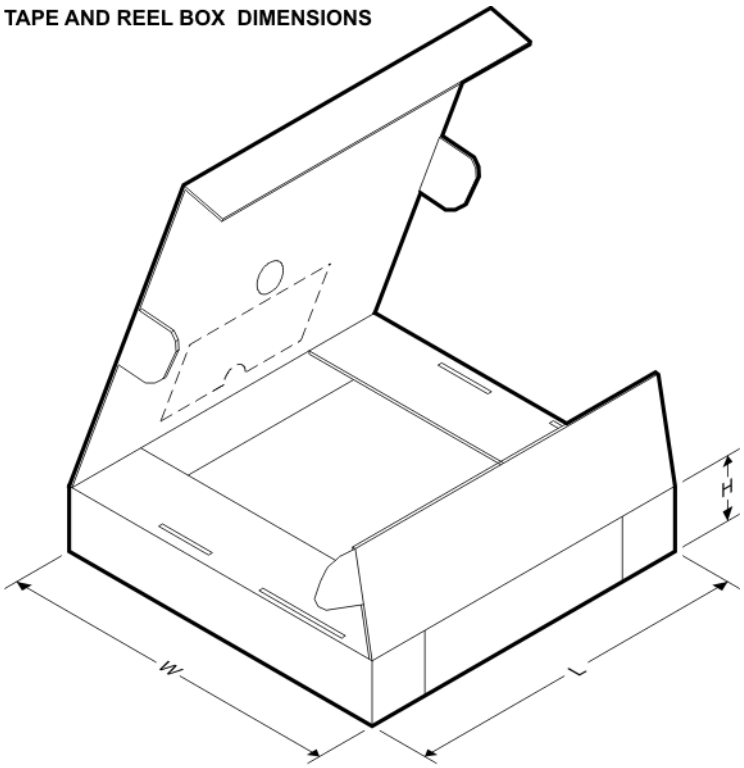
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

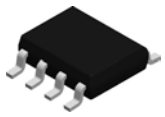
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59731DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59731DR	SOIC	D	8	2500	340.5	338.1	20.6

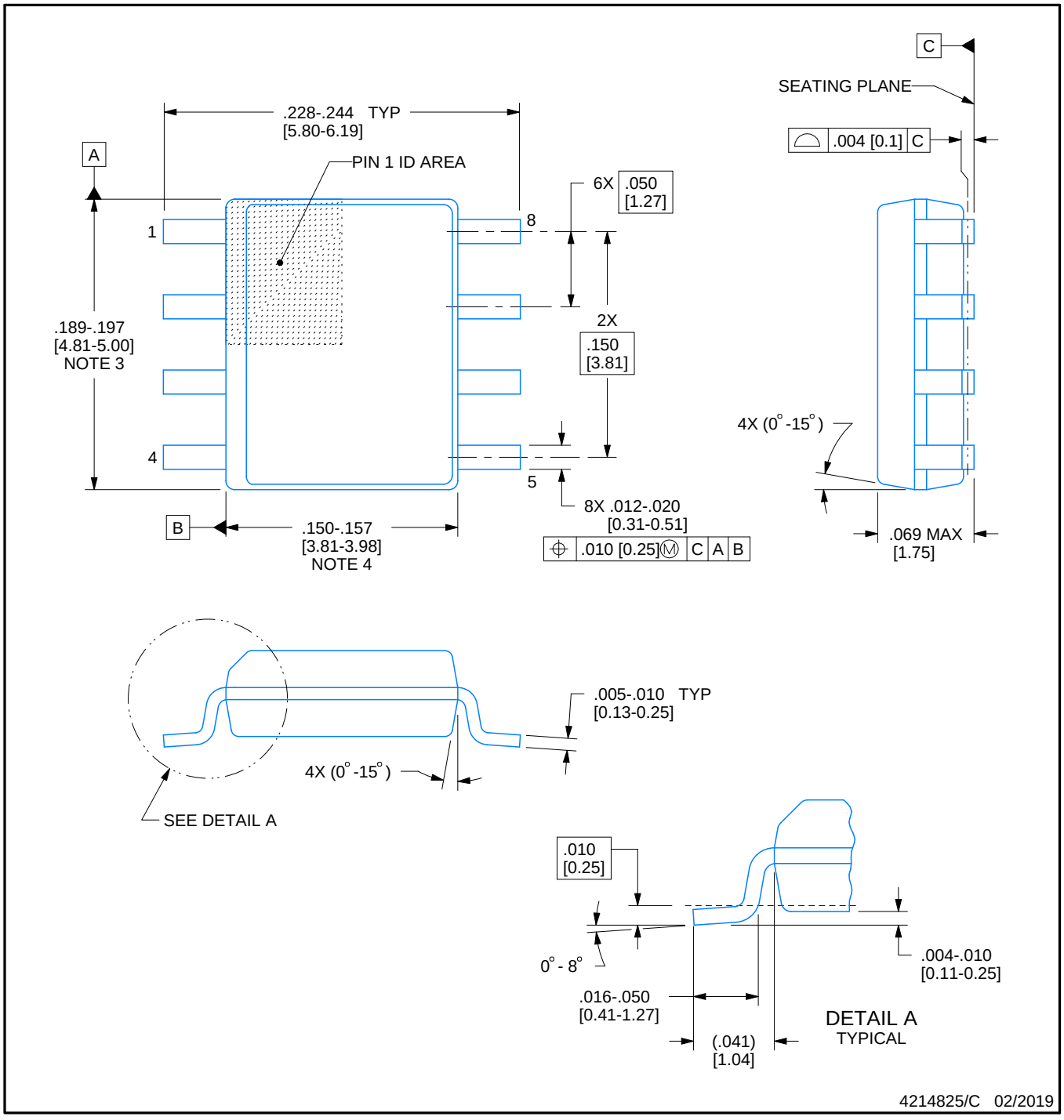


PACKAGE OUTLINE

D0008A

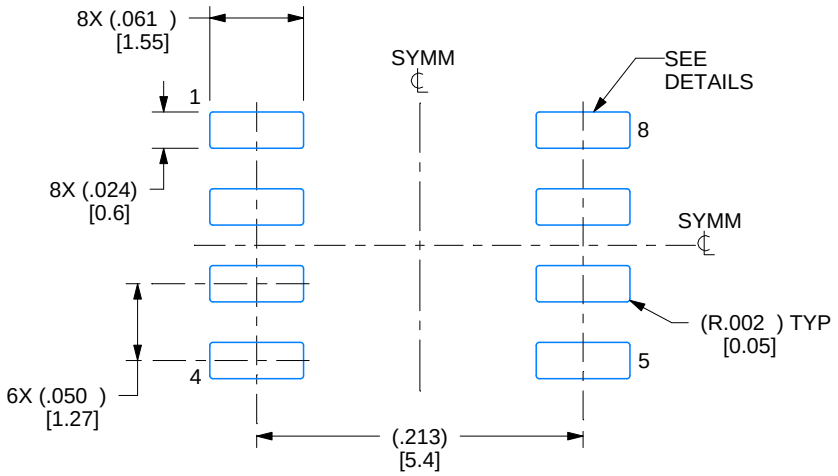
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

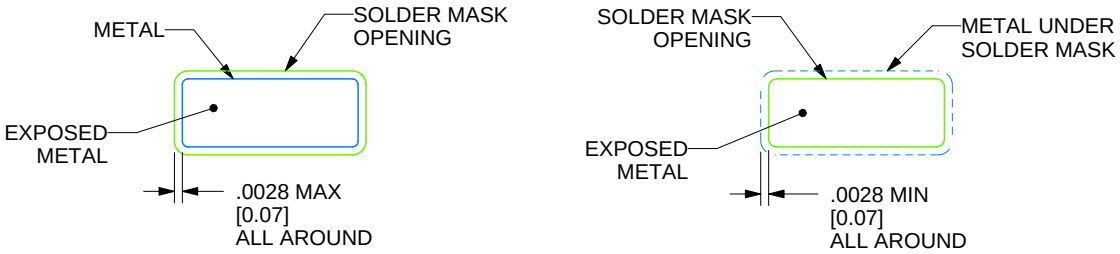


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

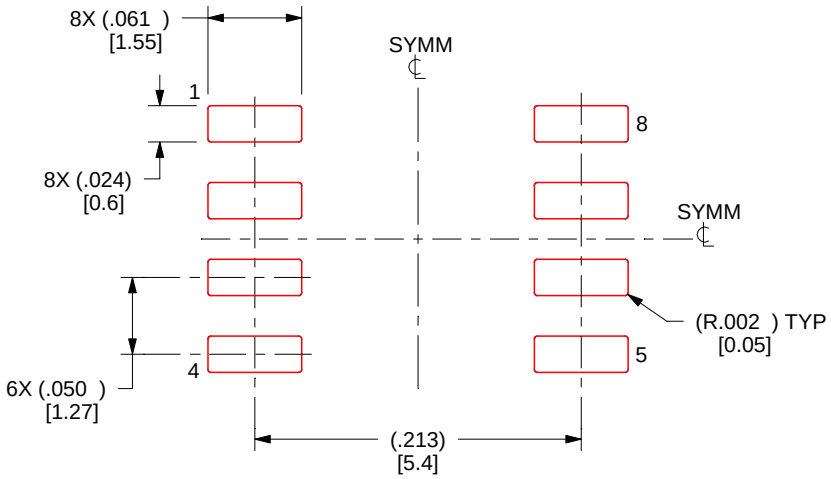
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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