AN083—Hot Swap Device

MP5022A Design Notes

Application Note

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ABSTRACT

MP5022A is an update version of MP5022. It is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output.

At start up, in-rush current is limited by the slew rate at the output. The maximum load at the output is current limited through a sense FET topology. The magnitude of the current limit is controlled by a resistor from the ISET pin to ground. The MP5022A on resistance is 3mΩ.It includes an IMON option that produces a voltage proportional to current through the power device set by a resistor from this pin to ground.

The MP5022A includes an optional discharge function that provides a discharge path for the external output capacitor when the part is disabled. Fault protection includes current limit, thermal shutdown and damaged power FET detection. The device also features over-voltage protection and under-voltage protection.

The MP5022A can be latched off by below conditions:

(a) Timer ramps up to 1.24V when OC and SC occur

(b) Trigger thermal shutdown

(c) EN and LOADEN Lower than its falling threshold

(d) Input voltage is lower than UVLO

Figure 1 shows the typical application circuit.

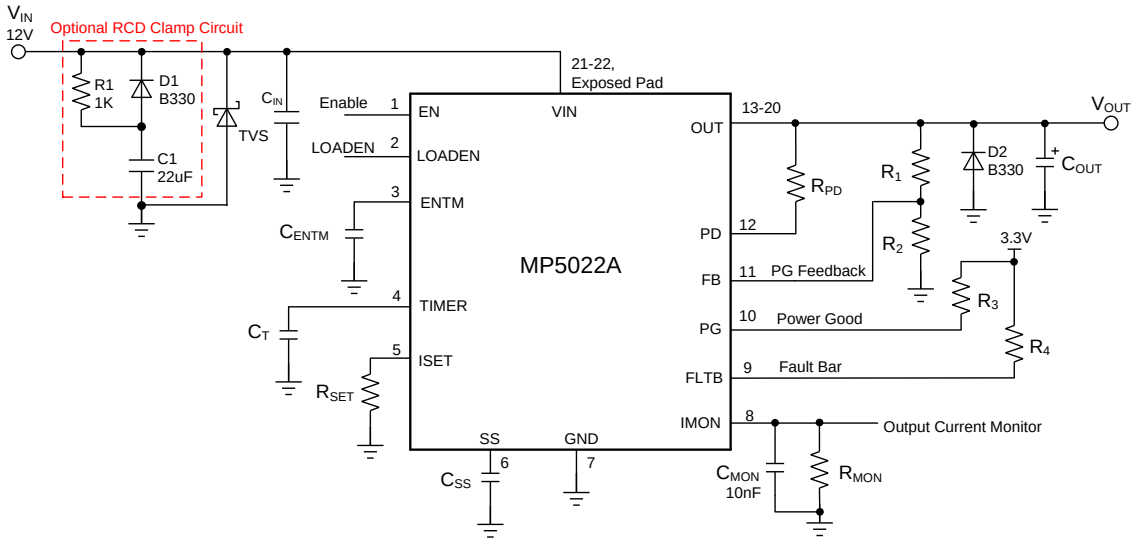

Figure 1—MP5022A Typical Application Circuit

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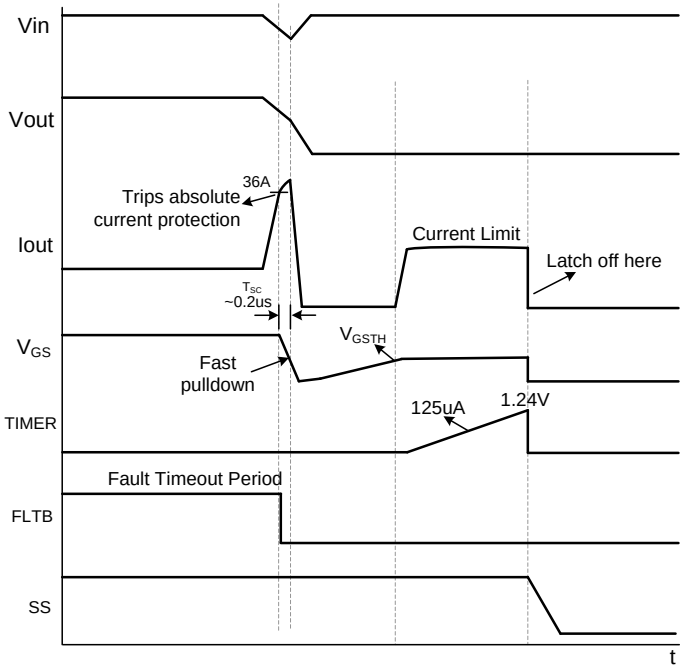
1. PROTECTION DESIGN NOTES

The MP5022A includes several protection functions. Short Circuit Protection, Over Current Protection, Thermal Protection, Damaged MOSFET Detection, Input voltage line Transient or spike protection, the design notes will be introduced in this section.

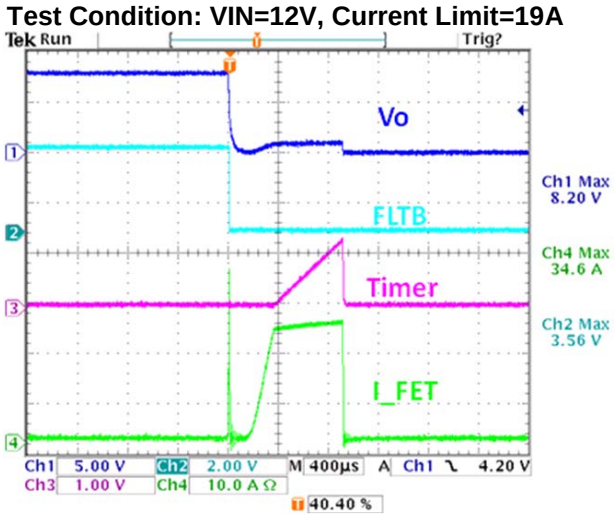
1.1 Short Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold by a lot before the control loop can respond. If the current reaches a 36A secondary current limit level, a fast turn-off circuit activates to turn off the power FET using a 100mA pull-down gate discharge current, as shown in Figure 2. This limits the peak current through the switch to limit the input voltage drop. The total short circuit response time is about 200ns. When the chip triggers short-circuit protection, it will restart once more which used to check whether the over load condition exists or not. If real short circuit happens, the part will latch off absolutely after hitting current limit and TIMER ramping up to 1.24V. Details see Figure 2-a.

FLTB switches low once it reaches a 36A current limit, and keeps low until the short circuit is removed. Figure 2-b shows the bench test result.



a)—Short Circuit Protection



b)—Short Circuit Tested Waveform

Figure 2—Short Circuit Protection and Tested Waveform

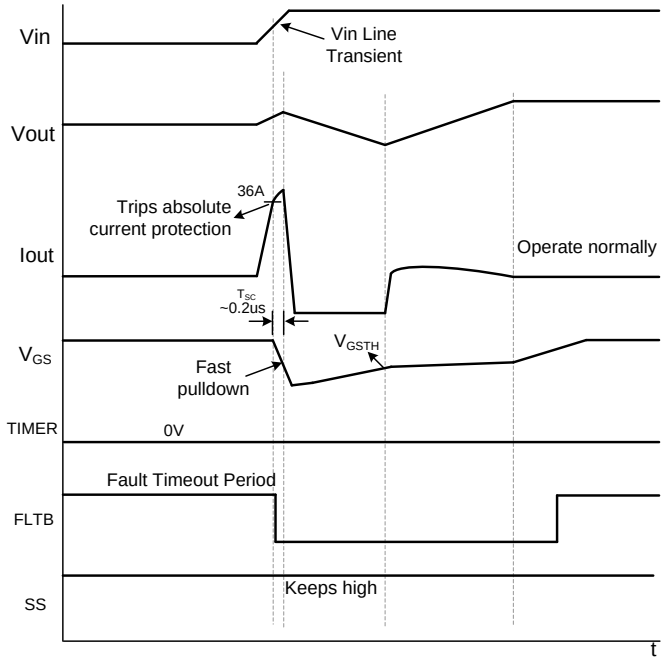
1.2 VIN Line Transient or Voltage Spike Protection

Actually, VIN line transient or voltage spike protection is the same with short circuit protection function.

If input voltage has a rapid slew rate line transient, the MP5022A should operate normally and can't be latched off as shown in Figure 3. For example, if VIN ramps up higher rapidly, the output voltage tries to follow VIN and large current will flow from the internal power FET to charge the output capacitor. If the load current increases rapidly, the current may exceed the current limit threshold by a lot before the control loop can respond.

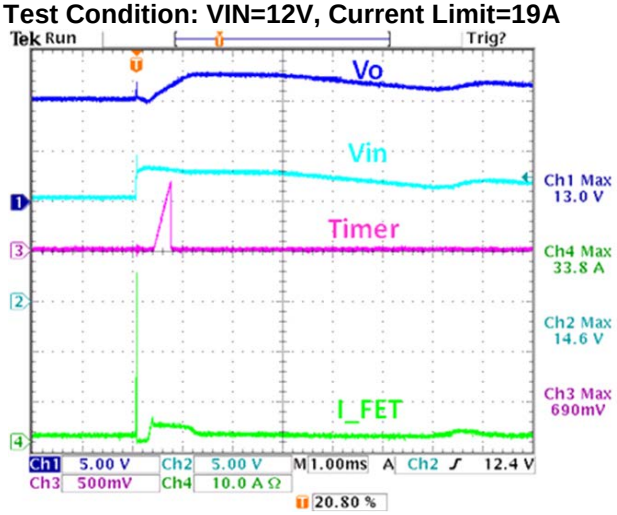
If the current reaches a 36A secondary current limit level, the same with short circuit protection, a fast turn-off circuit activates to turn off the power FET using a 100mA pull down gate discharge current, the total response time is about 200ns. When the chip triggers secondary current limit, it will restart once more. When the power FET gate-to-source voltage V_{GS} is pulled low, the 100mA pull down discharging current is disabled and the MP5022A internal charge pump charges the power FET gate voltage higher.

When the V_{GS} reaches V_{GSTH}, the power FET is turned on again. Soft start voltage SS keeps high during this period, the output voltage ramping slew rate depends on the gate charge current and output capacitor.



a)—VIN line transient Protection

Test Condition: VIN=12V, Current Limit=19A



b)—Line Transient Tested Waveform

Figure 3—VIN Line Transient and Tested Waveform

1.3 Over Current Protection

The MP5022A provides a constant current limit that can be programmed by an external resistor from ISET pin. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. In order to limit the current, the gate to source voltage needs to be regulated from 4V to around 1V. The typical response time is about 20μs and the output current may have a small overshoot during this time period.

When the current limit triggers, the fault timer starts. If the output current falls below the current limit threshold before the end of the fault timeout period, the MP5022A resumes normal operation. Otherwise, if current limit duration exceeds the fault timeout period, the power FET is latched off.

The MP5022A Current Limit value should be higher than the normal maximum load current, allowing the tolerances in the current sense value. The current limit can be set by below equation:

$$I_{LIMIT} = \frac{1.3(V)}{R_{SET}} \times 10^5 (A)$$

a) Current Limit lower than 7A

Figure 4 shows the current limit values vs. R_{SET} resistor when current limit is lower than 7A based on bench test results.

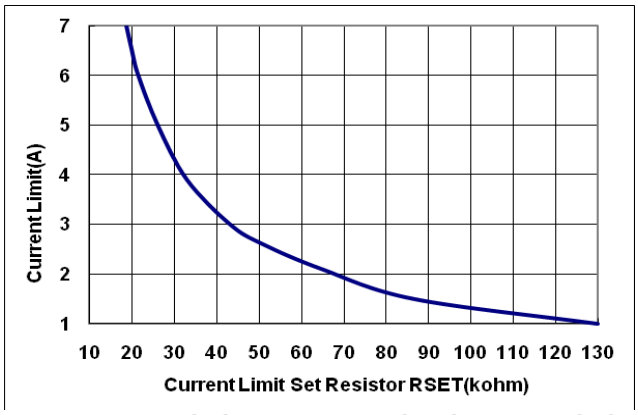


Figure 4—Current Limit vs. RSET Value (Current Limit < 7A)

The MP5022A current limit control loop gain increases when the current limit sets lower than 7A. Special design should be taken into condensation.

If over current happens, the internal power FET works in saturation region. From the relationship between the drain current I_D of power FET and gate-to-source voltage V_{GS}, the lower current limit, the lower V_{GS} voltage, that is, the power FET V_{GS} is close to V_{GSTH} when current limit is set lower.

$$I_D = K_n \cdot (V_{GS} - V_{GSTH})^2$$

Where $K_n = \frac{\mu_n C_{ox}}{2} \frac{W}{L}$, which is the power FET constant parameters.

If V_{GS} closes to V_{GSTH}, tiny V_{GS} changes will induce much change of drain current. For example, if MP5022A hits current limit, the power FET V_{GS} voltage is discharged and V_{GS} is pulling down. Drain current drops much as V_{GS} decrease, the over current condition may disappear. When lose over current condition, V_{GS} pulling down doesn't work and the power FET gate is charged up higher again by internal charge pump, drain current may increase a lot as V_{GS} ramps up. Therefore the load current may ring and current limit control loop is unstable. The ringed control loop cannot give stable current limit signal to TIMER controller, so the TIMER voltage can't to ramp up higher.

To decrease the current limit control loop gain when current limit is set lower, it's recommended to add an R/C circuit to parallel with R_{SET} resistor as shown in Figure 5. Generally, choose R=20kΩ, C=560pF.

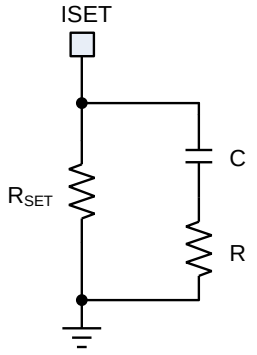
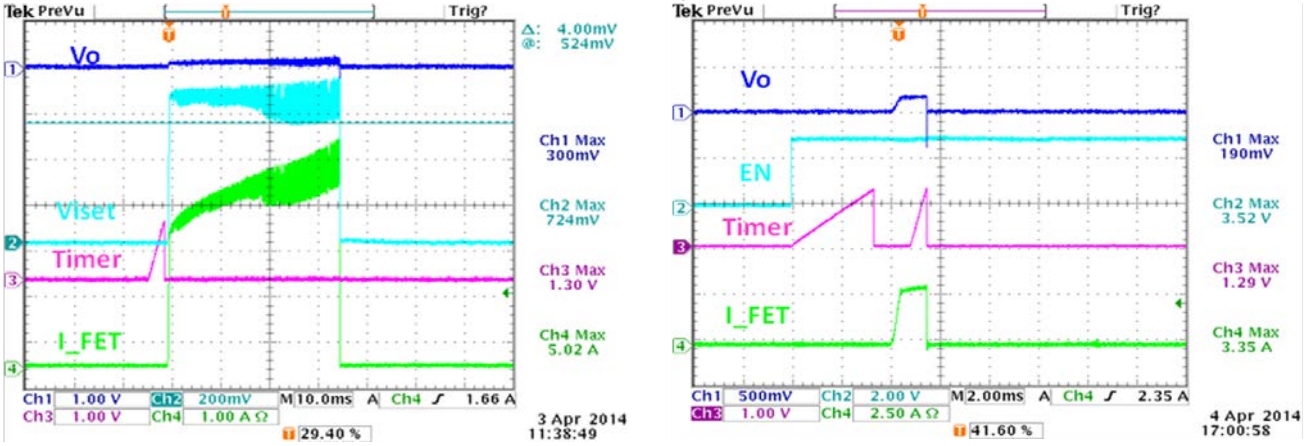


Figure 5—R/C circuit for R_{SET} When Current Limit <7A

Figure 6 shows the bench test results when start up through EN @ short circuit condition. When no paralleled RC with R_{SET}, the load current rings, when adds R/C circuit, the part operates normally.

Test Condition: VIN=12V, Current limit =2.6A



a) Performance NG w/o R/C Circuit **b) Performance OK w/ R/C Circuit**

Figure 6—Waveforms of EN Start up @ Short Circuit, Current Limit=2.6A

As shown in the waveform of Figure 7, when the MP5022A start up through EN @ short circuit condition, there is some time delay for TIMER ramping up when hit current limit. The delay is caused by internal control logic.

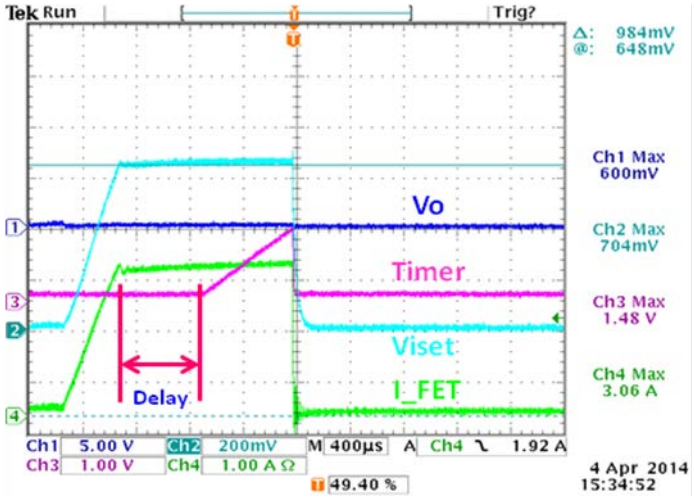


Figure 7—EN start up @ Short Circuit, TIMER has Delay

There are 2 conditions to control TIMER ramping up in MP5022A as shown in Figure 8.

a. Power FET gate-to-source voltage V_{GS}<2V

b. The Current limit control loop gate pulling down current reaches to 8uA.

During start up @ short circuit, the power FET V_{GS} voltage is always lower than 2V, the first condition for TIMER ramping up is met.

For the second condition, during short circuit start up, SS ramps up higher from zero, the soft start control loop will induce discharging current for V_{GS}. That is, even through the part has hit current limit, but the ISET current limit loop pulling down current is lower than 8uA.

The SS control loop loses control gradually when SS voltage is much higher than Vout, all the 8uA current flows from current limit control loop, then TIMER voltage begins rising. Therefore, there exists some time delay for TIMER ramping up and the delay is ok.

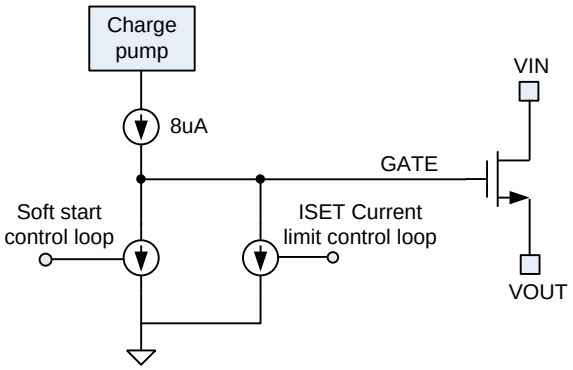


Figure 8—MP5022A Gate Control

b) Current Limit higher than 7A

When the current limit is higher than 7A, the MP5022A current limit control loop is much more stable and there is no need to add additional the RC circuit to R_{SET} resistor. Figure 9 gives the relationship between current limit value and R_{SET} resistor when current limit ≥7A.

The maximum normal operation current for MP5022A is about 20A, so the maximum current limit can be set to 120% of normal current (about 24A).

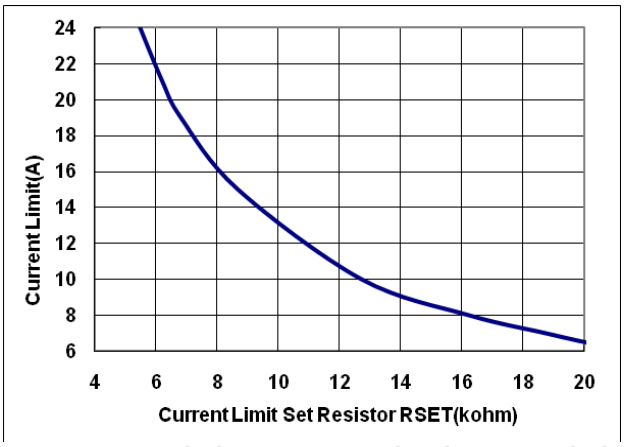


Figure 9—Current Limit vs. RSET Value (Current Limit ≥ 7A)

1.4 Need VIN RCD Circuit if Hard Short Happens

The typically input decoupling capacitor for MP5022A application is around 0.1μF or no input capacitor. When hard short circuit happens, the input voltage may be pulled low rapidly because of the input line trace parasitic impendence from the power supply.

When VIN falls below VULO threshold, the GATE fast turning off control logic will out of control and the internal power FET can't be turned off immediately; the load current may run away.

Therefore, additional RCD circuit is required if the MP5022A chip location is a little far away from the power supply. As shown in Figure 10, the RCD circuit can prevent input voltage from dropping below its UVLO threshold. A 22μF ceramic capacitor is enough to hold the line voltage and turn off the power FET in time for MP5022A if short circuit happens. During normal start up, the capacitor is not involved in the circuit and it's unable to produce inrush current. Put the RCD circuit near the hot swap input leads.

If the chip location is near the power supply, eg, there is bulk capacitor on the backplane board's output terminal, which is used for the MP5022A input. The RCD circuit is unnecessary and can be removed, in this condition, the input voltage won't be pulled much lower.

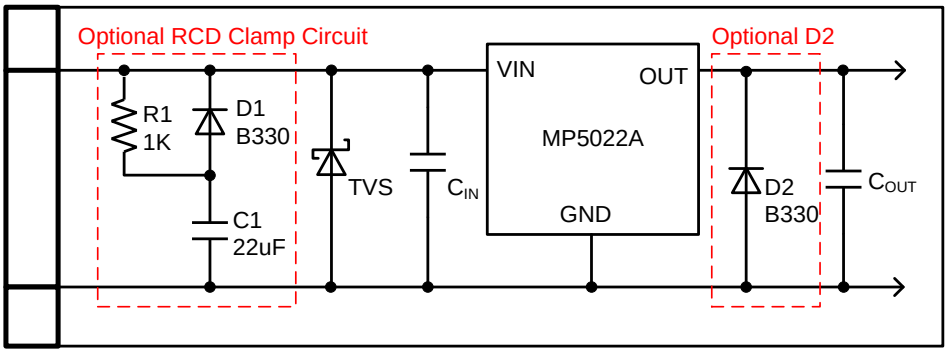


Figure 10—RCD Clamp Circuit in MP5022A Hot Swap System

1.5 Input and Output Transient Protection

Hot swap system experience positive transient on the input during hot plug or rapid turnoff with high current due to parasitic inductance in the input circuit.

For Input transient protection, a TVS diode (transient voltage suppressor, a type of Zener diode), may be required on the input to limit transient voltages below the absolute maximum ratings as shown in Figure 10.

The output may experience negative transient during rapid turnoff with high current due to parasitic inductance in the output circuit. An output voltage clamp diode may be required on the output to limit negative transients as shown in Figure 10. Select a schottky diode with low forward voltage at the anticipated current during an output short. By doing that the negative voltage spike at the output terminal can be clamped at less than -0.7V thus the IC can be protected during short output. If the output circuit parasitic inductance is tiny, the output voltage clamp diode can be optional.

1.6 Damaged MOSFET Detection

The MP5022A can detect a shorted pass FET during power up by treating an output voltage that exceeds V_{IN}-1V during power-up as a short on the power FET. The detail operation can be seen in Figure 11 and Figure 12. The FLTB# pin will be pulled low to indicate a fault condition and the power switch is held off, PG signal keeps low.

Once remove short and $V_{OUT} \leq V_{IN}$-1, the part starts up normally. During this period, PG signal keeps low until the following three conditions are met. 1) VFB>1.245V, 2) VGS>3V, 3) VOUT> VIN-1V.

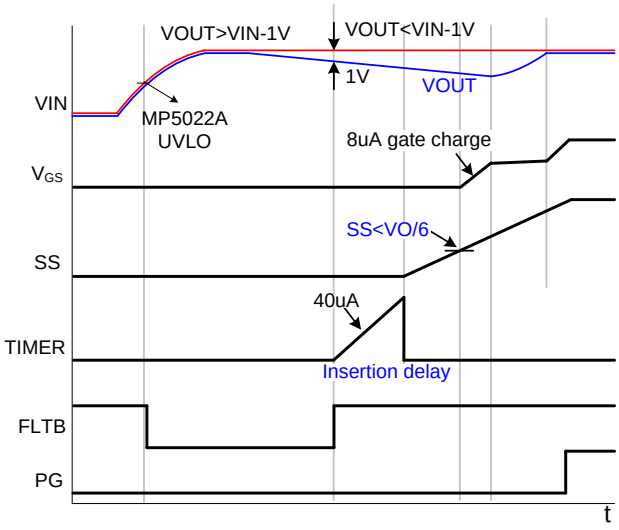


Figure 11: Damaged MOSFET Detection

Test Condition: VIN=12V, Iload=0A

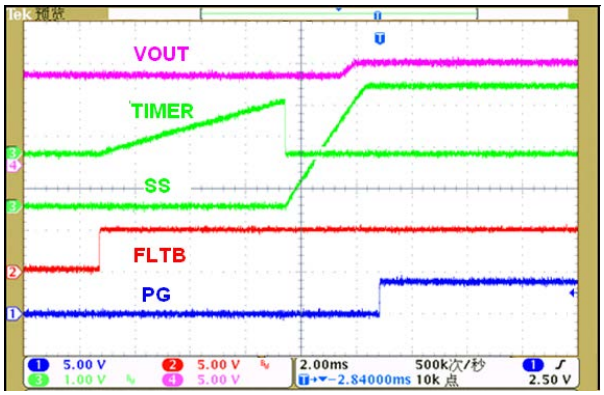


Figure 12: Damaged MOSFET Tested Waveform

2. NORMAL OPERATION DESIGN NOTES

This section mainly introduces EN, LOADEN and IMON design notes.

The Soft-Start, Fault Timer and LOADEN Blanking Timer are also introduced briefly, these items set is similar with MP5022.

2.1 EN Design Note

EN can be connected to external power supply to control the on/off of the part, also EN can be connected to VIN by a resistor divider for an automatic start up. If EN is connected to VIN by a resistor divider or directly pulled high to VIN, please make sure add a 10nF capacitor from EN pin to ground.

a)—EN Connected to VIN by a Resistor Divider **b)—EN pin Connection if EN Pulled to VIN**

Figure 13—EN Connected to VIN by a Resistor Divider

2.2 LOADEN Function Introduction

LOADEN is used to control the ON/OFF of the MP5022A together with EN pin as below table shows. LOADEN is used to shut down the power switch after LOADEN blanking time but can't turn it on by recycle LOADEN only.

Table 1—Output Enable Table

Enable blanking time is over?	EN	LOADEN	Status
N	0	0	OFF
N	0	1	OFF
N	1	0	ON
N	1	1	ON
Y	0	0	OFF
Y	0	1	OFF
Y	1	0	OFF
Y	1	1	ON

a) LOADEN Design Notes

LOADEN can be connected to external power supply to control the on/off of the part, if LOADEN connected to VIN by a resistor divider for an automatic start up, the LOADEN divider ratio should be set to among 1/2 to 1/4 to avoid abnormal shut down. A small capacitor about 10nF is also recommended to connect from LOADEN to GND as shown in Figure 14.

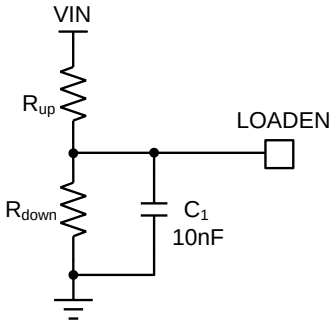


Figure 14—LOADEN pin Connection

b) LOADEN Blanking Time

LOADEN has a programmable blanking time that prevents LOADEN from de-asserting during the blanking time. All fault functionality is operative during the start-up so that the power switch shuts down if a fault was detected; however, LOADEN pulling low during this blanking time won't turn off the switch. After LOADEN blanking time is over, LOADEN behaves as normal and can turn off the power switch. The blanking time can be set by a capacitor connected to the ENTM pin by:

$$C_{ENTM} = \frac{t_{LDNB} \cdot 10^{-6}}{1.24}$$

Where: t_{LDNB} = LOADEN blanking time, C_{ENTM} = LOADEN blanking time capacitor on ENTM pin. Below table shows the typical LOADEN blanking time when different C_{ENTM} are adopted.

Table 2—LOADEN Blanking Time vs. C_{ENTM}

C_{ENTM}	LOADEN Blanking Time
0.1μF	124ms
0.33μF	409ms
1μF	1.24s

Floating the ENTM pin generates a fast ramp-up voltage on the ENTM pin. The blanking time during this period is negligible.

c) How to Disable LOADEN Function

If customers don't want to use LOADEN, short ENTM to GND will disable the LOADEN function.

If short ENTM to GND, the LOADEN blanking time equivalents to be stretched to infinity, so the high or low of LOADEN signal has no influence to the part as shown in Figure 16. In this condition, the LOADEN signal can be connected to high/low or float optionally. It's recommended to connect to ground.

Figure 17 shows the bench test results when short ENTM to GND, the part works normally when LOADEN becomes low.

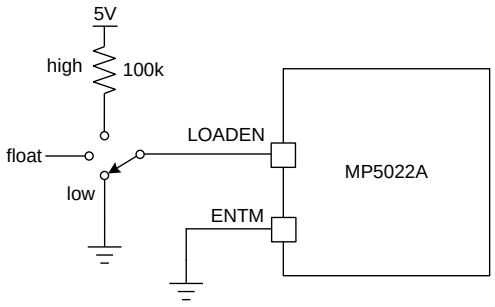


Figure 15—Connect ENTM to Ground to Disable LOADEN

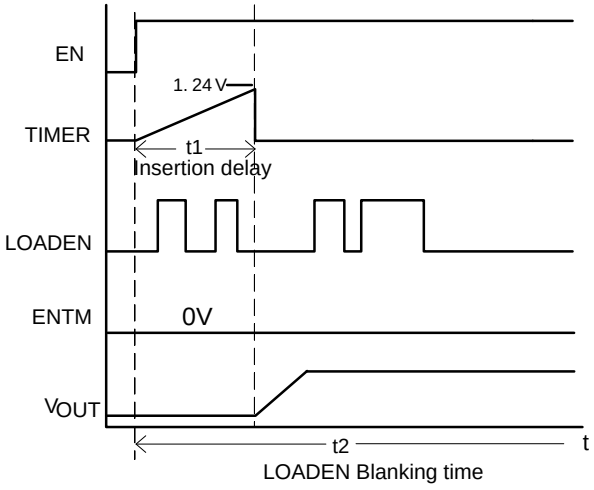


Figure 16—LOADEN Blanking Time

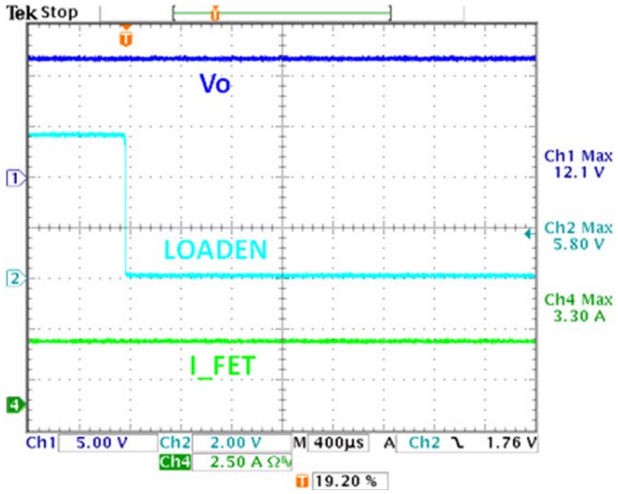


Figure 17—Bench Results @ ENTM short to GND

2.3 IMON Pin Design Note

The MP5022A IMON pin is the output of an accurate current-sense amplifier and provides a source current proportional to the load current flowing into the main switch. The current sense gain is set to 10μA/A. To make sure IMON signal stable, more than 10nF capacitor should be paralleled with R_{MON} resistor. To get best accuracy, it's recommended to use resisters within 1% accuracy.

Placing 10k resistor to ground creates a 0V to 2V voltage when power FET current ranges from 0A to 20A. The voltage compliance for IMON pin is from 0V to 3V.

$$V_{MON} = R_{MON}(K\Omega) \times 10 \times I_{POWER\_FET} \quad (mV)$$

Where I_{POWER_FET} is the current flowing from power FET

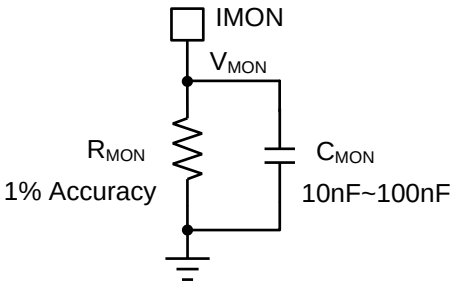


Figure 18—IMON Pin Connection

2.4 Soft-Start Time Design

The MP5022A limits inrush current by controlling the ramp-up slew rate of output voltage. The output voltage rises at a similar slew rate to the voltage at SS pin. A capacitor connected to the SS pin determines the charging slew rate and the soft-start time. When the insertion delay time ends, a constant current source that is proportional to input voltage charges up the voltage on the SS pin. Float the SS pin to generate a fast ramp-up voltage. An 8μA current source pulls up the gate of the power FET. The gate charge current controls the output voltage rise time. The approximate soft start time is then 1ms and is the minimum soft-start time.

The SS capacitor value is given by below equation.

$$C_{SS}(nF) = \frac{6 \times t_{SS}(ms)}{R_{SS}(M\Omega)}$$

Where: t_{SS}=soft start time, R_{SS}=1.1MΩ.

Table 3 gives the typical soft start time when different C_{SS} are adopted.

Table 3—Soft Start Time vs. C_{SS}

SS Cap C_{SS}	Soft Start Time T_{SS}
47nF	8.6ms
100nF	18.3ms
220nF	40.3ms

The soft-start time should be chosen carefully when the load capacitance is extremely large. It should be long enough charge up the output capacitor without hitting the current limit. For worst case: the continuous current load is less than and close to the current limit, the minimum soft-start time to charge up the output capacitor without tripping current limit can be estimated by:

$$t_{SS} > \frac{C_{OUT} \times V_{OUT}}{I_{LIMIT} - I_{LOAD}}$$

However, the soft-start time can't be chosen too long. The MP5022A has over temperature shutdown function. Once the die temperature exceeds approximately 145°C, the internal power FET will be turned off. During soft-start time, instantaneous power consumption is much higher since the power FET is not fully enhanced, which will increase the die temperature. The power consumption should keep in the SOA rating of the power FET. Figure 19 shows the maximum load current vs. soft-start time without over temperature protection trips. No load capacitors are applied during this test.

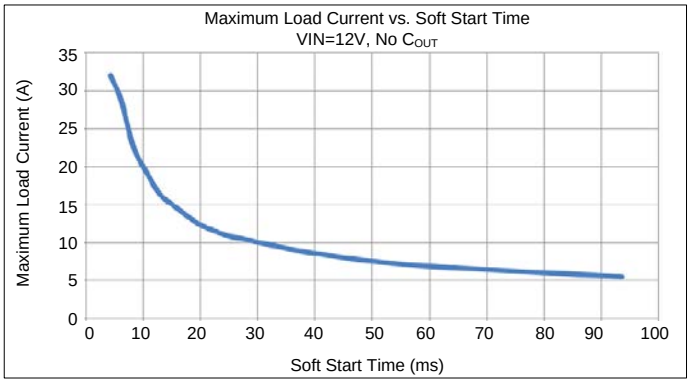


Figure 19—Maximum Load Current vs. Soft-Start Time of MP5022A

From the description above, to support a 2200uF output capacitor, 15A constant-current load with 18A current limit, the soft-start time should be between 8.8ms and 11ms.

2.5 Fault Timer Design

When the current reaches its limit threshold, a 215μA internal constant current source charges the external TIMER pin capacitor C_T. If the over current limit state ceases before the TIMER voltage reaches 1.24V, the MP5022A returns to normal operation mode and it will release timer immediately when over current fault removed. If the over current limit state lasts beyond the TIMER pin voltage reaches 1.24V, the power FET switches off. The fault time is given by below:

$$t_{FLT}(s) = \frac{1.24 \cdot C_T(\mu F)}{215(\mu A)}$$

When the C_T is chosen, the insertion delay during power up sequence is determined as well since they share the TIMER pin capacitor but the charging current during hot-plug insertion delay is 43μA. So the insertion delay is:

$$t_{DELAY}(s) = \frac{215}{43} \times t_{FLT}$$

Table 4 shows the typical LOADEN blanking time when different C_{ENTM} are adopted.

Table 4—Fault and Delay Time vs. TIMER capacitor C_T

TIMER Cap C_T	Fault Time t_{FLT}	Insertion Delay Time t_{DELAY}
0.1μF	0.58ms	2.9ms
0.33μF	1.9ms	9.5ms
1μF	2.7ms	13.6ms

3. LAYOUT DESIGN GUIDE

1) The high current path from the board's input to output, and the return path, should be parallel and close to each other to minimize loop inductance.
2) Connect MP5022A GND pin and signal GND together at first, and then Kelvin connect to its PGND or internal GND layers.
3) Input decoupling capacitors on VIN pin should have minimal trace length to the VIN pins and to GND.
4) Place a transient voltage suppressor diode (TVS) to the VIN, the TVS can absorb the input voltage spike when load current decreased sharply.
5) Place the schottky diode close to the OUT pin and GND to absorb negative voltage spike when the power FET is shut off
6) Place output capacitors as close to the part as possible to minimize the effect of PCB parasitic inductance.

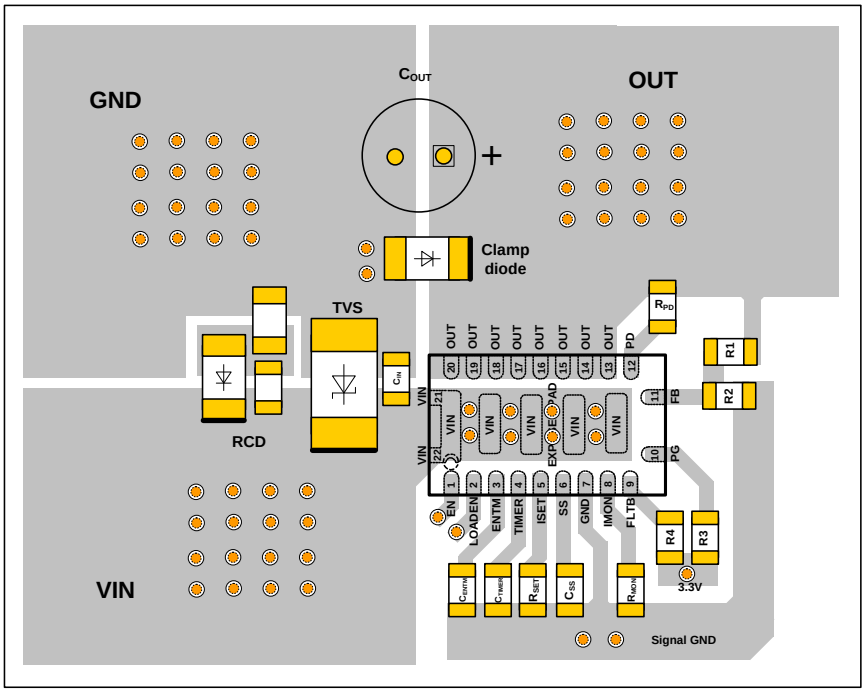


Figure 20—Recommended Layout