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A Typical Wide Input Range 12-W DC-to-DC Isolated Converter for xEV Auxiliary Power Supply

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APPLICATION NOTE

AND90111/D

Quasi−square wave resonant converters also known as Quasi−Resonant (QR) converters are widely used in the adaptor market. They help designing flyback Switched−Mode Power Supply (SMPS) with a reduced Electro−Magnetic Interference (EMI) signature and improved efficiency. However, a major drawback of the structure is that the frequency can become dramatically high at light load.

In traditional QR converters, the frequency is limited by a frequency clamp. But, when the switching frequency of the system reaches the frequency clamp limit, valley jumping occurs: the controller hesitates between two valleys resulting in an instable operation and acoustic noise can be heard in the transformer at medium and light output loads.

In order to overcome this problem, the NCV1362 features a proprietary “valley lockout” circuit: the switching frequency is decreased step by step by changing valley from valley n to valley $(n + 1)$ as the load decreases. Once the controller selects a valley, it stays locked in this valley until the output power changes significantly. This technique extends the QR operation of the system towards lighter loads without degrading the efficiency.

Several Electrical Vehicles sub−systems such as On Board Chargers and Traction Inverters look for simple, compact and reliable isolated flyback converters. One of the most common solution is to perform a Primary Side Regulation (PSR), where the voltage and current regulation, usually made in a chip placed in the secondary side and communicating via an optocoupler with the primary−side controller, is performed in the primary side thanks to a patented method. All components related to a classical feedback loop (optocoupler, shunt regulator, bridge resistance) are saved and the circuit gains in reliability and assembly costs.

This application note focuses on the design of a power supply taking a 50 up to 400 V dc input that delivers an isolated and well regulated 12 V/1 A output using the NCV1362. The equations developed are further used to build a 12−W adaptor.

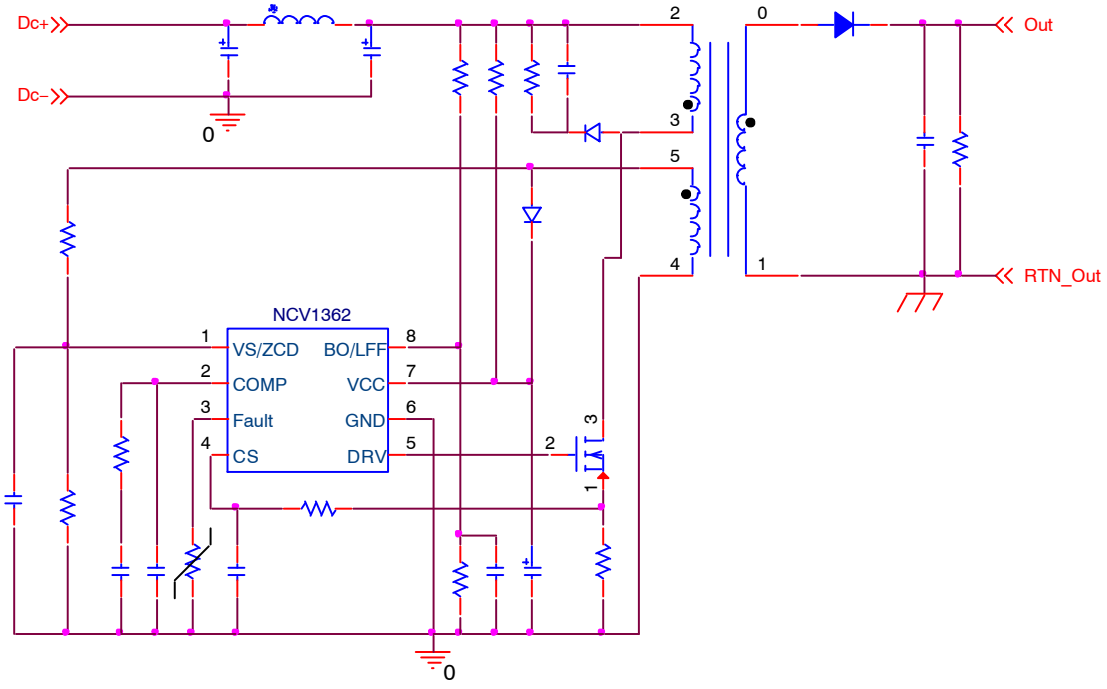

Figure 1. Typical Application Schematic

Power Stage Dimensioning

The design of the power stage driven by the PSR controller can be divided in 8 steps:

1. Specification of the Adapter
2. Transformer Design
3. Sense Resistance
4. ZCD Bridge Resistance
5. Secondary−side Components (diode and capacitor)
6. Compensation Network
7. Brown out and LineFeed Forward
8. Startup resistor

Step 1: Specification of the Adapter

In order to illustrate this application note, a 12−V/12−W power supply will be the design example.
The specifications are detailed in Table 1.

Table 1. SPECIFICATION OF THE 12 V, 12 W ADAPTER

Parameter	Symbol	Value
Minimum input voltage	$V_{in,min}$	50 V dc
Maximum input voltage	$V_{in,max}$	400 V dc
Output voltage	V_{out}	12 V
Nominal output power	$P_{out(nom)}$	12 W
Switching frequency at $V_{in,min}$, $P_{out(nom)}$	F_{sw}	50 kHz
Efficiency	η	85%
Maximum startup time	$T_{startup}$	< 3 s

Step 2: Transformer Design

The principal component in a power supply is the transformer. The whole structure works around this part so we will start the design with its characteristics. Three mains parameters are needed to define a transformer:

1. Primary to secondary turn ratio (N_{ps})
2. Primary inductance (L_p)
3. Primary to auxiliary winding turns ratio (N_{aux})

Primary to Secondary Turns Ratio (N_{ps})

The turns ratio between the primary and the secondary winding is intimately connected to the maximum MOSFET voltage (BV_{DSS}), the maximum input voltage and the nominal output voltage. The typical drain voltage is shown in Figure 2 for a flyback topology.

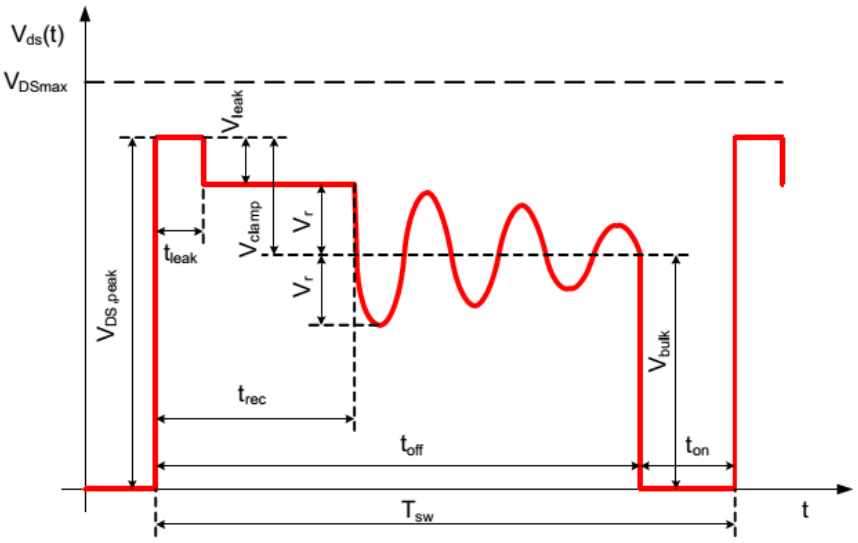

Figure 2. Drain−Source MOSFET Voltage

The voltage on the drain pin during the off time is the addition of different parameters. The first contributor is the input voltage (V_{bulk}). Then we have the output voltage reflected on the primary side via the transformer turns ratio (V_r). Finally, the leakage inductance will bring an additional voltage called V_{leak}. Also, due to the slow reaction of the clamping network, another voltage is added (typically V_{os} = 20 V). The addition of these four voltages must remain below the maximum voltage allowed by the MOSFET after applying the choosing derating factor (k_d = 90% generally).

The ratio between the reflected voltage and the clamp voltage is called k_c.

$$k_c = \frac{V_{clamp}}{V_r} \quad \text{(eq. 1)}$$

The selection of k_c depends on design choices. Poorly designed transformers with a large leakage inductance will require a greater k_c coefficient ($k_c > 2$). On the other hand, less than 1% leakage inductance will allow the reduction of the difference between the clamp threshold and the reflected voltage ($1.3 < k_c < 1.5$). In this example we will set $k_c = 1.9$.

Thanks to the above explanation, the turns ratio can be defined by:

$$N_{ps} = \frac{k_c(V_{out} + V_f)}{k_d BV_{DSS} - V_{os} - V_{in\_max}} \quad \text{(eq. 2)}$$

Applying the equation 2 to our adaptor specification:

$$N_{ps} = \frac{1.9(12 + 0.6)}{0.9 \times 650 - 20 - 400} = 0.145 \quad \text{(eq. 3)}$$

In the above equation, we assume the diode forward drop to be 0.6 V.

Primary Peak Current (I_{pk})

Knowing the turns ratio, we are able to determine the primary peak current. The parameter will be needed to set the primary current saturation of the transformer. The worst case will happen when the input voltage is to the minimum level. The lower input voltage is 50 V dc.

We can now evaluate the maximum primary peak current:

$$I_{pk,pri} = \frac{2P_{out}}{\eta}\left(\frac{1}{V_{in\_min}} + \frac{N_{ps}}{V_{out} + V_f}\right) + \pi\sqrt{\frac{2P_{out}(C_{OSS} + C_{DS})f_{sw}}{\eta}} \quad \text{(eq. 4)}$$

Where C_{OSS} is the MOSFET output capacitance and C_{DS} the optional added capacitor in parallel with the Drain−Source.

Applying equation 4 to our adapter specification:

$$I_{pk,pri} = \frac{2 \times 12}{0.85}\left(\frac{1}{50} + \frac{0.145}{12 + 0.6}\right) + \pi\sqrt{\frac{2 \times 12\ (10p + 0)\ 50k}{0.85}} = 0.901\ A \quad \text{(eq. 5)}$$

Primary Inductance (L_p)

The traditional formula to calculate the output power for a Flyback topology is:

$$P_{out} = \frac{1}{2} L_p I_{pk,pri}^{\ 2} f_{sw} \eta \quad \text{(eq. 6)}$$

By rearranging equation 6, the primary inductance can be extracted:

$$L_p = \frac{2P_{out}}{I_{pk,pri}^{\ 2} \eta f_{sw}} \quad \text{(eq. 7)}$$

$$L_p = \frac{2 \times 12}{0.901^2 \times 0.85 \times 50k} = 695\ \mu H \quad \text{(eq. 8)}$$

Primary to Auxiliary Winding Turns Ratio (N_{aux})

The last parameter that has to be defined relates to the transformer turns ratio affecting the primary and the auxiliary windings. The turns ratio is chosen in order to have the right supply voltage for the controller regardless of operating conditions. Due to the leakage inductance, the voltage on the V_{cc} pin will be higher when the power supply (PSU) operates at full load compared to the level in stand−by mode. In this last case, the part works at the minimum switching frequency (i.e. 1 kHz) so the duration between each cycle is longer. Also, due to the low frozen peak current, the energy stored in the transformer during the on−time is reduced and the demagnetization time will be narrow. The V_{cc} capacitor refresh will be limited. The auxiliary winding will thus be defined to have enough voltage in no−load condition to supply the controller and have some margins regarding the UVLO threshold (i.e. 6.5 V typ.).

Also, the V_{cc} voltage excursion must remain reasonable otherwise the stand−by performance will be affected by the driver stage power dissipation. In a no−load condition, the MOSFET peak current during the on−time is limited so there is no need to have a strong gate−source voltage (at 12−13 V).

Accounting for all these criteria, a good trade−off for this controller is to set the V_{cc} voltage around 9 V in no−load condition.

$$N_{aux} = \frac{N_{ps}(V_{cc} + V_{f,aux})}{V_{out} + V_f} \quad \text{(eq. 9)}$$

Where V_f is the forward voltage of the secondary diode and $V_{f,aux}$ the forward voltage of the V_{cc} diode.

The turn ratio between the primary and the auxiliary winding should be:

$$N_{aux} = \frac{0.145 \times (9 + 0.8)}{12 + 0.6} = 0.11 \quad \text{(eq. 10)}$$

The four mains transformer characteristics have been calculated in the above section:

1. Primary to secondary turn ratio
2. Primary to auxiliary turn ratio
3. Primary current saturation
4. Primary inductance

Step 3: Sense Resistance

Another key component for the primary−side constant current regulation (CC) patented by ON Semiconductor is the sense resistor.

The controller is able to reconstruct the output current by sensing two parameters:

1. The primary current through the CS pin voltage
2. The demagnetization time thanks to the auxiliary winding

The leakage inductance brings an error in the CC regulation. The primary current negative slope at turn−off is reduced as depicted in the Figure 3. The consequence is that the secondary peak current is lower than expected:

$$I_{pk,sec} < \frac{I_{pk,pri}}{N_{ps}} \qquad \text{(eq. 11)}$$

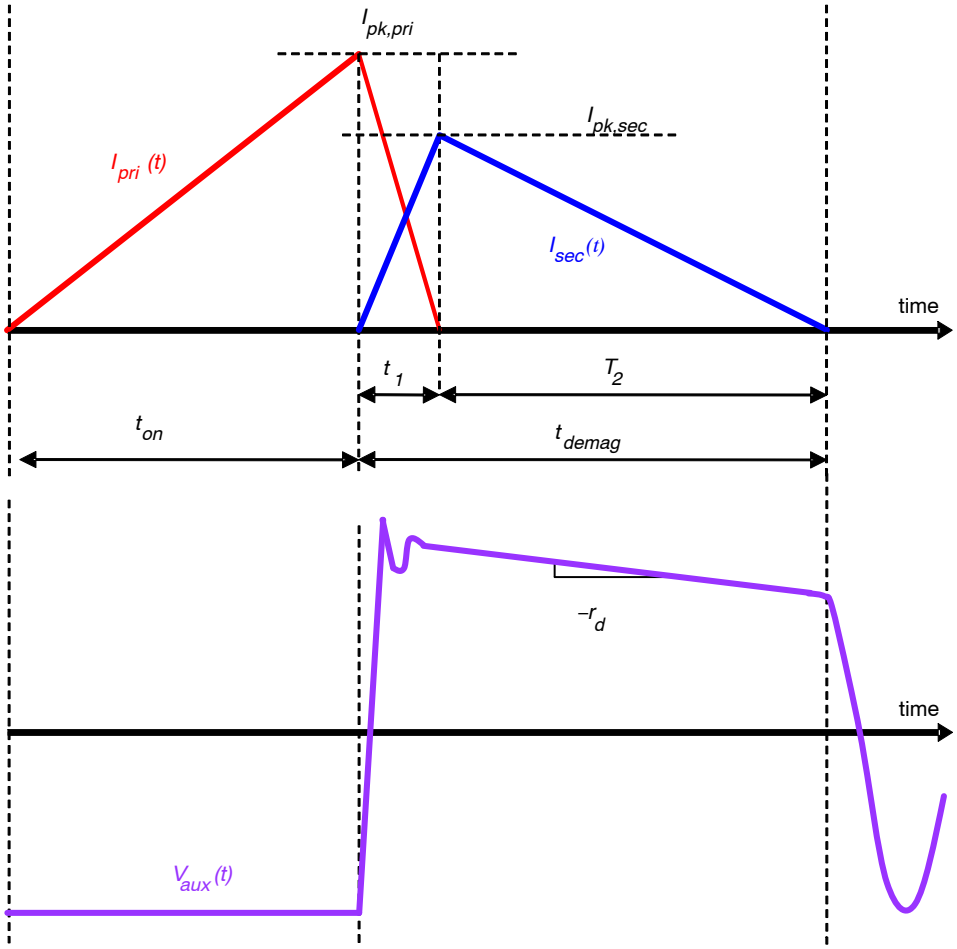

Figure 3. The Ripple Voltage during the Off−time is Mainly Dictated by the Diode Dynamic Resistance r_d

Thanks to its internal constant−current block, the controller accounts for the leakage inductance effect and forces a constant output current with a value defined by:

$$I_{out} = \frac{V_{Ref\_CC}}{2K_{comp}N_{ps}R_{sense}} \qquad \text{(eq. 12)}$$

NOTE: In this formula, V_{Ref_CC} is the internal voltage reference for the CC regulation.

The output current limit is set by choosing the sense resistor:

$$R_{sense} = \frac{V_{ref\_CC}}{2K_{comp}N_{ps}I_{out}} \qquad \text{(eq. 13)}$$

The internal reference voltage V_{ref_CC} is 1 V and the K_{comp} divider is 4. For the 12−V/12−W application, the nominal output current will be 1 A. Applying a 10% margin, the sense resistance should be:

$$R_{sense} = \frac{1}{2 \times 4 \times 0.145 \times 1.1} = 0.784\ \Omega \qquad \text{(eq. 14)}$$

Step 4: ZCD Resistive Bridge

When the load is below the maximum threshold allowed by the CC loop, the controller operates in constant voltage (CV) regulation. How is the CV regulation implemented for this controller?

When the energy stored in the transformer is delivered to the secondary during the demagnetization time, the auxiliary voltage is the sum of the output voltage scaled by the auxiliary to secondary turn ratio and the secondary

forward diode voltage. This secondary forward diode voltage could be split in two elements: the first one is the forward voltage of the diode (V_{T0}) and the second is related to the dynamic resistance of the diode multiplied by the secondary current ($r_d \cdot i_{sec}(t)$). The illustration of the dynamic resistance can be seen in Figure 3. This second term, especially the secondary current, will depend on the load and line conditions.

To reach an accurate primary−side constant−voltage regulation, the controller detects the end of the demagnetization time and precisely samples the output voltage level seen on the auxiliary winding. Because this moment coincides with a secondary−side current equal to zero, the diode forward voltage drop becomes independent from the loading conditions.

$$V_{aux} = \frac{N_{aux}}{N_{ps}} \left(V_{out} + V_{fo}\right) \qquad \text{(eq. 15)}$$

The internal reference voltage for the CV regulation is 2.5 V. We already defined the auxiliary winding (step 1) to deliver 10 V when the output voltage is regulated to 12 V. A resistor divider has to be added to set 2.5 V on the ZCD pin when the output voltage is regulated to 12 V, the nominal voltage.

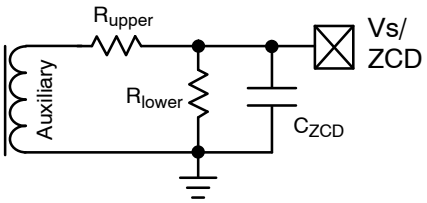

Figure 4. ZCD Pin Network

Let's arbitrarily fix the upper resistor to 10 kΩ. According to the internal voltage reference V_{ref_CV}, the lower resistor will be:

$$R_{lower} = \frac{V_{ref\_CV}}{V_{aux} - V_{ref\_CV}} R_{upper} \qquad \text{(eq. 16)}$$

$$R_{lower} = \frac{2.5}{9.6 - 2.5} \times 10k = 3.5\ k\Omega \qquad \text{(eq. 17)}$$

These resistors have to be adjusted in the laboratory to obtain the exact output voltage value.

The capacitor C_{ZCD}, connected in parallel to the pull−down resistor offers a way to delay the MOSFET turn−on event and exactly switch in the minimum of the drain−source voltage: switching losses are greatly reduced in this case.

Please note that this capacitor must be of reasonable value to keep a good accuracy on the CV regulation in stand−by mode when the demagnetization time is really limited. The maximum recommended time constant τ is around 300 ns.

We can deduce the ZCD capacitor:

$$C_{ZCD} \leq \frac{R_{upper} + R_{lower}}{R_{upper} R_{lower}} \tau \qquad \text{(eq. 18)}$$

In our application, the capacitor on the ZCD pin must be below:

$$C_{ZCD} \leq \frac{10k + 3.5k}{10k \times 3.5k} 300n \leq 38\ pF \qquad \text{(eq. 19)}$$

Step 5: Secondary Side Components

The component count in the secondary is limited owing to the PSR topology. In a classical application, an optocoupler with a voltage reference (TL431) are needed. In our case, these components are saved, only the power parts are inserted like the output rectifier diode and capacitor.

Output Rectifier

Let's talk about the output rectifier. Two parameters will help choosing this diode. The first one is the maximum peak repetitive reverse voltage noted V_{RRM}. The second one is related to the power dissipation at the nominal output power. Indeed, as explained above, the forward voltage can be expressed by:

$$V_f = V_{T0} + r_d I_d \qquad \text{(eq. 20)}$$

The power dissipated by the diode will be:

$$P_d = V_{T0} I_{out} + r_d I_{rms,sec}^2 \qquad \text{(eq. 21)}$$

This equation highlights the impact of the dynamic resistance (r_d) and the forward voltage without current (V_{T0}).

We will compare two different diodes and see the power dissipation in our application. The first diode will be a classical Schottky diode, MBR5100MFS. This diode will be compared to the trench−based diode (NRVTSS5100E). One of the advantages of this second diode is a lower forward voltage. The characterization curves help us to extract r_d and V_{T0}.

In our application according to the transformer specification, the secondary rms current will be 2.2 A for the worst case. By doing the ΔV over ΔI around the operating current (the nominal I_{out}), the dynamic resistance is defined. We took the 125°C curve to be as closed as possible to the normal condition when the ambient temperature is above 50°C.

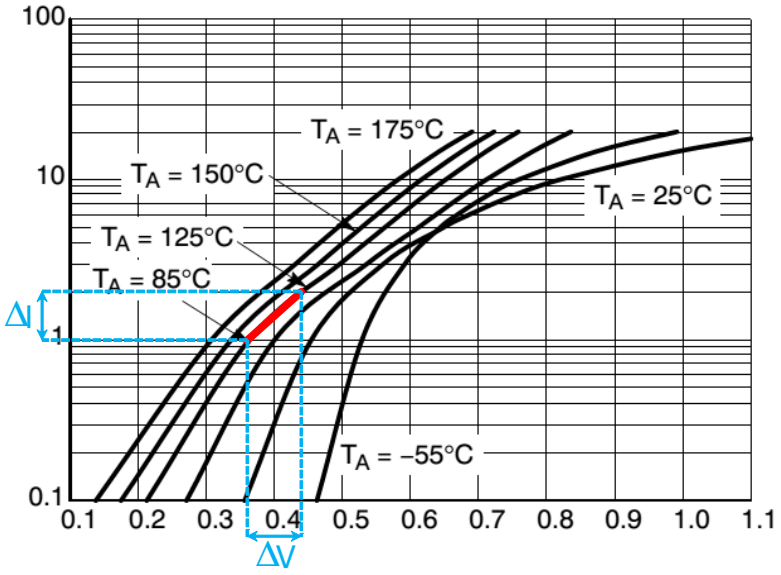

Figure 5. V_f vs. I_f for NRVTSS5100E

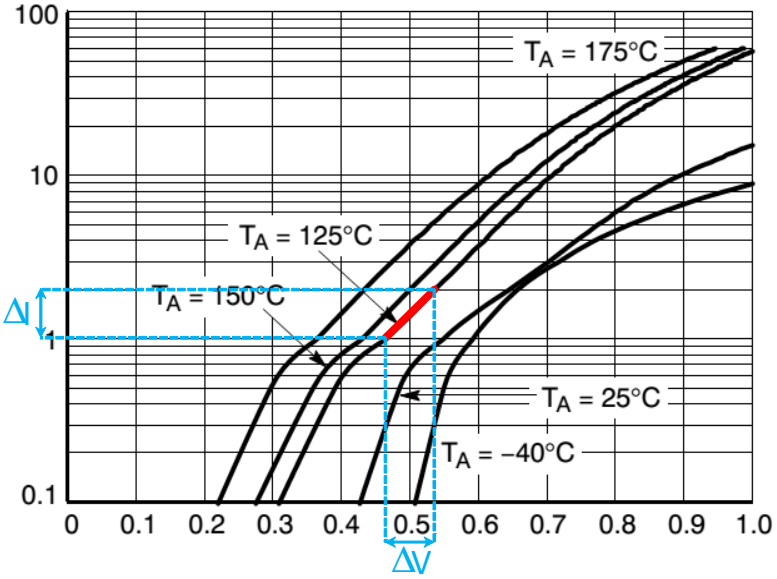

Figure 6. V_f vs. I_f for MBR5100MFS

Table 2. COMPARISON BETWEEN NRVTSS5100E AND MBR5100MFS

Parameters @ 125°C	NRVTSS5100E	MBR5100MFS
V_{f0}	0.21 V	0.31 V
r_d around 1.4 A	90 mΩ	80 mΩ
P_d (eq. 21)	0.386 W	0.467 W

By choosing a diode with a lower forward voltage (and the same average current), the losses can be reduced by almost 20%.

Now, why a 100−V breakdown voltage has been used for the comparison?

This parameter is mostly dependent from the transformer turns ratio and the maximum input voltage. The Peak Inverse Voltage (PIV) is defined by:

$$PIV = N_{ps} V_{in\_max} + V_{out} \quad \text{(eq. 22)}$$

Applying to our case:

$$PIV = 0.145 \times 400 + 12 = 70\ V \qquad \text{(eq. 23)}$$

Due to the leakage inductance, some oscillations can occur at the MOSFET turn−off event so, including some margins, a 100−V maximum reverse voltage is the right choice.

Output Capacitor

The output capacitor is the second component on the secondary side. Combined to the output diode, it contributes to absorb the ac current delivered by the transformer while the dc component is transmitted to the load.

For a classical flyback topology, the output capacitor C_{out} is selected to accept the adequate rms current (2 A in our application) and to limit the undershoot ΔV when the output is subjected to a current step ΔI.

The undershoot depth can be divided in two parts:

1. The drop related to the Equivalent Series Resistance (ESR) of the capacitor.
2. The drop related to the closed−loop operation of the converter. Considering a bandwidth f_c, it can be evaluated via the following formula:

$$\Delta V \approx \Delta I \cdot f_c \cdot C_{out} \qquad \text{(eq. 24)}$$

The typical undershoot during a step load is depicted in the Figure 7.

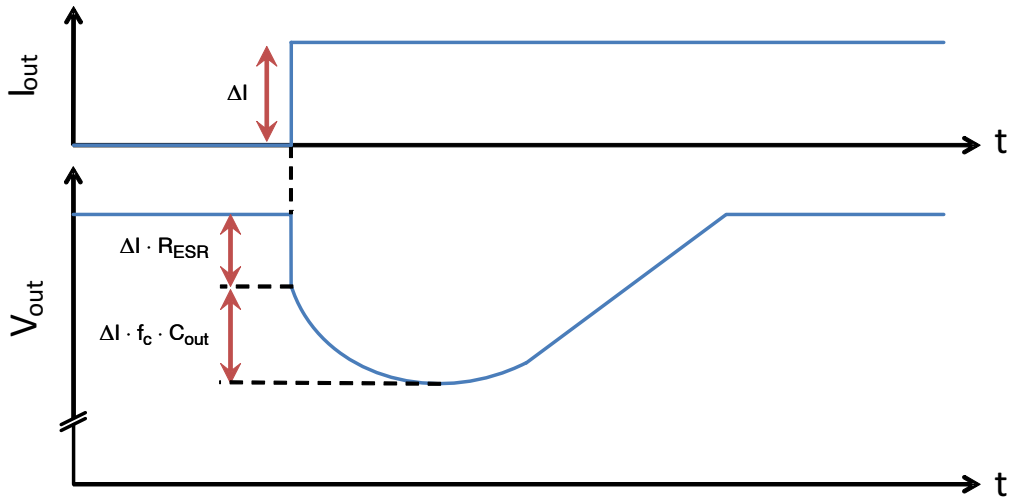

Figure 7. The Typical Response of a Flyback Converter operated in a Closed−loop Condition

An undershoot corresponding to 5% of the output voltage (i.e. 12 V) allows a drop voltage to 600 mV.

For a PSR Flyback application, another parameter has to be considered. Because the output voltage is not directly sensed, the controller limits the minimum switching frequency to 1 kHz in no load condition to have an acceptable step load response.

Indeed, the main limitation of the PSR with the F_{min} is the step load answer. As explained in the datasheet, the output voltage is read on the auxiliary winding at the end of the demagnetization time. Between two cycles, the internal feedback loop is not refreshed so if the step load is applied, the primary controller will not be able to react until 1 ms for the worst case (1 kHz period).

Taking in account this behaviour, the ESR impact can be negligible as shown in Figure 8.

$$\Delta I \cdot R_{ESR} = \frac{\Delta I \cdot t_r}{C_{out}} \qquad \text{(eq. 25)}$$

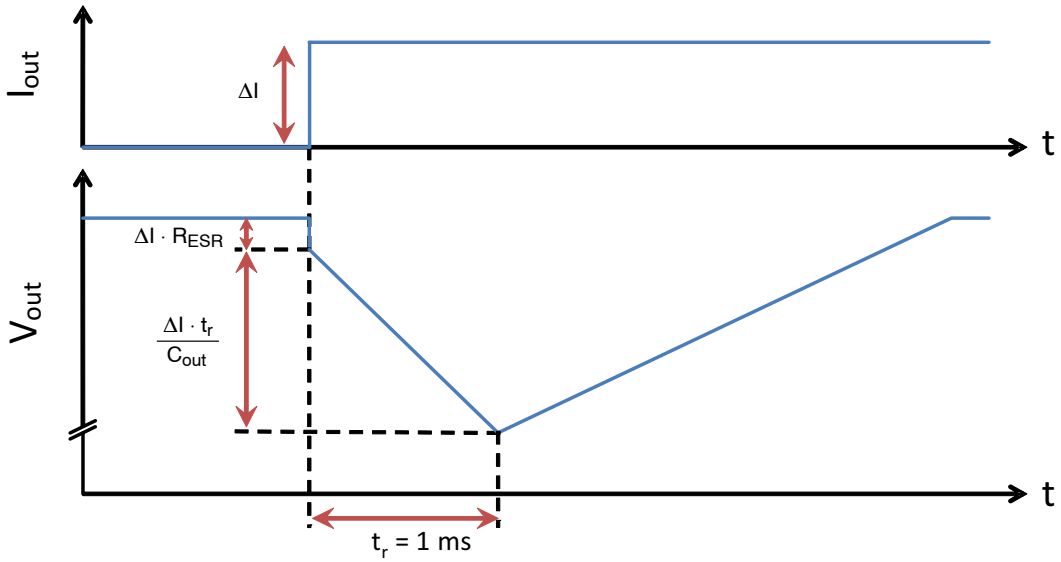

Figure 8. Typical PSR Flyback Output Voltage during a Step Load

Following the above explanation, if we want to limit the undershoot below a 5% deviation, the output capacitor should be:

$$C_{out} = \frac{\Delta I \cdot t_r}{\Delta V} = \frac{1\ A \times 1\ ms}{5\% \times 12\ V} = 1.66\ mF \quad \text{(eq. 26)}$$

By adding a dummy load on the output, the minimum switching frequency can be increased from 1 kHz to 3 kHz for instance. Thanks to this additional SMD resistance, the output capacitor can be reduced to:

$$C_{out} = \frac{1\ A \times 0.33\ ms}{5\% \times 12\ V} = 550\ \mu F \quad \text{(eq. 27)}$$

Step 6: Compensation Network

The PSR controller needs a type 2 compensation to ensure stability. The type 2 has two additional components (a series RC network is added in parallel with a capacitor) compared to the type 1 network. These parts will be needed to implement phase boost at the selected crossover frequency.

All equations related to the power stage with the internal patented implementation have been defined and can be found in the Mathcad spreadsheet (reference [4]). The reference [5] give also the explanation of these formula. From these both references, we can now extract the compensation network values according to the needed Phase Margin (PM) and the Crossover Frequency (F_c).

For our 12−V / 12−W demoboard, the type 2 compensator looks like:

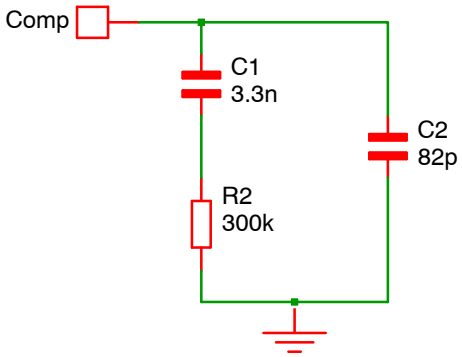

Figure 9. Type 2 Compensation

Step 7: Brown out (BO) and LineFeed Forward (LFF)

The controller embeds a dedicated pin for the BO function and also the LFF. The internal thresholds are set to 0.8 V for the BO turn on level and 0.7 V for the turn off. It means that the pin voltage has to be above the turn on threshold at startup to generate drive pulses (in addition to $V_{cc(on)}$ condition). The switching cycle will be stopped if the voltage drops below 0.7 V.

The target of our application is to have a minimum input voltage at 50 V dc. This voltage will correspond to 0.7 V on the BO pin.

Let us fix arbitrary the lower resistor to 68 kΩ. The needed upper resistor can be found thanks to the following equation:

$$R_{BO\_up} = \frac{R_{BO\_lo} \times V_{in\_min}}{V_{BO(off)}} - R_{BO\_lo} = \quad \text{(eq. 28)}$$

$$= \frac{68k \times 50}{0.7} - 68k = 4.79\ M\Omega$$

We will select 4.7 MΩ as a normalized value. Doing the reverse process will give us the final turn on and turn off input voltage thresholds:

$$V_{in\_start} = \frac{V_{BO(on)} \times (R_{BO\_up} + R_{BO\_lo})}{R_{BO\_lo}} = \quad \text{(eq. 29)}$$

$$= \frac{0.8 \times (4.7M + 68k)}{68k} = 56\ V$$

$$V_{in\_stop} = \frac{V_{BO(off)} \times (R_{BO\_up} + R_{BO\_lo})}{R_{BO\_lo}} = \quad \text{(eq. 30)}$$

$$= \frac{0.7 \times (4.7M + 68k)}{68k} = 49\ V$$

We also need to check that the voltage on this pin at the maximum input voltage do not exceed the maximum rating (ie 5.5 V):

$$V_{BO(max)} = \frac{R_{BO\_lo} \times V_{in\_max}}{R_{BO\_up} + R_{BO\_lo}} = \quad \text{(eq. 31)}$$

$$= \frac{68k \times 400}{4.7M + 68k} = 5.7\ V$$

The result is above the maximum rating for this application so the solution will be to place a Zener diode on the BO pin to clamp the maximum voltage at high input voltage.

The pin 8 also integrates the linefeed forward (LFF) function in order to improve the constant current regulation over the input voltage range. All the calculations are described into the datasheet but one point has to be mentioned related to our particular wide input voltage range application. The LFF current is clamped to 52 μA when the BO pin voltage reaches 3.4 V. It means that above this voltage, there is not compensation anymore.

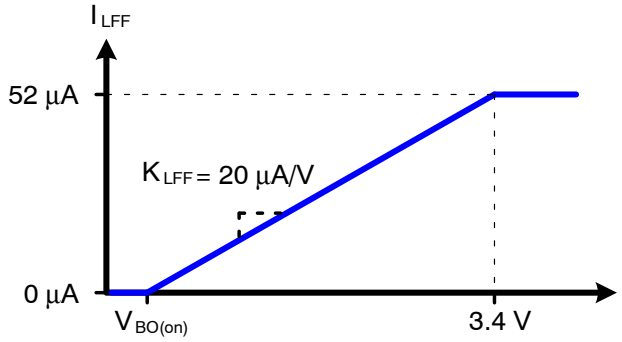

Figure 10. Transfer Function of the Line Feed Forward

With the BO resistors calculated previously, the 3.4−V threshold will correspond to V_{in} = 238 V. So the propagation delay will be well compensated from 50 V to 238 V with an accurate constant current limit. Above this voltage, the output current limit will start to increase.

Step 8: Start−up Resistor

Finally, the startup resistor has been sized in order to find a trade off between the starting duration at low input voltage and the power losses at high line. In the Table 1, we defined at a starting time below 3 seconds. It means that the V_{cc} capacitor has to be charged from 0 V to $V_{cc(on)}$ in less than 2.5 s for instance in order to keep half of a second to charge the output capacitor and reach the 12−V regulation point.

Let's now defined the needed minimum charging current:

$$I_{charge} \geq \frac{V_{cc(on)} \cdot C_{Vcc}}{t_{start-up}} \geq \frac{18 \cdot 2.2\ \mu}{2.5} \geq 16\ \mu A \quad \text{(eq. 32)}$$

If we account for the $I_{CC(start)}$ = 7 μA (maximum) that will flow inside the controller, then the total charging current delivered by the start−up resistor must be 23 μA. Then the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{V_{in\_min} - V_{cc(on)}}{I_{charge}} = \quad \text{(eq. 33)}$$

$$= \frac{50 - 18}{23\ \mu} = 1.39\ M\Omega$$

The dissipated power at high line amounts to:

$$P_{R_{start-up,max}} \approx \frac{V_{in\_max}^{2}}{R_{start-up}} \approx \frac{400^2}{1.39\ M} \approx 115\ mW \quad \text{(eq. 34)}$$

Summary

All the key steps have been described in this application note to design a Dc−Dc power supply around the NCV1362 controller. Several boards have been already designed around this controller but none of them with this particular specification. The best candidate for a laboratory modification will be the NCV1362WGEVB. By looking the schematic of this demoboard shown in the Figure 11, the needed modification have been highlighted in red.

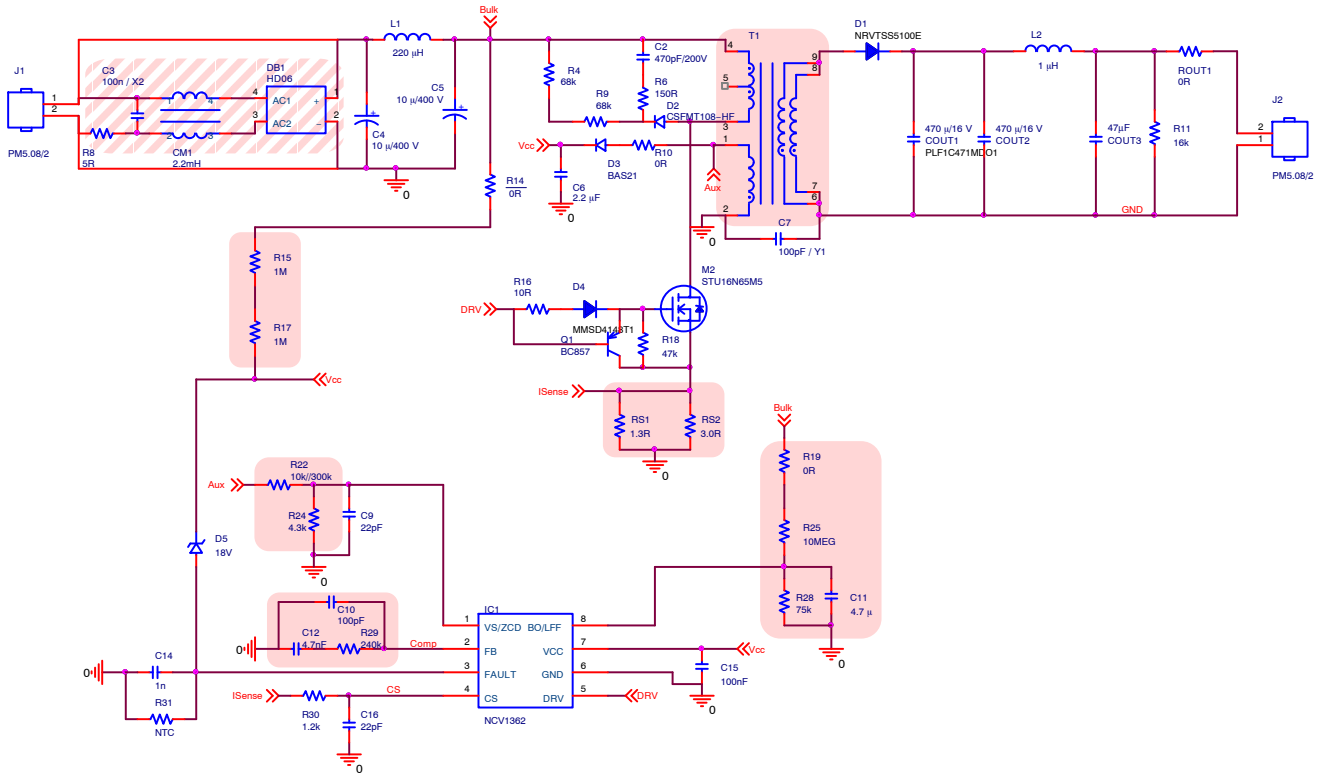

Figure 11. Schematic of the NCV1362WGEVB Demoboard

The first modification is to connect the dc power source directly on the bulk capacitor C_4 since the bridge diode is not more needed. This modification is not mandatory but it will avoid minor power losses into these front end components. Linked to that modification, R_{13} resistor will have to be removed and replaced by R_{14}.

Regarding the power loop, the transformer T_1 with the sense resistances (R_{S1} and R_{S2}) will have to be change according to the above calculations.

Also, in order to adjust to output voltage regulation, the resistor R_{22} and R_{24} will have changed. Laboratory measurements are mandatory to find the right value, calculations will just give us an approximate values.

The type−2 compensation network will have to be changed even if the current value should work properly.

Finally, linked to the minimum input voltage, the BO resistors will have to be updated (R_{25} and R_{28}) like the start−up components (R_{15} and R_{17}). Please also note that the capacitor C_{11} on the BO/LFF pin can be reduced to 10 nF since we have a dc input voltage for this application. Finally, a Zener diode has to be place in parallel of R_{28} (anode on the ground) due to the wide input voltage range.

In second time, some other adjustments could needed to fine tune the behavior of the PSU like LFF compensation via R_{30} or the RCD clamp network dependent of the transformer leakage inductance.

If your requirement regarding input voltage range or output power is different, you just need to change few numbers in the above equations. Also, for higher input voltage like applications connected on the 800−V battery or 1000−V dc input voltage, dedicated boards with SiC MOSFET have been developed for 15 W output power and 40 W..

Conclusion

This paper summarizes the key steps when dimensioning a NCV1362 PSR flyback. The proposed approach being systematic, it can be easily applied to other applications. All the equations (and more) presented have been implemented inside a Mathcad® spreadsheet that can be downloaded from our website [4].

The process has been illustrated by the example of the 12−W, 12−V output voltage with wide DC input voltage.

More details on the circuit operation can be found in its data sheet [2].

References

[1]"Switch−Mode Power Supplies: SPICE Simulations and Practical Designs" 2nd edition by Christophe Basso, McGraw−Hill, New−York, 2012

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[3]NCV1362WGEVB Evaluation board, https://www.onsemi.com/support/evaluation−board/ncv1362wgevb

[4]Yann Vaquette, "NCV1362 Mathcad Spreadsheet" by Yann Vaquette, https://www.onsemi.com/pub/collateral/ncp−ncv1362%20design%20worksheet%20(dc%20input)%20−%20mathcad.zip

[5]Yann Vaquette, "Building An Average Model For Primary−Side Regulated Flyback Converters " by Yann Vaquette, How2Power, March 2017